PART – I, VOL - I

TYPICAL QUESTIONS & ANSWERS

OBJECTIVE TYPES QUESTIONS

Each Question carries 2 marks

Choose correct or the best alternative in the following:

Q.1 A resistor with colour bands Red, Violet, Green and Black will have a value

(A) 27 K ± 10% K
(B) 2.7 M ± 20% K
(C) 270 K ± 5% K
(D) 2.7 K ± 2% K

Ans: B

Q.2 In an n-type semiconductor, as temperature T increases, the Fermi level E_F

(A) moves towards conduction band
(B) moves towards middle of forbidden energy gap
(C) does not vary
(D) may or may not shift depending upon the concentration of donor atoms

Ans: A

Q.3 In a BJT with $\beta = 100$, α equals

(A) 99
(B) 0.99
(C) 1.0
(D) 1.01

Ans: C

Q.4 In integrated circuits, npn construction is preferred to pnp construction because

(A) npn construction is cheaper
(B) to reduce diffusion constant, n-type collector is preferred
(C) npn construction permits higher packing of elements
(D) p-type base is preferred

Ans: B

Q.5 Pinch-off voltage V_P for an FET is the drain voltage at which

(A) significant drain current starts flowing
(B) drain current becomes zero
(C) all free charges get removed from the channel
(D) avalanche break down takes place

Ans: C

Q.6 In SCR, the turn ON time

(A) is independent of V_g
(B) decreases with increase of V_g
(C) varies as V_{g_2}
(D) varies as V_g^2

Ans: A

Q.7 Avalanche breakdown results basically due to

(A) impact ionisation
(B) strong electric field across the junction
(C) emission of electrons
(D) rise in temperature

Ans: A

Q8 Dynamic plate resistance of pentode is of the order of

(A) 1 K Ω **(B)** 10 K Ω
(C) 100 K Ω **(D)** 1M Ω

Ans: D

Q.9 At room temperature, the current in an intrinsic semiconductor is due to

(A) holes **(B)** electronics
(C) ions **(D)** holes and electronics

Ans: D

Q.10 The varactor diode is usually

(A) Forward biased **(B)** reverse biased
(C) Unbiased **(D)** holes and electronics

Ans: B

Q.11 The diode in which impurities are heavily doped is

(A) Varactor diode **(B)** PIN diode
(C) Tunnel diode **(D)** Zener diode

Ans: C

Q.12 A transistor in common emitter mode has

(A) a high input resistance and low output resistance
(B) a medium input resistance and high output resistance
(C) a very low input resistance and a low output resistance
(D) a high input resistance and a high output resistance

Ans: B

Q.13 In an SCR the holding current is

(A) more than latching current **(B)** less than latching current
(C) equal to latching current **(D)** very small

Ans: B

Q.14 The negative potential at the control grid in a vacuum triode that causes plate current Zero is called

(A) cut off bias **(B)** cut in voltage
(C) reverse blocking voltage **(D)** forward blocking voltage

Ans: A

Q.15 A constant current source supplies a current of 300 mA to a load of 1 Kohm. When the Load is changed to 100 ohm, the load current will be

(A) 3 Amp **(B)** 300 mAmp
(C) 30 mAmp **(D)** 600 mAmp

Ans: B

Q.16 An Op-amp as a voltage follower has a voltage gain of

(A) Infinity **(B)** Zero
(C) Unity **(D)** less than unity

Ans: C

Q.17 A resistor used in colour TV has the following colour bands: yellow, violet, orange and silver. Its nominal value is

(A) 4.7 KΩ $\pm$ 10 % **(B)** 4.7 KΩ $\pm$ 5 %
(C) 47 KΩ $\pm$ 10 % **(D)** 470 KΩ $\pm$ 5 %

Ans: C

Q.18 Ratings on a capacitor are given 25 μ F, 12 V. Also a plus sign is written near one of its terminals. The capacitor is

(A) mica capacitor **(B)** ceramic capacitor
(C) electrolytic capacitor **(D)** paper capacitor

Ans: C

Q.19 An ideal voltage source of 12 V provides a current of 150 mA to a load connected across it. If the load impedance is halved, the new load current will be

(A) 0.3 A **(B)** 0.15 A
(C) 0.6 A **(D)** 1.2 A

Ans: A

Q.20 An intrinsic semiconductor at the absolute zero temperature

(A) behaves like a metallic conductor
(B) behaves like an insulator
(C) has a large number of holes
(D) has a large number of electrons

Ans: B

Q.21 Which of the following diodes is operated in reverse bias mode ?

(A) P-N junction **(B)** Zener
(C) Tunnel **(D)** Schottky

Ans: B

Q.22 Compared to bipolar transistor, a JFET has

(A) lower input impedance
(B) higher voltage gain
(C) higher input impedance and high voltage gain
(D) higher input impedance and low voltage gain

Ans: D

Q.23 The minimum gate current which can turn on SCR is called

(A) trigger current **(B)** holding current
(C) junction **(D)** break over current

Ans: A

Q.24 A virtual ground

(A) is a ground for voltage
(B) is a ground for both voltage and current
(C) is ground for current
(D) is a ground for voltage but not for current

Ans: D

Q.25 Which of the following doping will produce a p-type semiconductor

(A) Germanium with phosphorus **(B)** Silicon with Germanium
(C) Germanium with Antimony **(D)** Silicon with Indium

Ans: D

Q.26 The majority charge carriers in the emitter of an NPN transistor are

(A) pentavalent atoms **(B)** trivalent atoms
(C) electrons **(D)** holes

Ans: C

Q.27 An ideal differential amplifier has CMRR equaling

(A) Unity
(B) – 1 (minus unity)
(C) Infinity
(D) Zero

Ans: C

Q.28 Which of the following is an active device

(A) an electric bulb
(B) a diode
(C) a BJT
(D) a transformer

Ans: C

Q.29 Which configuration has unity voltage gain (ideal)

(A) a Common Collector (CC)
(B) a Common Emitter (CE)
(C) a Common Base (CB)
(D) CE followed by CB

Ans: A

Q.30 JFET is a

(A) Current controlled device with high input resistance
(B) Voltage controlled device with high input resistance
(C) Current Controlled Current Source (CCCS)
(D) Voltage Controlled Voltage Source (VCVS)

Ans: B

Q.31 The depletion region in a Junction Diode contains

(A) only charge carriers (of minority type and majority type)
(B) no charge at all
(C) vacuum, and no atoms at all
(D) only ions i.e., immobile charges

Ans: D

Q.32 Photo-electric emission current is proportional to

(A) frequency of the incident light
(B) incident light flux
(C) work function of photo-cathode
(D) angle of incidence of radiation

Ans: A

PART – II, VOL – I

NUMERICALS

Q.1 Power is to be supplied from a source whose resistance is 20 KΩ to a load of 100 Ω. Would you consider it as a constant current source or voltage source? Explain. **Marks (6)**

Ans:

The given source is considered as a constant current source because, a source which has a very high internal resistance (20 KΩ) as compared to the load resistance (100 Ω) is a constant current source.

Explanation: In fig.1(a), a load impedance Z_L is connected to a current source. Let is be the short-circuit current of the source, and Z_s be its internal impedance. The current is is divided into two parts I_1 through Z_s and I_L through Z_L. That is

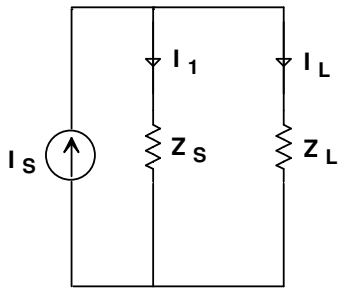


Fig.1(a)

$$I_S = I_1 + I_L$$

or $$I_1 = I_S - I_L$$

Since the impedance Z_s and Z_L are in parallel, the voltage drop across each should be equal, i.e.,

$$I_1 Z_S = I_L Z_L$$

$$(I_S - I_L)\, Z_S = I_L$$

$$I_L = I_S \frac{Z_S}{Z_S + Z_L} = \frac{Z_S}{1 + \left(\frac{Z_L}{Z_S}\right)}$$

The above equation tells us that the load current I_L will remain almost the same as the current I_S, provided the ratio Z_L/Z_S = 100/20000 = 1/200 is small compared to unity. The source then behaves as a good current source. In other words, the larger the value of internal impedance Z_S (20KΩ) compared to the load impedance Z_L (100Ω), the smaller is the ratio Z_L/Z_S, and the better it works as a constant current source.

Q.2 The current flowing in a certain PN junction at room temperature is 2 X 10^{-7} A, when a large reverse bias voltage is applied. Calculate the current when a forward voltage of 0.1 V is applied across the junction. **Marks (6)**

Ans:

The diode current is given as $I = I_O\left(e^{V/\,V_T} - 1\right)$

From given data:

Large reverse bias current $I \approx I_O = 0.2\ \mu A$
Applied Voltage $V = 0.1$ V
Volt-equivalent of temperature, $V_T = 26$ mV or 0.026 V at room temperature

so, the current flowing through the diode, $I = 0.2 \times 10^{-6}\left(e^{0.1\ /\ 0.026} - 1\right) = 29.38\ \mu$ A

Q.3 Determine the voltage gain for the circuit shown in fig 3(a), with $R_F = 100K\,\Omega$ and $R_1 = 10\ K\,\Omega$ **Marks (4)**

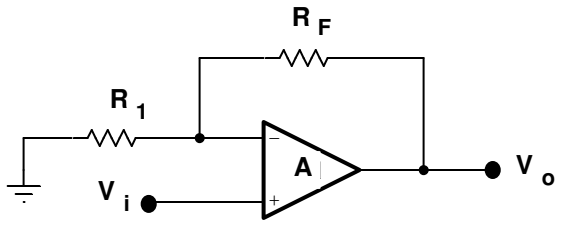


Fig.3(a)

Ans:

Determination of voltage gain:

The given operational amplifier is a non-inverting amplifier. By virtual ground, the voltage at inverting terminal of Op-amp is also V_i. Writing KCL at this terminal gives

$$\frac{0 - V_i}{R_1} = \frac{V_i - V_o}{R_F} \quad \text{OR} \quad \frac{V_o}{V_i} = 1 + \frac{R_F}{R_1} = A_V$$

From the given data $R_F = 100\ K\Omega$ and $R_1 = 10\ K\Omega$

$$A_V = 1 + \frac{100}{10} = 1 + 10 = 11$$

Q.4 Determine current flowing through $5\,\Omega$ resistor in the circuit shown at Fig.4(a) . Use Source transformation technique. **Marks (3)**

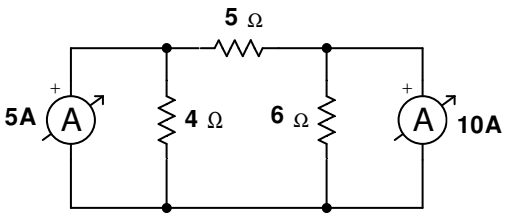


Fig.4(a)

Ans:

Determination of current flowing through 5 Ω resistor

The two current sources cannot be combined together because of the 5 Ω resistance presence between points A and C shown in fig.4(b) However, the hurdle can be removed by converting 5 A current source into the equivalent voltage source of 20 V and 10 A current source can be converted into the equivalent voltage source of 60 V as shown in fig.4 (c)

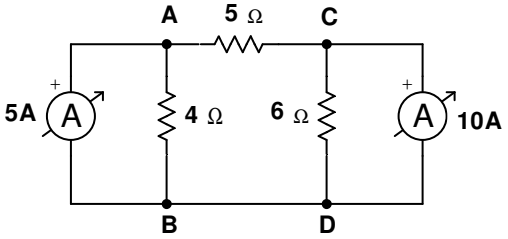


Fig.4(b)

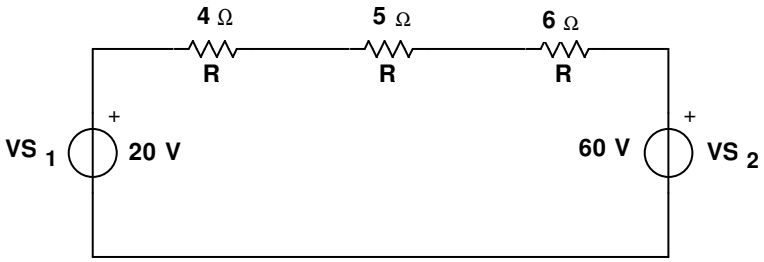


Fig. 4(c)

The circuit shown in above fig.4(c) is a simple series circuit having total voltage of 40V and total resistance of 4 + 5 + 6 = 15 Ω . So, the current flowing through the 5 Ω resistance is equal to $\frac{40}{15} = 2.667A$

Q.5 A triode valve acting as an amplifier gives a voltage gain of 30. If the anode resistance is 20 K Ω for the valve and load resistance is 60 K Ω , what is the value of amplification factor for the valve? **Marks (2)**

Ans:

Given data;

Voltage gain (A) = 30

Anode or Plate resistance (r_p) = 20 K Ω

Load resistance (R_L) = 60 K Ω

Formula to be used is

$$A = \frac{\mu}{1 + \frac{r_p}{R_L}}$$

$$30 = \frac{\mu}{1 + \frac{20}{60}}$$

Amplification Factor (μ) = 39.999

Q.6 Determine the range of V for obtaining a regulated voltage shown in Fig.5(a) for the data $0 \leq I_L \leq 4$ mA
$2 \leq I_Z \leq 8$ mA **Marks (7)**

Ans:

Determination of range of V for the given circuit diagram shown in fig.6(a):

In the fig.6(a), the voltage across the series or current limiting resistor equals the difference between the source voltage and zener voltage. Therefore, the current through the series resistor R_S is given by

$$I_S = \frac{V_S - V_Z}{R_S}$$

The zener diode and the load resistor are in parallel. So, the sum of their currents has to equal the total current, which is the same as the current through the series resistor. i.e.,

$I_S = I_Z + I_L$

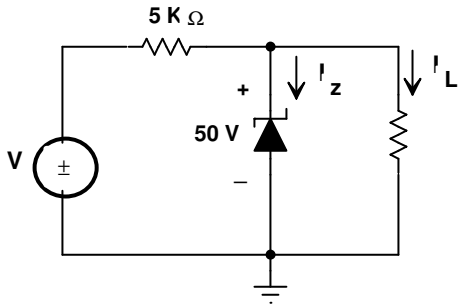


Fig.6(a)

From the given data the load current is in between 0 mA (I_{LMIN}) and 4 mA (I_{LMAX}) and the Zener current is in between 2 mA (I_{ZMIN}) and 8 mA (I_{ZMAX}).

(i) **The minimum value of Source Current is given by**

$I_{s(min)} = I_{z(min)} + + I_{L(min)}$ i.e.,
$I_{S\,(MIN)}$ = 2 mA + 0 mA = 2 mA, and
The minimum value of source current is given by

$$I_{S(MIN)}) = \frac{V_{S(MIN)} - V_Z}{R_S}$$

From the fig.3.1, V_Z = 50 V and R_S = 5 KΩ

$$2X10^{-3} = \frac{V_{S(MIN)} - 50}{5X10^3}$$

Therefore, the minimum value of source voltage is given by

$V_{S\,(MIN)} = 50 + 10 = 60$ V

(ii) **The maximum value of source current is given by**

$I_{SMAX} = I_{ZMAX} + I_{LMAX}$

= 8 mA + 4 mA = 12 mA and

The maximum value of source current is given by

$$I_{S(MAX)} = \frac{V_{S(MAX)} - V_Z}{R_S}$$

$$12X10^{-3} = \frac{V_{S(MAX)} - 50}{5X10^{3}}$$

Therefore, the maximum value of source voltage is given by

V_{SMAX}= 50 + 60 = 110 V

The value of source voltage is $50 \le V_S \le 110$ V

Q.7 For the circuit shown in fig.7(a), draw the waveform of output voltage Vo. Assume ideal diode D and lossless capacitor C.

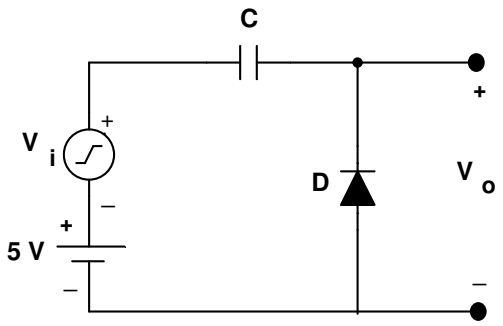


Fig.7(a)

Ans:

The name of the circuit given in fig 7.(a) is Positive Clamper. A circuit that shifts the signal in the positive side in such a way that the negative peak of the signal falls on the zero level, is called a Positive Clamper.

Working:

During negative half-cycle of the input voltage, the diode conducts heavily and acts like a closed switch see fig 7.c(i). The capacitor C is charged to 5 V (V_m) at the negative peak of the signal with the polarity as marked. Slightly beyond the negative peak, the diode stops conduction through it and behaves as an open switch (see fig.7c(ii)). The charged capacitor (V_m = 5V) just behaves as a battery whose voltage adds to the signal voltage, see fig7.c(ii).During positive half-cycle of the signal, the diode is reverse biased and acts as an open switch. The resultant output voltage coming across the load resistor R_L will be as shown in Fig.7(b): By writing KVL to the circuit shown in fig5.a (iii)., we get 5V + 5V – Vo = 0 i.e.,

Output Voltage (V_o) = 10 V.(at positive peak)

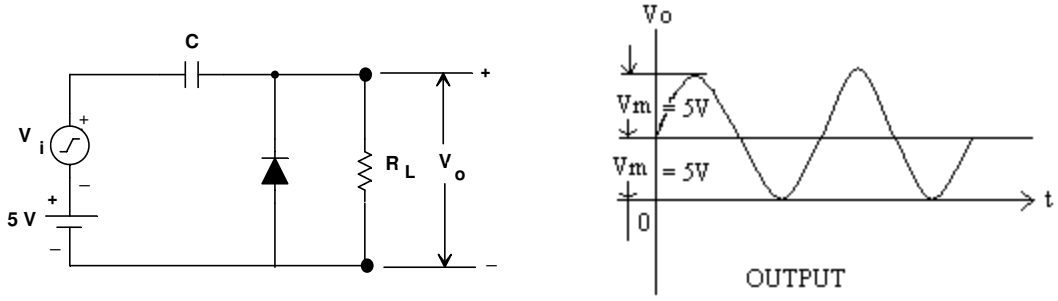


Fig.7.(b).Positive Clamper adds a dc component (5V) to signal

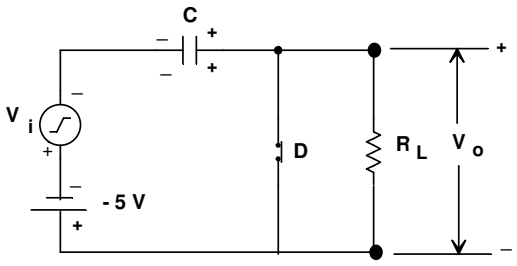


Fig.7.c (i)

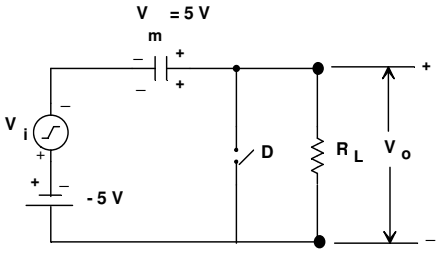
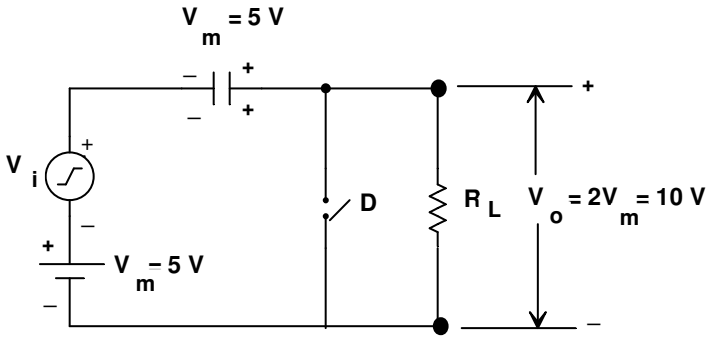


Fig.7.c (ii)



DESCRIPTIVE TYPE QUESTIONS

Q.1 Draw and explain the V-I characteristics of constant current and constant voltage sources. **Marks (4)**

Ans: **V-I Characteristics of Constant Voltage Source:** A voltage source, which has very low internal resistance (or impedance) as compared to load resistance (or impedance) is known as a Constant Voltage Source.

A real voltage source (constant voltage source) has some internal resistance. For instance, a flashlight battery has an internal resistance of less than 1 ohm, a car battery has an internal resistance of less than 0.1 ohm, and an electronic voltage source may have an internal resistance of less than 0.01 ohm. A real voltage source, having an internal resistance of 0.01 ohm with load resistance R_L is shown in below fig.1(a). When, a load resistance varies from 11.99 ohm to 1.19 ohm, the terminal voltage varies from 11.99V to 11.9 V and the load current varies from 10A to 1A respectively.

$$V = \frac{E \times R_L}{Ri + R_L}$$

$$i.e. V = \frac{12 \times 11.99}{0.01 + 11.99} = 11.99V$$

This shows that the terminal voltage remains constant and the source behaves as a constant voltage source irrespective of load current, as shown in fig.1(b).

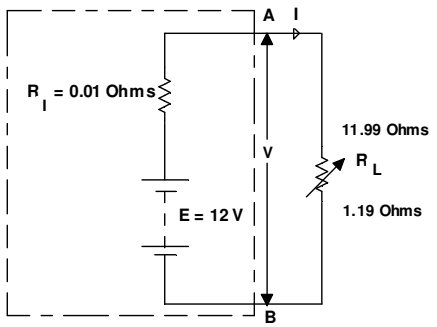


Fig. 1(a)

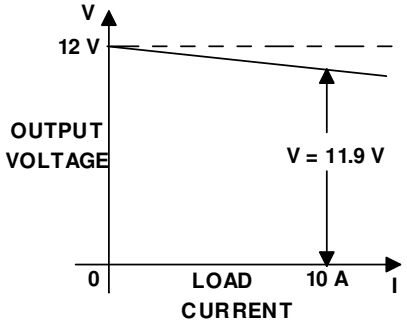


Fig.1(b)

V-I Characteristics of Constant Current Source: A source that has high internal resistance (or impedance) as compared to the load resistance (or impedance) is considered as a constant current source.

A real current source has high internal resistance. For instance a real current source having an internal resistance of 10 MΩ with load resistance R_L is shown in below fig. 1(c). When load resistance varies from 1 KΩ to 100 KΩ,

$$I = \frac{E}{R_i + R_L} = \frac{12}{10.001} = 1.1881\ \mu A$$

∴The current varies from 1.19988 μA to 1.1881 μA.

This shows that the load current remains almost constant and the source behaves as constant current source irrespective of the value of load resistance, which is shown in fig.1(d).

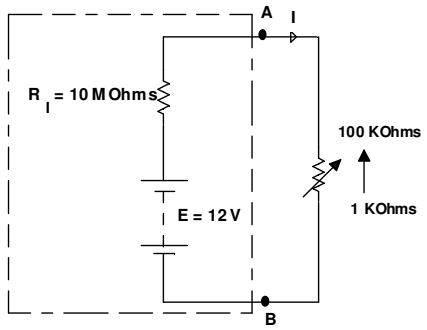


Fig. 1(c)

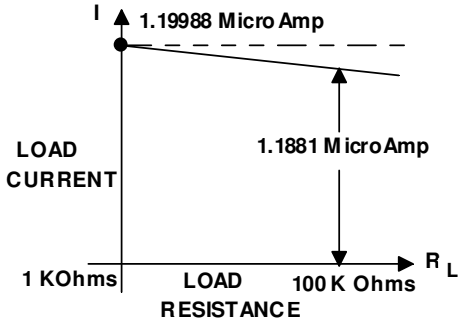


Fig.1(d)

Q.2 While designing and constructing Inductance standards, what considerations should be taken into account ? **Marks(4)**

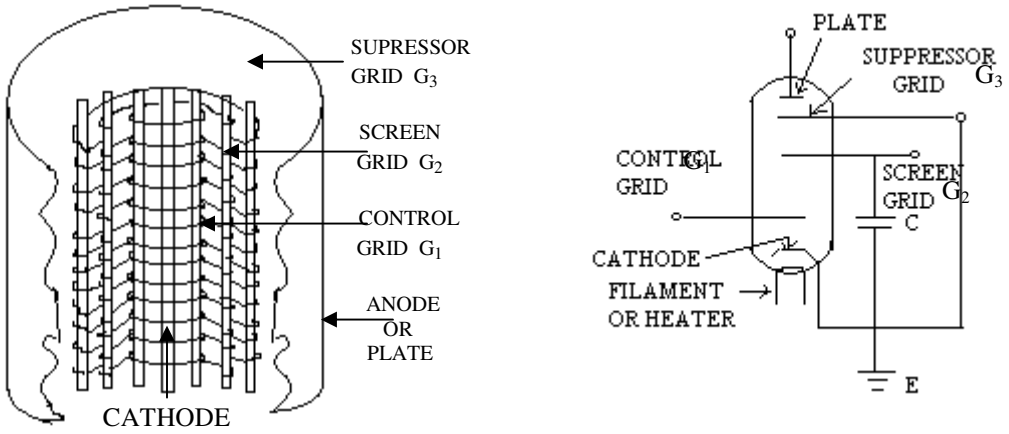
Ans: **Construction of Inductors:**

The constructional features of an inductor are determined largely by the frequency range in which it is to operate. In general, low frequency inductors have many turns and employ an iron core. In contrast high-frequency inductors have fewer turns and often employ an air core. The stray capacitance between the turns and between the layers of turns is an important factor in high-frequency coils, and therefore special winding configurations may be employed to minimize this capacitance

Current and voltage considerations also determine the constructional features of an inductor. The gauge of the wire, for example, is selected in accordance with the amount of current the coil must carry. Receiver coils, which normally carry only a few milli-amperes of current, are therefore wound from fine wire. Transmitter coils, however, often carry much greater currents and are wound using heavier wire. The spacing between turns, the insulation of the wire, and the insulation between layers of turns must be adequate to prevent voltage breakdown and arcing. An inductor designed for use in high-voltage circuits will, therefore, have heavier insulation than one designed for low-voltage applications. Inductors may be made of Iron core, Powder core, Ferrite core or Air core depending upon the frequency range of their operation.

Q.3 Give the basic construction of pentode. **Marks (4)**

Ans: **Construction of Pentode:** The constructional details of a typical pentode are shown in fig.3(a) and fig.3(b) Pentode consists of five electrodes namely a cathode, three grids (suprressor grid, screen grid, control grid) and a plate. The grid closest to the cathode is the control grid, next is the screen grid, and the third is the suppressor grid. The suppressor grid is usually coarser than the control grid or even the screen grid mesh and is placed very close to the plate. It does not obstruct the flow of electrons from cathodes to anode (or plate). To keep the control grid-to-plate capacitance small extra shields are provided either within the glass envelope or external to it. In the latter case the bulb is so shaped as to allow the shield to come very near to the plate.



(a) Cut-away-View (b) *Symbolic Representation*

Pentode

Fig. 3

Q.4 Draw and discuss Pentode Plate Characteristics. **Marks (6)**

Ans: **<u>Pentode Plate Characteristics</u>**: Pentode plate characteristics (plate current-plate voltage curves at constant grid voltage) are plotted in fig.4(a)

1. The characteristics are non-linear below the knee of the curve.
2. The dip noticed in the plate characteristics of a tetrode is eliminated in the pentode plate characteristics. This is due to the suppression effect of suppressor grid.
3. Over the major portion (above the knee) of the characteristics plate current is largely independent of plate voltage. So the pentode may be thought as a constant current device. A pentode is usually operated in this region.

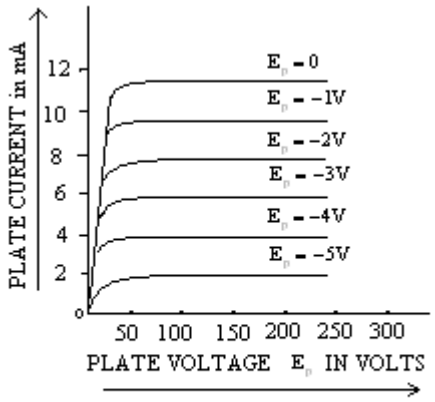


Plate Current-Plate Voltage Characteristics of a Pentode

Fig. 4(a)

Q.5 Explain how suppressor grid eliminates the effect of secondary emission in pentode **Marks (4)**

Ans: Suppressor grid is placed in between the plate and screen grid. It is connected with the cathode and obtains the same potential as that of cathode. Since the suppressor grid is at negative potential with respect to plate, the secondary electrons emitted from the plate are repelled back to plate or suppressed by it. Thus the effect of secondary emission is eliminated.

Q.6 Describe the phenomenon of avalanche and zener breakdown. **Marks (4)**

Ans: **Avalanche Breakdown:** The minority carriers, under reverse biased conditions, flowing through the junction acquires a kinetic energy, which increases with the increase in reverse voltage. At a sufficiently high reverse voltage (say 5v or more), the kinetic energy of minority carriers becomes so large that they knock out electrons from the covalent bonds of the semiconductor material. As a result of collision, the liberated electrons in turn liberate more electrons and the current becomes very large leading the breakdown of the crystal structure itself. This phenomenon is called Avalanche Breakdown.

Zener Breakdown: Under a very high reverse voltage, the depletion region expands and the potential barrier increases leading to a very high electric field ($3X10^7$ V/m) across the junction. The electric field will break some of the covalent bonds of the semiconductor reverse current. This is called the Zener effect. The breakdown occurs at a particular and constant value of reverse voltage called the breakdown voltage.

Q.7 Sketch V-I characteristics of a zener diode. How are they determined in the laboratory ? **Marks (6)**

Ans: **Determination of Forward and Reverse Characteristics of a Zener Diode in the laboratory**:

Forward Characteristic of Zener diode: Connect the circuit shown in fig 7(a) using the 5.1 V zener diode. For forward characteristic, reverse the connection of the zener diode.

Switch on the variable dc power supply. Observe and record the voltage across the diode for various values of currents say, 1 mA, 10 mA and 30 mA. The current can be varied by varying the power supply voltage. Observe and record the corresponding voltage too. It should be evident that the forward characteristic is similar to that of a junction rectifier diode as shown in below fig.7 (b)

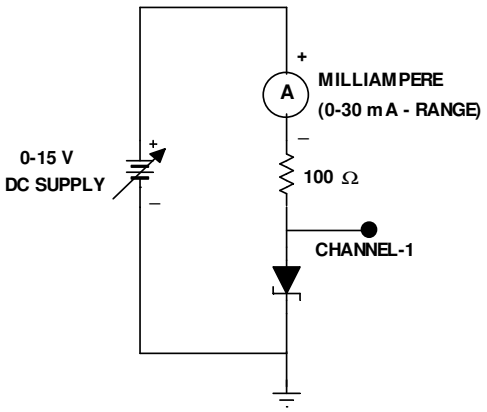


Fig 7(a) circuit arrangement

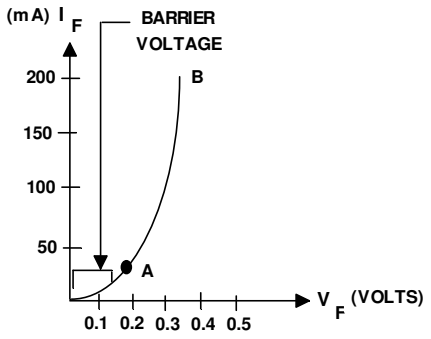


Fig 7(b) characteristic

Reverse Characteristic of a Zener diode: Reset the voltage to zero. Connect zener diode as shown in fig.7(c) and the reverse characteristics are shown in fig. 7(d)

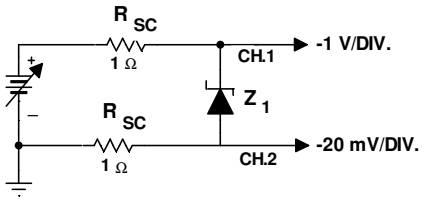


Fig.7(c) circuit arrangement

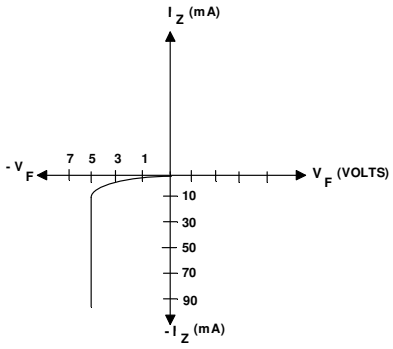


Fig.7 (d) characteristics

Raise the voltage slowly and observe the current meter. Set the value of the zener current of 1 mA, 2 mA, 5 mA, 10 mA, 20 mA, 30 mA and record the corresponding voltage drop across the diode and plot the points on the graph.

The graph should show that very little current flows until the voltage has risen to a value near the nominal voltage (5.1 V) of the zener diode. However, a very slight increase in voltage causes a large current to flow. Once an appreciable current is flowing in the diode, any alteration in that current will make little difference to the voltage. The terminals to which voltmeter is connected will look like a source of voltage having a low source resistance. This voltage may be referred to as the 'zener voltage' or the avalanche voltage, (this being a reference to the physical process inside the semiconductor).

Q.8 Can an ordinary diode be used as a zener diode? Justify your answer. **Marks (4)**

Ans: Ordinary diode cannot be used as a Zener diode, because the ordinary diodes are not operated in the reverse bias breakdown region to avoid them from damaging. These diodes are normally operated in forward region and never operated in reverse region, since small signal and rectifier diode are never operated in breakdown (or reverse region). Zener diode is a specially designed silicon diode, which is optimized to operate in the breakdown region.

Q.9 What is meant by tunneling phenomenon? **Marks (4)**

Ans: **Tunneling Phenomenon**: A tunnel diode is a high conductivity two-terminal P-N junction doped heavily about 1,000 times higher than a conventional junction diode. Because of heavy doping depletion layer width is reduced to an extremely small value of the order of 10^{-5} nm, reverse breakdown voltage is also reduced to a very small value (approaching zero) resulting in appearance of the diode to be broken for any reverse voltage, and a negative resistance section is produced. It is found that the reduced depletion layer can result in carriers 'punching through' the junction with the velocity of light even when they do not possess enough energy to overcome the potential barrier. The result is that large forward current is produced at relatively low forward voltage (less than 100 mV). Such a mechanism of conduction in which electrons (possessing very little energy) punch through a barrier directly instead of climbing over it is called tunneling phenomenon.

Q.10 Draw the energy band diagrams of a tunnel diode for different biasing conditions and Describe how tunneling takes place. **Marks (6)**

Ans: **Band Diagrams of a Tunnel diode:** The energy band diagram for a heavily doped unbiased P-N junction is shown in fig. 10(a) Note that the depletion region is very narrow and the filled levels on the N-side are exactly opposite those on the P-side. In this condition, no tunneling occurs, as there are no empty lower energy levels to which electrons from either side might cross the depletion region. It is also to be noted that the conduction and the valence bands on p- side are (negatively) higher than those on the n-side, this is due to the formation of the depletion region and barrier potential as a result of electrons crossed from the n-region to the p-region. The n-region has lost negative charge and p-region has gained them.

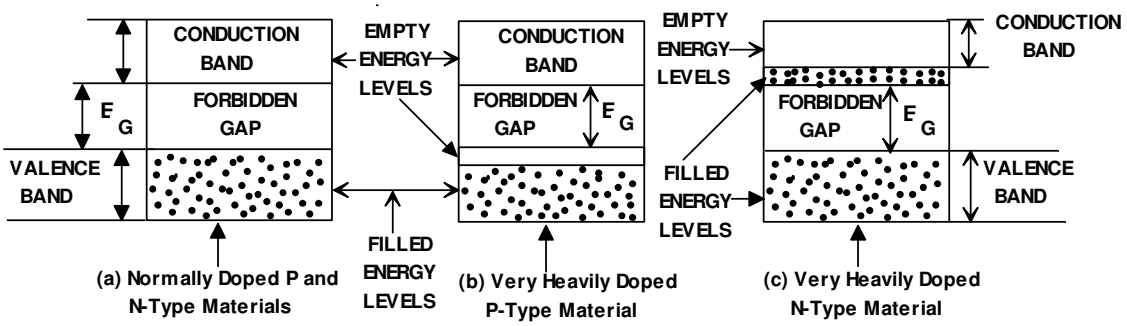
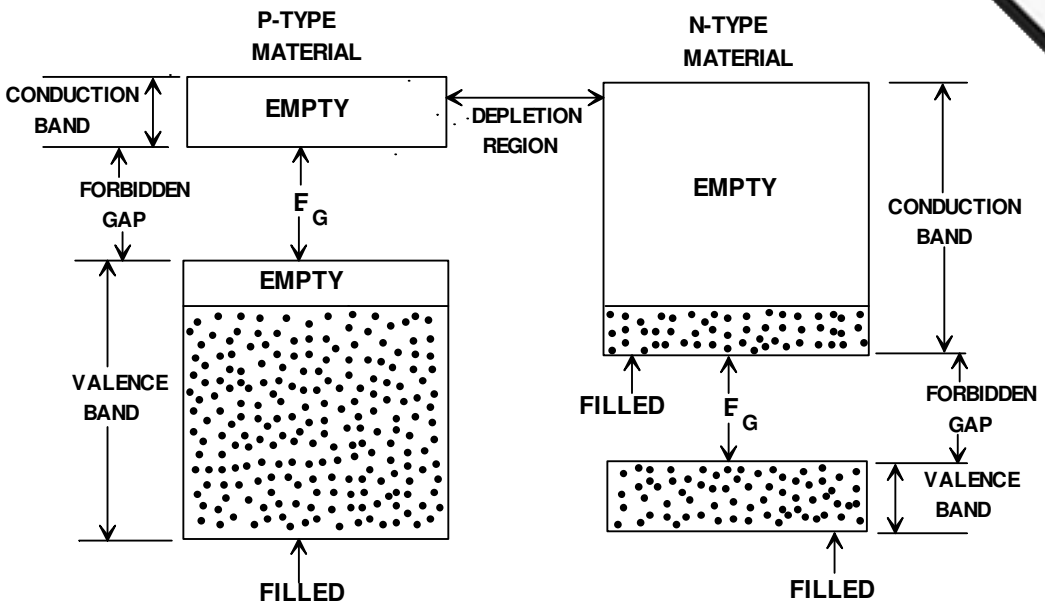


Fig. 10

When the junction is reversed biased, the p-region moves up with respect to the n-region as a result, filled energy levels on the p- side become opposite empty energy levels on the n-side. At this stage electrons tunnel through the narrow space charges region from the higher energy levels on the p- side to the lower energy levels on the n- side. Despite the fact that the junction is reverse biased significant current flows. With the increase in reverse bias, more and more electrons tunnel from the p-side to n-side and a larger current flow. Thus the reverse characteristic of a tunnel diode is liner, just like that of a resistor.

When the tunnel diode is forward biased, its initial behaviour is similar to that when it is reverse biased. Now, some of the filled energy levels on the n-side shift to a high energy level than empty level on the p-side electron tunneling now occurs, from the n-side to the p-side. With the increase in forward bias, more and more electrons tunnel from the N-side to the P-side.



Q.11 Draw and discuss the volt-ampere characteristics of a tunnel diode. **Marks (4)**

Ans: **Volt-ampere characteristics of a tunnel diode**: The V-I characteristics of a tunnel diode are shown in fig. 11(a) Forward bias produces immediate conduction as soon as forward bias is applied, significant current is produced. The current attains quickly its peak value I_p, when the applied forward bias attains a value of V_p volts. The current variation in the vicinity of origin is due to quantum mechanical tunneling of electrons through narrow space charge region of the junction. With the further increase in forward voltage, the diode current starts decreasing till it attains its minimum value, called the valley current I_v corresponding to valley voltage V_v. Thus from peak point A to valley point B the diode current falls with the increase in voltage resulting in negative resistance in this region. In fact this portion A B of the characteristic constitutes the most useful property of the diode. In this region the diode, instead of absorbing power, produces power. So the tunnel diode can be used as a very high frequency oscillator. For voltages higher than valley voltage V_v current starts increasing as in any normal diode.

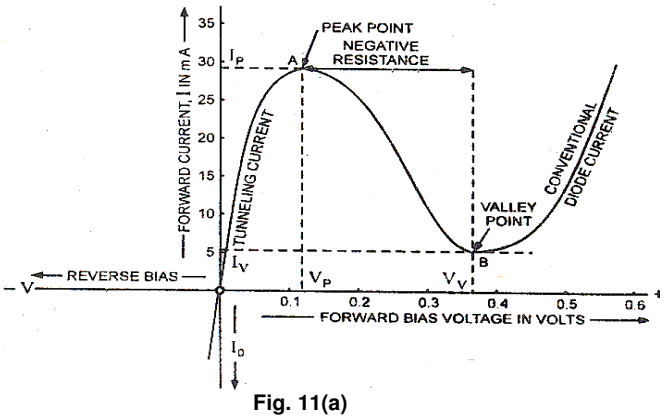


Fig. 11(a)

Q.12 Compare the merits and demerits of semiconductor diodes and vacuum diodes.

Marks (4)

Ans: **Merits of Semiconductor Diode over Vacuum Diode**:

(i) Smaller in size
(ii) Greater efficiency
(iii) Cheaper
(iv) Robust

Demerits of Semiconductor Diode over Vacuum Diode:

(i) It cannot withstand high reverse voltage
(ii) It cannot operate at fairly high temperatures.

Merits of Vacuum Diode over Semiconductor Diode:

(i) Vacuum Diodes can withstand high reverse voltages
(ii) Vacuum Diodes can operate at fairly high temperatures.

Demerits of Vacuum Diode over Semiconductor Diode:

(i) Bigger in size
(ii) Less efficiency
(iii) Expensive

Q.13 Explain the formation of a potential barrier in a p-n junction and show the polarity of the Barrier potential.

Marks (6)

Ans: **Formation of Potential Barrier in a P-N junction**: The two types of extrinsic semiconductors p-type and n-type are shown in fig. 13(a). The p-type semiconductor is having negative acceptor ions and positively charged holes. Whereas, the n-type semiconductor is having positive donor ions and negatively charged electrons.

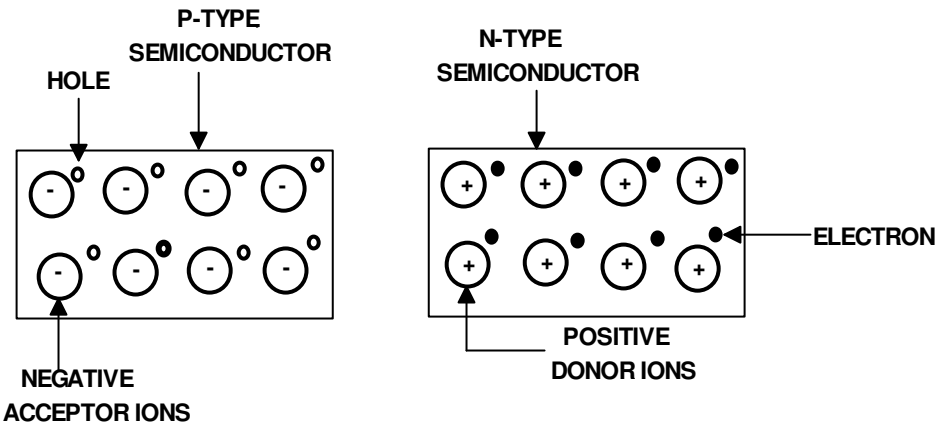


Fig. 13(a)

When these two pieces are joined together and suitably treated, they from a pn junction. The moment they form a pn junction, some of the conduction electrons from n-type material diffuse over to the p-type material and undergo electron-hole recombination with the holes available in the valence band. Simultaneously holes from p-type material diffuse over to the n-type material and undergo hole-electron combination with the electrons available in the conduction band. This process is called diffusion. In this process, some of the free electrons move across the junction from n-type to p-type, leaving behind positive donor ions as they are robbed of the free electrons. This establishes a positive charge on the n-side of the junction.

Simultaneously, the free electrons which cross over the junction recombine with t holes of p-type and uncover some of the negative acceptor ions as shown in fig. 13(b). This establishes a negative charge on the p-side of the junction. This process of diffusion continues till a sufficient number of donor and acceptor impurity ions are uncovered and establish a requisite potential difference (i.e. nearly 0.3 V in case the pn junction is formed of germanium semiconductor and 0.7 V for silicon pn junction). After this, further diffusion is prevented because now positive charge on n-side repels holes to cross from p-type to n-type and negative charge on p-side repels free electrons to enter from n-type to p-type. Thus, a potential difference created across the junction acts as a barrier which restricts further movement of charge carriers i.e. holes and electrons. This is called a Potential Barrier or Junction Barrier V_o

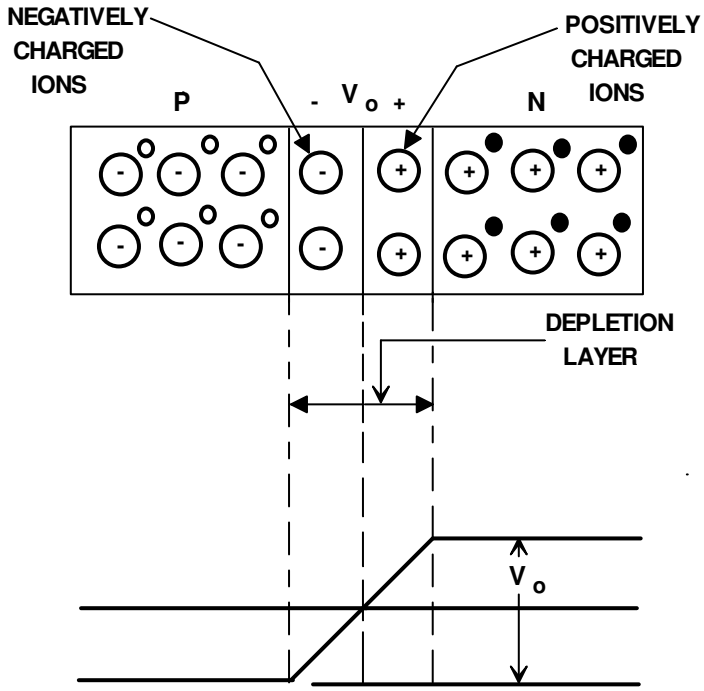


Fig. 13(b)

Q.14 Explain physically how a p-n junction functions as a rectifier. **Marks (4)**

Ans: When a P-N junction diode is forward-biased and the applied voltage is increased from zero, hardly any current flows through the device in the beginning. It is so because the external voltage is being opposed by the internal barrier voltage V_B whose value is 0.7 V for Silicon and 0.3 V for Ge. As soon as V_B is neutralized, current through the diode increases rapidly with increasing applied battery voltage. So, in forward bias condition, the P-N junction diode behaves like a closed switch. When a P-N junction diode is reverse biased, majority carriers are blocked and only a small current (due to minority carriers) flows through the diode. It is of the order of nanoamperes (nA) for Si and microamperes (μA) for Ge. For all practical purposes, this current is almost negligible. So, in Reverse bias condition, the P-N junction diode behaves like an open switch. So, the above discussion shows that the P-N junction functions as a rectifier.

Q.15 Compare CB and CE transistor configurations with regard to AC input and outp resistance.

Marks (6)

Ans: **AC Input Resistance in Common Base Configuration**: The ratio of change in emitter-base voltage (ΔV_{EB}) to the resulting change in emitter current (ΔI_E) is known as input resistance, i.e., at constant V_{CB}

$$R_i = \frac{\Delta V_{EB}}{\Delta I_E} \quad \text{at constant } V_{CB}$$

The value of input resistance R_i in CB configuration is very low. Its value further decreases with the increase in collector-base voltage $V_{CB.}$ The typical value of input resistance varies from a **few ohms to 100 ohms.**

AC Input Resistance in Common Emitter Configuration: The ratio of change in base-emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage (V_{CE}) i.e.,

$$R_i = \frac{\Delta V_{BE}}{\Delta I_B} \text{ at constant } V_{CE}$$

In CE configuration, the typical value of input resistance is of the order of a **few hundred ohms**

AC Output Resistance in Common Base Configuration: The ratio of change in collector-base voltage (ΔV_{CB}) to the resulting change in collector current (ΔI_C) at constant emitter current (I_E). i.e.,

$$R_O = \frac{\Delta V_{CB}}{\Delta I_C} \text{ at constant } I_E$$

The Output Resistance of CB configuration is very high, of the order of **several tens of kilo-ohms (≅ 1 MΩ).**

AC Output Resistance in Common Emitter Configuration: The ratio of change in collector-emitter voltage (ΔV_{CE}) to the change in collector current (ΔI_C) at constant base current I_B, i.e.

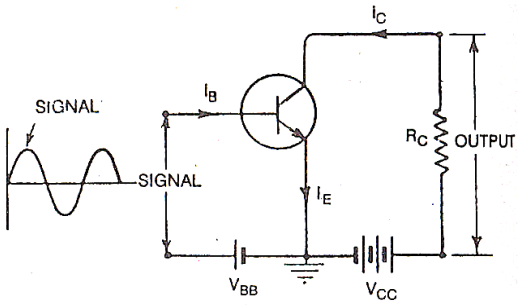
$$R_O = \frac{\Delta V_{CE}}{\Delta I_C} \quad \text{at constant } I_B$$

The output resistance of CE configuration is less than the CB configuration. Its value is of the order of **50 KΩ.**

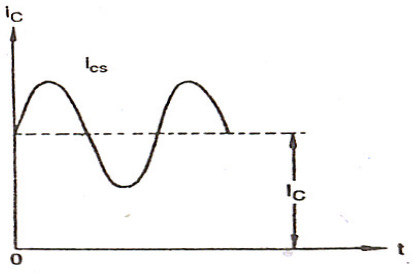
Q.16 Describe the operation of a transistor amplifier in CE configuration. **Marks(4)**

Ans: **Operation of a Transistor Amplifier in CE configuration**: A Common Emitter NPN transistor is shown in fig. 16(a). When a signal is applied in the emitter-base junction, during positive half cycle, the forward bias across this junction increases. This increases the flow of electrons from emitter to collector via base and thus increases the collector current. The increased collector current produces more voltage drop across the collector load resistor R_C. However, during negative half cycle of the signal, the forward bias

voltage across the emitter-base junction decreases. This decreases the collector curr which consequently decreases the voltage drop across the collector load resistor R_C. Hence, an amplified signal appears across the collector load resistor.



npn transistor amplifier circuit



Graph for collector current

Fig. 16(a)

Q.17 **Derive the relation :** $\alpha_{dc} = \dfrac{\beta_{dc}}{1+\beta_{dc}}$ **Marks (4)**

Ans: **Relationship between α and β:** The Beta factor (β) is the current gain factor of a common emitter circuit is defined as the ratio of change in collector current (I_C) to the change in base current (I_B) i.e.,

$$I_C = \beta_{dc} I_B + I_{CO}$$

$$I_C \cong \beta_{dc} I_B \quad \text{assuming } I_{CO} \text{ is very small}$$

or $$\beta_{dc} = \frac{I_C}{I_B}$$

and the alpha factor (α) is also called the current amplification factor and is defined as the ratio of change in collector current (I_C) to the change in emitter current (I_E) i.e.,

$$\alpha_{dc} = \frac{I_C}{I_E} = \frac{1}{1+\dfrac{I_B}{I_C}}$$

$$= \frac{1}{1+\dfrac{1}{\beta_{dc}}} = \frac{\beta_{dc}}{1+\beta_{dc}}$$

Q.18 Discuss the similarities and differences between JFET and MOSFET with regard to their construction and applications. **Marks (7)**

Ans: **Similarities in Construction**

(i) JFET is a three terminal semiconductor device(source, gate and drain) in which current conduction is by majority carriers (electrons or holes), whereas MOSFET is also a three terminal semiconductor device in which current conduction is by majority carriers.

(ii) JFET is Voltage Controllable Device (i.e., the gate terminal is used for controlling the drain current whereas MOSFET is also a Voltage Controllable Device.

Differences in Construction:

(1) An N-channel JFET is shown in fig. 18(a). It consists of a thin N-type silicon bar with two islands of P-type semiconductor material embedded in the sides, thus forming two PN junctions. Whereas in N-channel Depletion MOSFET, there is only one p-region instead of two. This region is known as substrate. The two P-regions are embedded in it as shown in fig. 18(b)

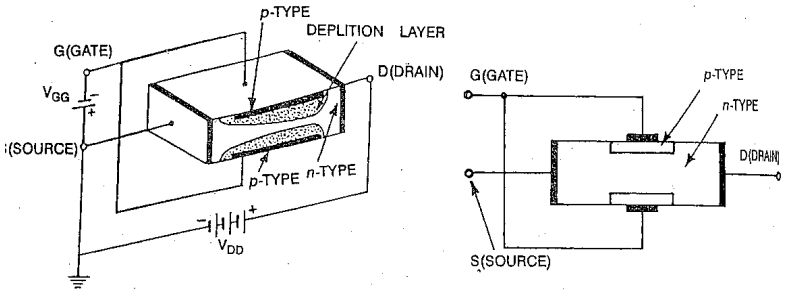


Fig. 18(a)

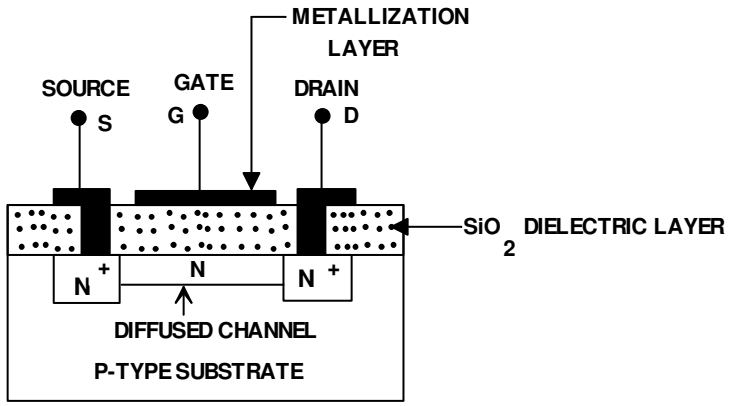


Fig. 18(b) N-CHANNEL DEPLETION MODE STRUCTURE

(2) In N-channel JFET, the two p regions are connected with each other (externally or internally) and are called gate (G). Ohmic contacts are made at the two ends of the N-type semiconductor bar. One terminal known as the source (S) through which the majority carriers (electrons in this case) enter the bar. The other terminal as the drain (D) through which these majority carriers leave the bar. But in MOSFET, over the left side of the channel, a thin layer of metal oxide (usually silicon dioxide) is deposited. A metallic Gate is deposited over the silicon dioxide .The gate is insulated from the semiconductor since silicon dioxide is an insulator. That is why MOSFET is also known as Insulated Gate FET. Like JFET, ohmic contacts are made at the two ends (Drain and Source) of the N-type semiconductor bar.

(3) Since the gate is insulated from the channel by a thin layer of silicon dioxide, the input impedance of MOSFET is very high (of the order of 10^4 to 10^9 MΩ) whereas the input impedance of JFET is 100MΩ as for a reverse biased pn junction.

(4) Unlike the JFET, a MOSFET has no gate diode, it forms a capacitor. The capacitor has gate and channel as electrodes and the oxide layer is dielectric. Because of this property, the device can be operated with negative as well as positive gate voltages.

Applications of JFET:
FET is used as a

(1) Buffer amplifier
(2) Low Noise Amplifier
(3) Cascaded Amplifier
(4) Analog Switch
(5) Chopper
(6) Phase Shift Oscillator circuits
(7) Voltage Variable Resistors in Operational Amplifiers and tone controls etc.,
(8) For Mixer operation on FM and TV receivers

Applications of MOSFET: MOSFETs can also be used for most applications where JFET is used. MOSFETs have become very popular for digital logic circuits due to high density of fabrication and low power dissipation.

(1) MOSFET is used in Sample and Hold circuit as a switch.
(2) P-MOSFET and N-MOSFET are used in digital logic circuits
(3) C-MOSFET is very popular in fabricating of MSI and LSI technology.

Q.19 Draw a single stage amplifier circuit using JFET and explain the purpose of each component Used. **Marks (7)**

Ans: The circuit of a **Single Stage Common Source N-channel JFET** amplifier using self bias is shown in fig. 19(a)

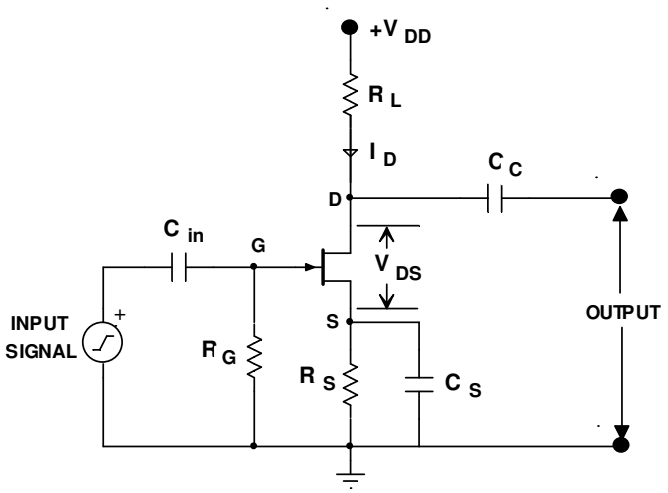


Fig. 19(a)

The purposes of these components are described below:-

Input Capacitor C_{in}: An ac signal is supplied to the gate of the FET through an electrolytic capacitor called input capacitor C_{in}. This capacitor allows only ac signal enter the gate but isolates the signal source from R_G. If this capacitor is not used, the signal source resistance will come across the resistor R_G and thus changing the biasing conditions.

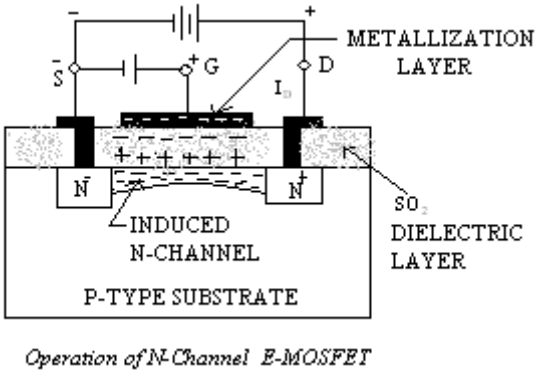
Biasing Network (R_s and C_s): The JFET is self-biased by using the biasing network R_s-C_s. The desired bias voltage is obtained when d.c. component of drain current flows through the source-biasing resistor Rs. Whereas, the capacitor C_s bypasses the a.c. component of drain current.

Resistor R_G: Resistor R_G provides d.c. path for reverse-biasing of gate-source junction

Coupling Capacitor (C_c): It is an electrolytic capacitor used to couple one stage amplification to the next stage or load. It allows only amplified ac signal to pass to the other side but blocks the dc voltage. If this capacitor is not used, the biasing conditions of the next stage will be drastically changed due to the shunting effect of R_d.

Q.20 Explain the principle of operation of any one type of MOSFET. **Marks (6)**

Ans: **Operating Principle of N-channel Enhancement MOSFET:** Operating principle of N-channel Enhancement MOSFET is shown in fig. 9(a). When drain is applied with positive voltage with respect to source and no potential is applied to the gate, two N-regions and one P-substrate form P-N junctions connected back to back with a resistance of the P-substrate. So a very small drain current i.e., a reverse leakage current flows. If the P-type substrate is now connected to the source terminal, there is zero voltage across the source substrate junction, and the drain-substrate junction remains reverse biased.



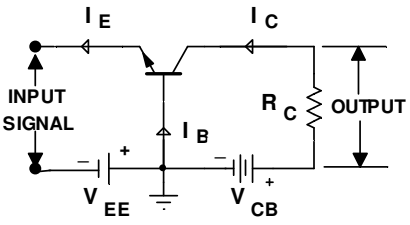
Operation of N-Channel E-MOSFET

Fig. 9(a)

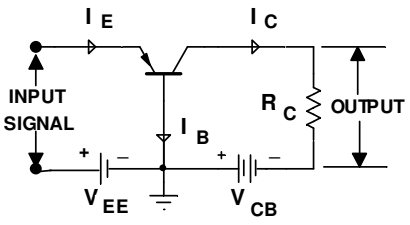
When the gate is made positive with respect to the source and the substrate, negative (i.e. minority) charge carriers within the substrate are attracted to the positive gate and accumulate close to the surface of the substrate. As the gate voltage is increased, more and more electrons accumulate under the gate. Since these electrons cannot flow across the insulated layer of silicon dioxide to the gate, so they accumulate at the surface of the substrate just below the gate. These accumulated minority charge carriers make N-type channel stretching from drain to source. When this occurs, a channel is induced by forming what is termed an inversion layer (n-type). The n-type drain and gate are now connected by the n-type channel and the current can flow from drain to source.

Q.21 Draw the three configurations in which a transistor may be connected showing battery Connections for each. **Marks (4)**

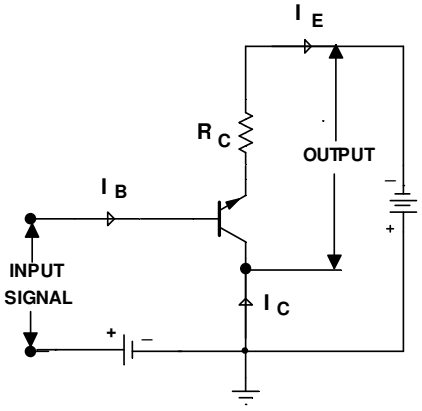
Ans: **Three Configurations (CB, CC, CE) :**



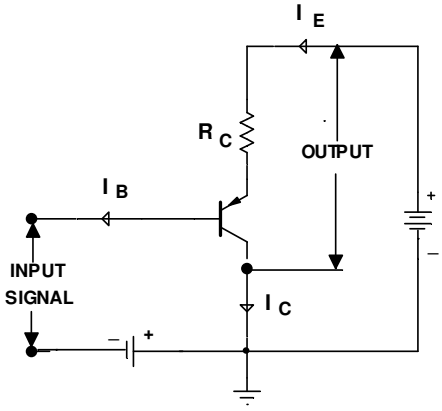
Common Base circuit of npn transistor



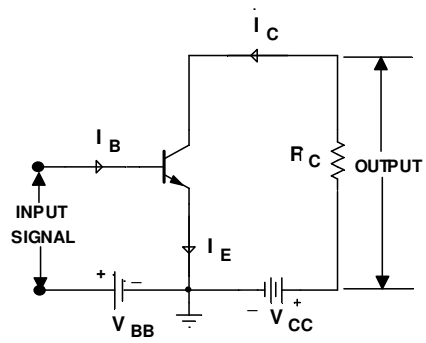
Common Base circuit of pnp transistor



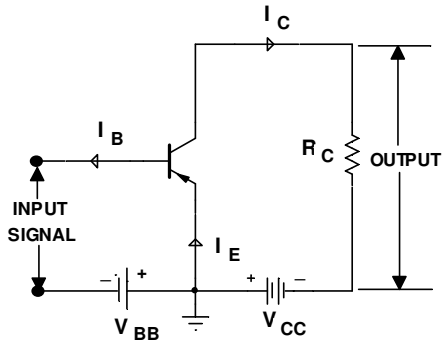
Common collector circuit of npn transistor



Common collector circuit of pnp transistor



Common emitter circuit of npn transistor



Common emitter circuit of pnp transistor

Q.22 What are the advantages of ICs over conventional circuits? **Marks (4)**

Ans: **Advantages of Integrated Circuits (ICs) over conventional circuits:**

(1) Extremely small size- thousand times smaller than discrete circuit.
(2) Very small weight owing to miniaturized circuit.
(3) Very low cost because of simultaneous production of hundred of similar circuits on a small semiconductor wafer.
(4) More reliable because of elimination of soldered joints and need for fewer inter-connections.
(5) Low power consumption because of their smaller size.
(6) Easy replacement as it is more economical to replace them than to repair them
(7) Increased operating speeds because of parasitic capacitance effect.
(8) Improved functional performance as more complex circuits can be fabricated for achieving better characteristics.
(9) Suitable for small signal operation.

Q.23 What are different characteristics of an ideal operational amplifier? **Marks (4)**

Ans: **Characteristics of an ideal Operational Amplifier:**

(1) Infinite voltage gain A

(2) Infinite input resistance R_i so that almost any signal source can drive it and the is no loading of the preceding stage.
(3) Zero output resistance R_o, so that output can drive an infinite number of other devices.
(4) Zero output voltage when input voltage is zero.
(5) Infinite bandwidth so that any frequency signals from 0 to ∝ HZ can be amplified without attenuation.
(6) Infinite common-mode rejection ratio, so that the output common-mode noise voltage is zero.
(7) Infinite slew rate so that output voltage changes occur simultaneously with input voltage changes.

Q.24 Explain the significance of virtual ground in an operational amplifier? **Marks (4)**

Ans: **Significance of Virtual Ground:** Fig. 24(a) shows the circuit diagram of basic Inverting Amplifier. In this figure, the non-inverting terminal is grounded, and the input signal is applied to the inverting terminal via resistor R_1. However, the difference input voltage is ideally zero: that is, the voltage at the inverting terminal (v_2) is approximately equal to that at the non-inverting terminal (v_1).
In other words, the inverting terminal voltage v_2 is approximately at ground potential. Therefore, the inverting terminal is said to be at Virtual Ground. This concept is extremely useful in the analysis of closed loop Op-amp circuits.

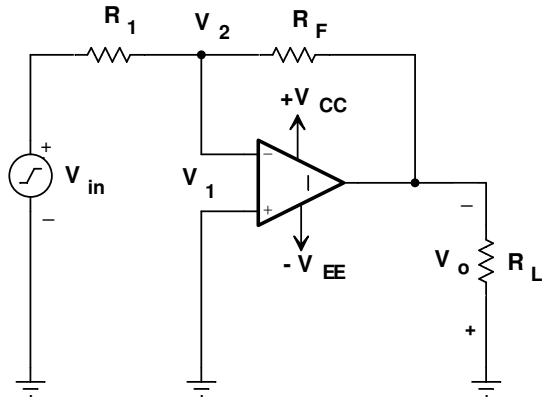


Fig.24(a) Inverting Amplifier with Feedback

Q.25 How do you use operational amplifier as differentiator and adder/subtractor. **Marks (6)**

Ans: Fig. 25(a) shows the **differentiator or differentiation amplifier**. As its name implies, the circuit performs the mathematical operation of differentiation; that is, the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier, if an input resistor R_1 is replaced by a capacitor C_1.
The expression for the output voltage can be obtained from Kirchoff's current equation written at node v_2 as follows:

$i_C = i_B + i_F$
Since $I_B \cong 0$,
$I_C = i_F$

$$C_1 \frac{d}{dt}(V_{in} - V_2) = \frac{V_2 - V_o}{R_F}$$

But $v_1 = v_2 \cong 0$ V, because A is very large. Therefore,

$$C_1 \frac{dV_{in}}{dt} = -\frac{V_o}{R_F}$$

$$V_o = -R_F C_1 \frac{dV_{in}}{dt}$$

Thus the output v_o is equal to the R_F C_1 times the negative instantaneous rate of change of the input voltage v_{in} with time.

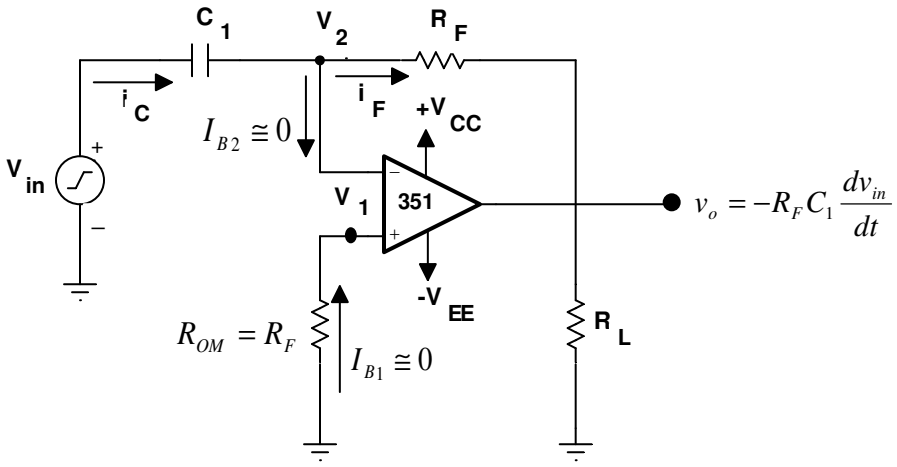


Fig. 25(a) Op-amp as Differentiator

Inverting Summing Amplifier: Fig.25(b) shows the **inverting summing amplifier**. It is a inverting configuration with three inputs V_a, V_b and V_c. Depending on the relationship between the feedback resistor R_F and the input resistors R_a, R_b, and R_c, the circuit can be used as a summing amplifier.

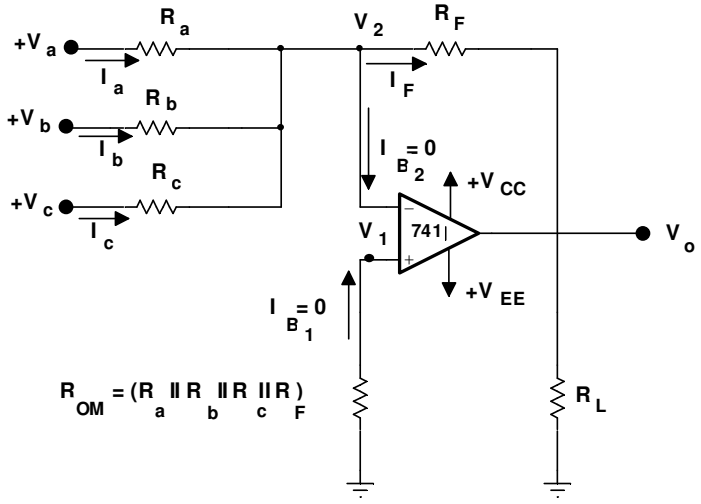


Fig. 25(b) Op-amp as Summing Amplifier

The circuit's function can be verified by examining the expression for the output voltage V_o, which is obtained from Kirchoff's current equation written at node V_2. Referring to the fig. 25(b)

$$I_a + I_b + I_c = I_B + I_F$$

Since R_i and A of the op-amp are ideally infinity, $I_B = 0$ A and $V_1 = V_2 \cong 0$ V

$$\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_C} = \frac{V_o}{R_F}$$

$$V_o = -R_F \frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_C}$$

If in the circuit 25(b), $R_a = R_b = R_c = R$, for example then the above equation can be written as

$$V_o = - (V_a + V_b + V_c)$$

This means that the output voltage is equal to the negative sum of all the inputs times the gain of the circuit R_F/R; hence the circuit is called a summing amplifier, Obviously, when the gain of the circuit is 1, that is $R_a = R_b = R_c = R_F$, the output voltage is equal to the negative sum of all input voltages. Thus

$$V_o = -(V_a + V_b + V_c)$$

Op-amp as a Subtractor: A basic differential amplifier can be used as a subtractor as shown in fig. 25(c) In this figure, all external resistors are equal in value, so the gain of the amplifier is equal to 1.

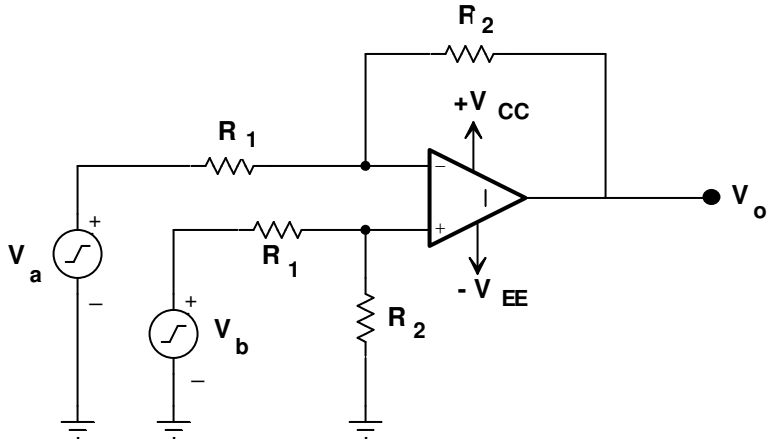


Fig.25 (c) Op-amp as Subtractor

From the figure.25(c), the output voltage of the differential amplifier with a gain of 1 is

$$V_O = V_a\left(\frac{-R_2}{R_1}\right) + V_b\left(\frac{R_2}{R_1 + R_2}\right)\left(1 + \frac{R_2}{R_1}\right)$$

$$\text{or } V_o = -\frac{R_2}{R_1}(V_a - V_b)$$

Thus the output voltage Vo is equal to the voltage applied to the non-inverting terminal V_b minus the voltage V_a applied to the inverting terminal; hence the circuit is called a subtractor.

Q.26 Describe the construction and working of UJT. **Marks (6)**

Ans: **Construction of UJT**: The basic structure of a UJT is shown in fig. 26(a). It consists of an n-type silicon bar, which is lightly doped. Two end connections are taken from the bar called base-one (B_1) and base-two (B_2). A heavily doped p-type region is diffused to n-type nearer to B_2.
This forms a pn junction with the bar as shown in fig.11(a). A lead is connected to p-region called emitter (E). The schematic symbol of UJT is shown in fig. 26(b)

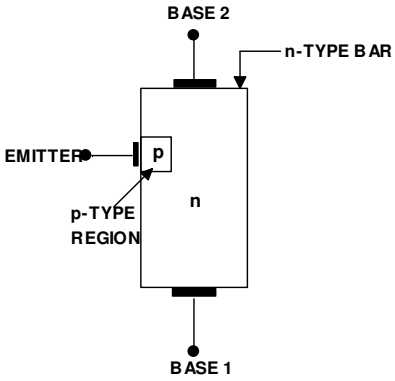


Fig. 26(a)

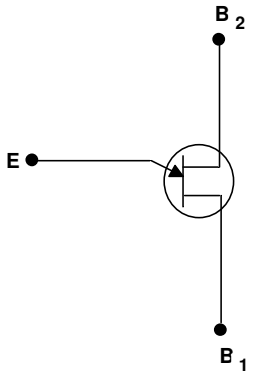


Fig.26(b)

Working: Make the circuit arrangement as shown in fig.26(c), where the UJT is represented by its equivalent circuit consisting of resistances R_{B1}, R_{B2} and a diode D. Normally, B_2 is kept positive with respect to B_1. A variable positive voltage is supplied to the emitter through a switch S.

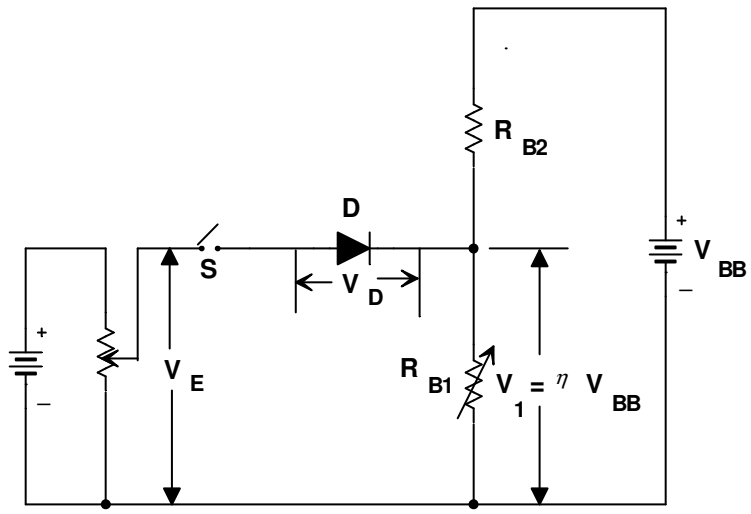


Fig. 26(c)

(i) When the emitter circuit is closed through switch S but the emitter voltage is reduced to zero, and a voltage V_{BB} is applied between the two bases, then a voltage gradient is established along the n-type bar. This sets up a voltage V1 = V_{BB} between emitter

junction and B_1 which is more than half the value of V_{BB} as the value of intrinsic stand-ratio (η) lies between 0.51 to 0.8. This voltage establishes a reverse bias on the pn junction and the emitter current is cut-off.

(ii) When a +ve voltage is applied at the emitter, the pn junctio n will remain reverse biased so long as the input emitter voltage is less than $V_1(=\eta\ V_{BB})$.

If the input voltage applied to the emitter is increased, a stage reaches when it exceeds V_1 by V_D i.e. $V_E = V_1 + V_D$. This will bring the pn junction in forward biased condition. At this stage, p-type material injects holes into the n-type bar. These holes are repelled by positive B_2 terminal and are attracted towards negative B_1 terminal of the bar.

This accumulation of holes in the emitter to B_1 region decreases the resistance of this section (i.e. R_{B1}) of the bar. This results internal voltage drop from emitter to B_1 and consequently increases the emitter current I_E. This process goes on and eventually a condition of saturation is reached. This is a stage where the emitter current is limited by only emitter power. The device is now said to be in the ON state.

(iii) The device can be brought to the OFF state, if a negative pulse is applied to the emitter. Under this condition, the pn junction is reverse biased and the emitter current is cut-off.

Q.27 Define the term intrinsic stand-off ration in UJT. **Marks (4)**

Ans: **Intrinsic Stand-off Ratio:** The equivalent circuit of a UJT is shown in fig.27 (a). The emitter diode forms the junction of two internal resistances R_{B1} and R_{B2} connected in series. Where

R_{B1} = resistance of silicon bar between B_1 and emitter junction.

and R_{B2}= resistance of silicon bar between B_2 and emitter junction.

Here, interbase resistance is given as:

$$R_{BB} = R_{B1} + R_{B2}$$

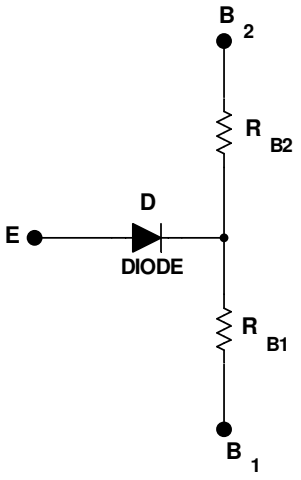


Fig.27(a)

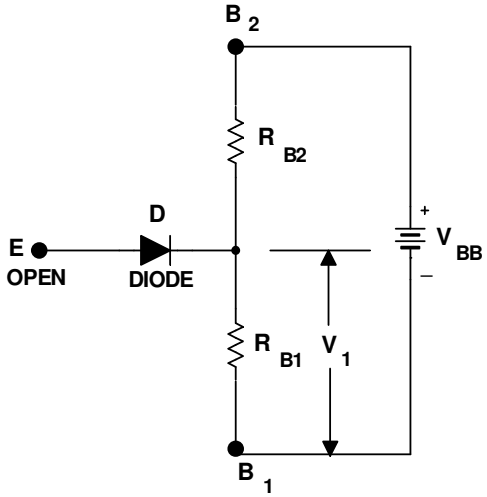


Fig.27(b)

The pn junction is represented as a diode D in the emitter as shown in figure. If a voltage V_{BB} is applied between the bases with emitter open (see fig..27(b), the circuit will behave as a potential divider. Thus, V_{BB} will be divided across R_{B1} and R_{B2} and the voltage across R_{B1} is

$$V_1 = \frac{R_{B1}}{R_{B1} + R_{B2}} \times V_{BB} \qquad \text{(or)}$$

$$\frac{V_1}{V_{BB}} = \frac{R_{B1}}{R_{B1} + R_{B2}}$$

This ratio V_1/V_{BB} is called intrinsic stand-off ratio and is represented by Greek letter η (eta).

hence,

$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}} = \frac{R_{B1}}{R_{BB}}$$

The typical range of η is from 0.51 to 0.8.

Q.28 Draw and discuss the static emitter characteristics of UJT. **Marks (4)**

Ans: **The static emitter characteristics of a UJT** is shown in fig. 28(a)

(i) When V_E is zero and a given voltage V_{BB} is applied across the bases i.e., B_2 and B_1, the emitter junction is reverse biased and the UJT is in the cut-off region. A slight leakage current flows from terminal B_2 to emitter due to minority carriers. This current is just a reverse current as it is shown in the figure. 28(a)

(ii) As emitter voltage V_E increases from zero, only leakage (reverse) current flows upto a certain value of V_E.

(iii) Above a certain value of V_E, forward emitter current I_E begins to flow. This increase in voltage and current goes on until peak point P is achieved where voltage and current are V_P (peak voltage) and I_P (peak current).

$V_P = V_1 + V_D = \eta V_{BB} + V_D = \eta V_{BB} + 0.7$ (since for Si, $V_D = 0.7V$)

(iv) After the peak point P, an attempt to increase V_E is followed by a sudden rise in emitter current I_E with a corresponding fall in V_E. This shows the negative resistance behaviour of the device.

(v) This behaviour of the device continues until the valley point V is achieved. At this point, the emitter voltage is called valley-point voltage V_V and the emitter current is called valley-point current I_V.

(vi) The region between peak point and valley point is called negative resistance region.

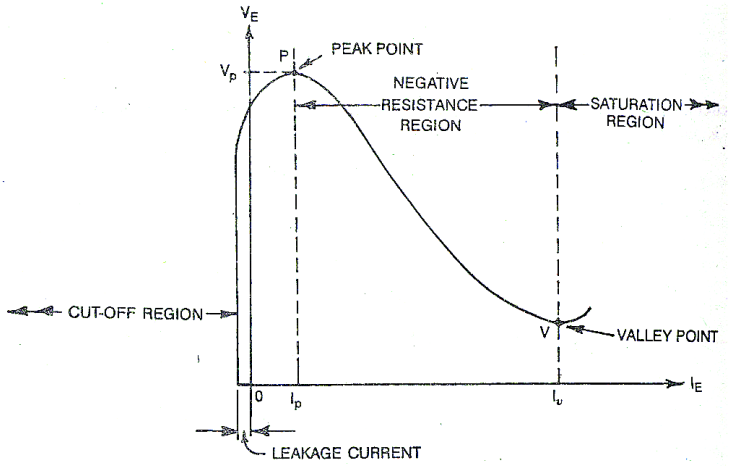


Fig. 28(a)

Q.29 Explain the constructional details and various types of thermistors **Marks (**

Ans: **Construction Details of Thermistors:** Silicon and germanium are not normally used for manufacturing thermistors, because larger and more predictable temperature coefficients are available with metal oxides. Modern thermistors are manufactured from the oxides of metals like manganese, nickel, cobalt, copper, iron, zinc, aluminium, titanium, magnesium and uranium. These oxides or their sulphides and silicates are milled, mixed in appropriate proportion, pressed into desired shape with appropriate binders and finally sintered. The electrical terminals are embedded before sintering or baked afterwards. The resistance of the thermistors at room temperature of 25˚C varies over a wide range, from several hundred ohms to mega ohms. Because of their high resistance they can be manufactured in very small sizes in the form of beads, discs and rods.

Various types of Thermistors are shown in fig. 29:

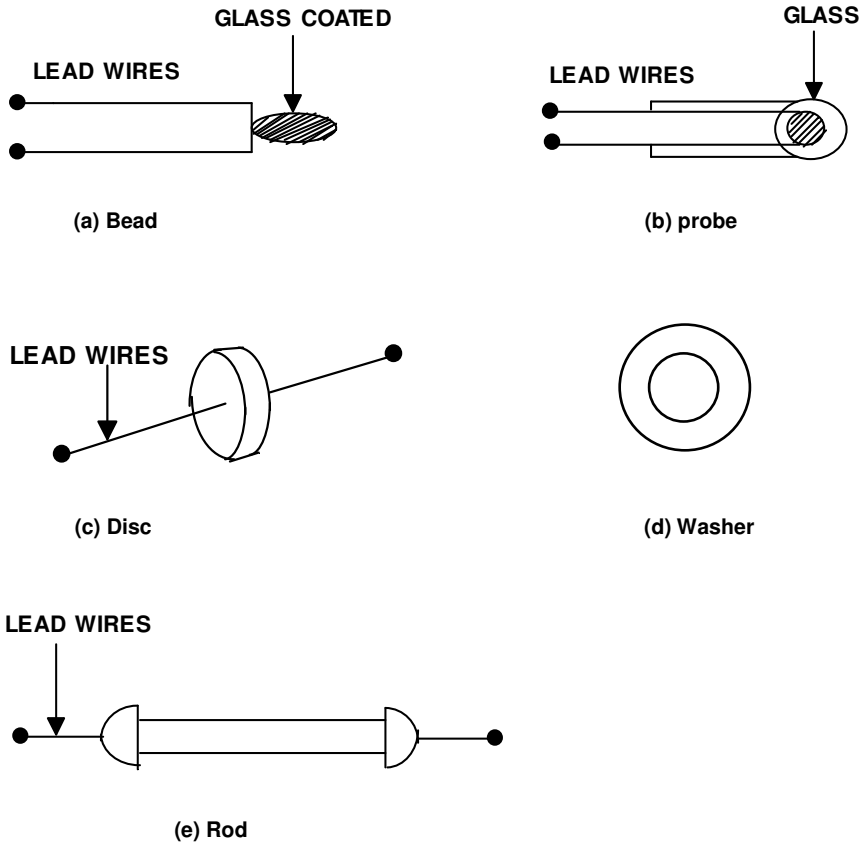


Fig. 29 Commercial Forms of Thermistors

Q.30 Draw the characteristics of both NTC and PTC thermistors and explain their salient features and one use of each. **Marks (6)**

Ans: **Characteristics of NTC and PTC Thermistors:** Characteristics of NTC thermistors and PTC thermistors is shown in fig.30(a) and fig.30(b)

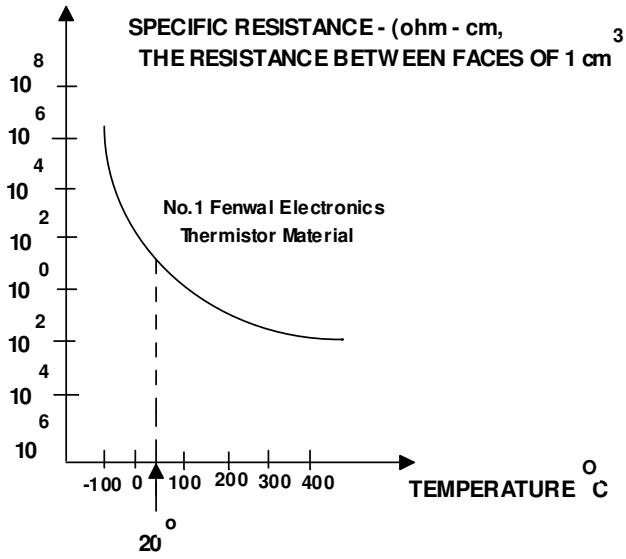


Fig.30(a)Characteristic of NTC thermistor

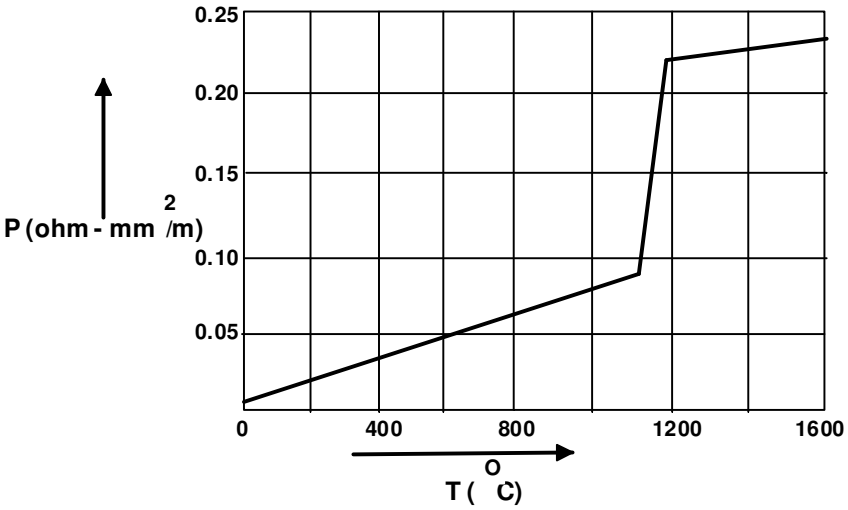


Fig.30(b) Characteristic of PTC thermistor

Features of NTC thermistors:

- An NTC thermistor has a smooth negative-resistance characteristics extending over a wide temperature range.
- They are semiconductors of ceramic materials.
- They are available in various configurations like beads, glass probes, discs, washers, etc.,
- The beads are available in sizes varying from 2.5 mm to 0.2 mm diameter.
- Beads have small size, high precision and stability
- Glass probes are easily mounted on PCB. Dimensions (standard) of discs are from 2.5 mm to 25 mm in dia, and 0.35 mm to 5 mm in thickness.
- Washers have a hole in the center so that they can be mounted on bolt and standard size is 16 mm in diameter.

- Washers may be connected either in series or in parallel.
- The washers have high power dissipating capabilities.

Uses: They are used as temperature sensors or temperature compensating devices in the fields of medical electronics and other industries.

Features of PTC thermistors:

- A PTC thermistor has a positive-resistance characteristics extending over a narrow temperature range.
- They are manufactured from doped polycrystalline and semi conducting barium titanate. Powdered mixture is raised to approx. 1200 degrees C from which pellets are made by pressing.
- PTC thermistors have a very narrow temperature range over which they can be used.
- As the temperature is raised, the resistivity of PTC thermistor increases abruptly above a certain critical temperature called the Curie temperature.

Uses: They are used for measurement and control of temperature, liquid level and gas flow etc.

Q.31 Explain how a Zener diode can be used as voltage regulator. Marks (8)

Ans: **Zener diode as a Voltage Regulator:** It provides a constant voltage to the load from a source whose voltage may vary over sufficient range. Fig.31(a) shows the circuit arrangement. The zener diode of zener voltage V_z is reverse connected across the load R_L across which constant voltage ($V_o = V_z$) is desired. A resistor R is connected in series with the circuit which absorbs the input voltage fluctuations so as to maintain constant voltage (V_o) across the load. Let a variable voltage V_{in} be applied to the regulator. When the value of V_{in} is less than Zener voltage V_z of the zener diode, no current flows through it and the same voltage appears across the load. When the input voltage V_{in} is more than V_Z, this will cause the Zener diode to conduct a large current I_Z.

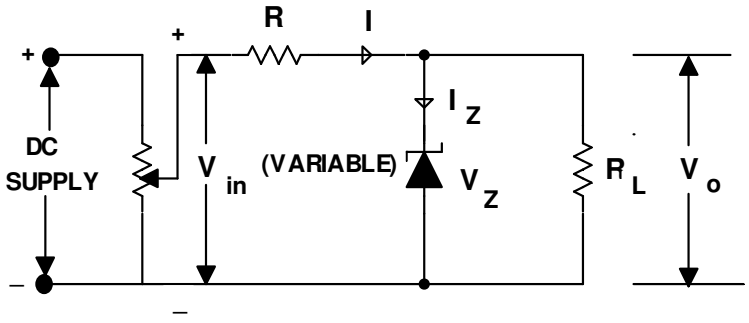


Fig. 31(a)

Consequently, more current flows through series resistor R which increases the voltage drop across it. Thus, the input voltage excess of V_z (i.e. $V_{in} - V_z$) is absorbed by the series resistor. Hence a constant voltage V_0 (=V_z) is maintained across the load R_L. When the load resistance R_L decreases for constant input voltage V_{in}, load current I_L increases. This additional current is not supplied from the source of supply but the demand of additional load current is met by decrease in Zener current Iz.

This keeps the voltage drop across series resistance R constant and also the output voltage V_{out}. The diode current I_z attains its maximum I_{zmax} when load current I_L becomes zero. Thus the value of series resistor R can be determined from the equation

$$R = \frac{V_{in} - V_{out}}{I_{z\max}}$$

Q.32 Draw the circuits to obtain the input and output characteristics of an NPN transistor in CE configuration. Marks (10)

Ans: **Characteristics of NPN Transistor in Common-Emitter configuration:** To determine the characteristics of a NPN transistor in CE configuration, the circuit arrangement as shown in fig. 32(a)

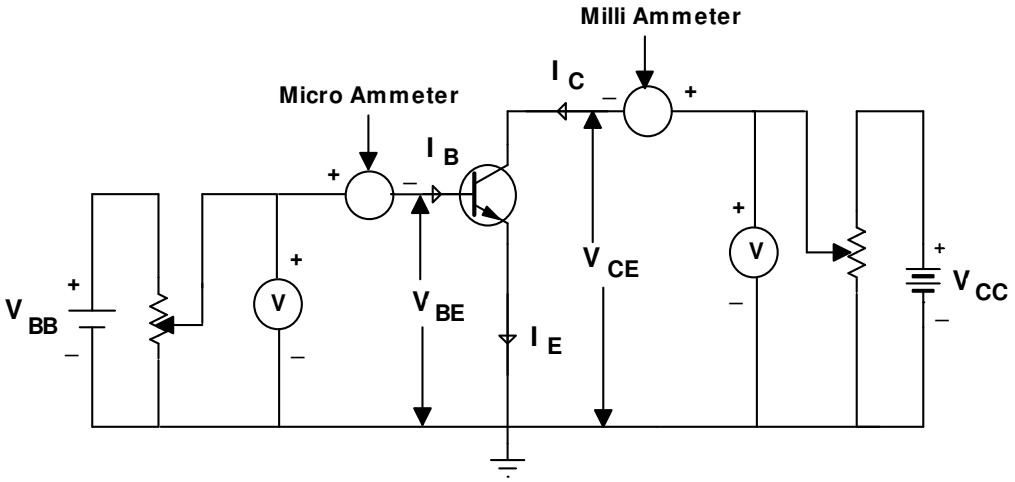


Fig. 32(a)

Input Characteristics: In CE configuration, the curve plotted between base current I_B and base-emitter voltage V_{BE} at constant collector-emitter voltage V_{CE} is called Input Characteristics.

To draw the input characteristic, note down the readings of Ammeter (I_B) connected in the base circuit for various values of V_{BE} at constant V_{CE}. Plot the curve on the graph taking I_B along y-axis and V_{BE} along x-axis as shown in fig.32(b) The following points are noted from these characteristics:

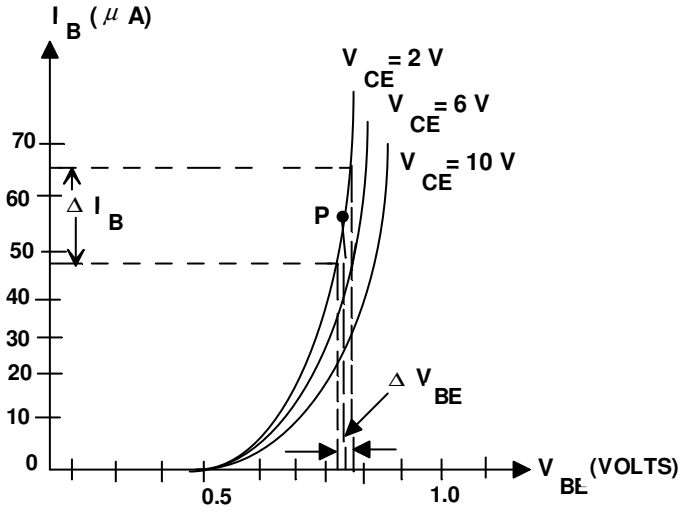
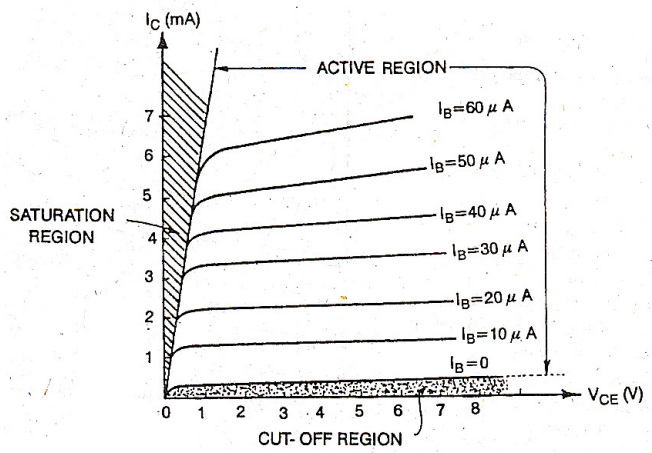


Fig.32(b)

(i) These curves are similar like a forward diode characteristics. I_B increases le rapidly with increase in $V_{BE.}$

(ii)The change in V_{CE} does not result in a large deviation of the curves and hence, the effect of change in V_{CE} on the input characteristic is ignored for all practical purposes.

Output Characteristics: In CE configuration, the curve plotted between collector current I_C and collector-emitter voltage V_{CE} at constant base current I_B is called output characteristic.



(i) In the active region, Ic increases slightly as V_{CE} increases. The slope of the curve is little bit more than the characteristics of CB configuration. Hence, the output resistance (r_o) of this configuration is less compared to CB configuration.

(ii)Since the value of Ic increases with the increase in V_{CE} at constant I_B, the value of β also increases since $\beta = I_C/I_B$

(iii) When V_{CE} falls below the value of V_{BE} (i.e. below a few tenths of a volt.), I_{ce} decreases rapidly. In fact, at this stage, the collector-base junction is also forward biased and the transistor works in the saturation region. In the saturation region, Ic becomes independent and it does not depend upon the input current I_B.

(iv) In the active region, $I_C = \beta I_B$. Hence, a small change in base-current I_B produces a large change in output current (I_C)

(v) When input current $I_B = 0$, the collector current I_C is not zero but its value is equal to the reverse leakage current I_{CEO} (i.e. collector emitter current when base is open).

Q.33 Mention the applications of CE, CB and CC configurations of BJT's Marks(4)

Ans: **Applications of CE configuration of BJT:**

(i) CE amplifier is used in audio frequency applications like Radio receivers, Tape recorders, TV receivers, FM receivers, etc.
(ii) CE amplifier is used in Oscillators.

Applications of CB configuration of BJT:

(i) To provide Voltage gain without Current gain: CB amplifier
provides voltage gain without increasing the value of ciruit current gain
(ii) For impedance matching in High Frequency Applications: It matches the low impedance source and high impedance load in order to have a maximum power transfer between source &load

Applications of CC configuration of BJT:

(i) To provide current amplification with no voltage gain: In digital Electronics, where an increase in current is required but no increase in voltage is needed. In such situation CC configuration can be used.

(ii) Impedance Matching: It matches the high impedance source and low impedance load in order to have a maximum transfer between source and load.

Q.34 Differentiate between FET and BJT transistors. Marks (4)

Ans **Differences between FET and BJT Transistors:**

(i) FET operation depends upon the flow of majority carriers only, it is therefore, a uni-polar (current conduction is due to one type of carriers either electrons or holes) device. On the other hand, the current conduction in BJT is due to both majority and minority carriers, it is therefore a bipolar device.

(ii) FET has high input impedance (of the order of 100 Megaohms), because its input circuit (gate to source) is reverse biased, and so permits high degree of isolation between the input and output circuits. On the other hand, BJT has low input impedance, because its input circuit is forward biased.

(iii) FET carries very small current because of reverse biased gate and input voltage controls the output current. This is the reason that FET is essentially a voltage driven device. BJT carries high current because of forward biased and it is a current operated device, since input current controls the output current.

(iv) BJT uses a current into its base for controlling a large current between collector and emitter whereas in a FET, voltage on the gate terminal is used for controlling the drain current (current between drain and source. Thus an ordinary transistor, gain is characterized by current gain whereas the FET gain is characterized as the transconductance.

(v) FET has no junction like BJT and the conduction is through bulk material current carriers (N-type or P-type semiconductor material) that do not cross junctions. Hence the inherent noise of BJT (owing to junction transitions) is not present in FET

(vi) FET has small gain-bandwidth product, low voltage gain in comparision to BJT.

Q.35 Explain the constructional features, principle of operation and characteristics of N-channel JFET. Marks (10)

Ans: **Constructional Features of N- Channel JFET:** In a N-channel JFET, an N-type silicon bar referred to as the channel, has two smaller pieces of P-type silicon material diffused on the opposite sides of its middle part, forming P-N junctions, as illustrated in fig.35.1

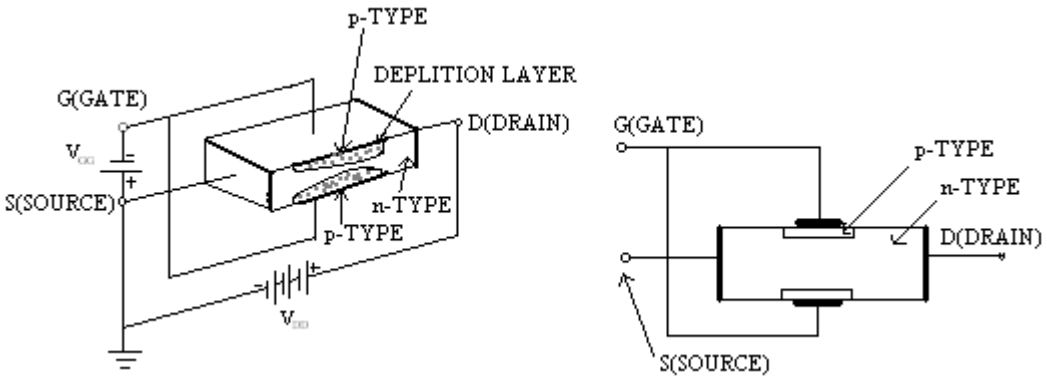


Fig. 35.1

The two P-N junctions forming diodes or gates are connected internally and a comm terminal, called the gate terminal is brought out. Ohmic contacts (direct electrical connections) are made at the two ends of the channel – one lead is called the source terminal (S) through which the majority carriers (electrons) enter the bar and the other drain terminal (D) through which the majority carriers leave the bar which is shown in fig. 35(b)

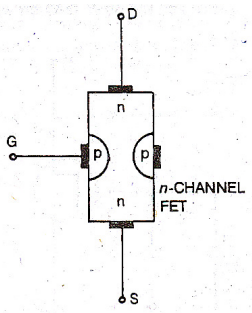


Fig. 35.2

Principle of Operation of N-Channel JFET:

The circuit diagram of an N-channel JFET with normal polarities is shown in fig.35.3

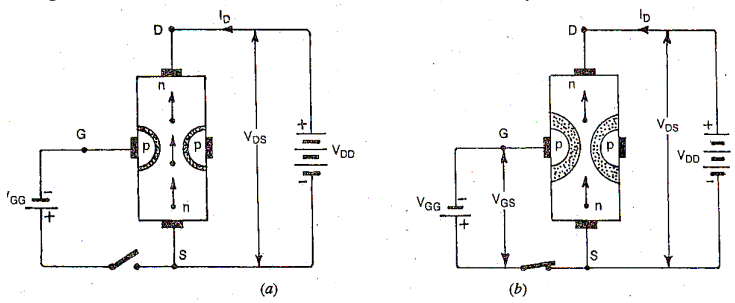


Fig. 35.3

When a voltage V_{DS} is applied across the drain and source terminals and voltage applied across the gate and source V_{GS} is zero (i.e. gate circuit is open) as shown in above fig.3 5.3(a), the two PN junctions establish a very thin depletion layer. Thus a large amount of electrons will flow from source to drain through a wide channel formed between the two depletion layers. When a reverse voltage V_{GS} is applied across the gate and source as shown in above fig. 35.3(b), the width of the depletion layer is increased. This reduces the width of the conducting channel thereby decreasing the conduction (flow of electrons) through it. Thus the current flowing from source to drain depends upon the width of the conducting channel which depends upon the thickness of depletion layer. The thickness of depletion layer established by the two PN junctions depends upon the voltage applied across the gate-source terminal. Hence, it is clear that the current from source to drain can be controlled by the application of potential (i.e. electric field) on the gate. That is why, the device is called Field Effect Transistor.

Characteristics of N-Channel JFET: A curve drawn between drain current (I_D) and drain-source voltage (V_{DS}) of a JFET at constant gate-source voltage (V_{GS}) is known as output characteristics of the JFET are shown in below fig.35.4

(i) At the initial stage, the drain current I_D increases rapidly with the increase in drain source voltage V_{DS} but then becomes almost constant. This voltage is called pinch-off voltage.

(ii) After pinch off voltage, the depletion layers almost touch each other and the conduction channel becomes very narrow. Therefore, the increase in drain current I_D is very small with the increase in drain-source voltage V_{DS}. Thus, the drain current almost becomes constant.

(iv) Further increase in drain-source voltage V_{DS} eventually causes the avalanc breakdown across the reverse-biased gate junction and the current I_D shoots to a very high value.

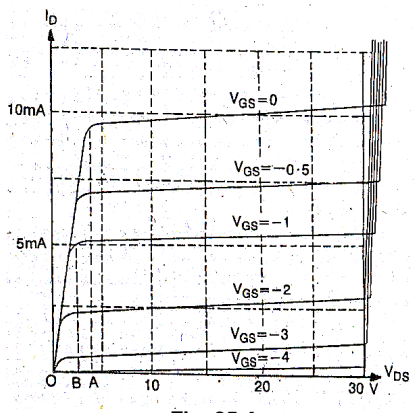


Fig. 35.4

Q.36 Write short notes on any Two of the following: **Marks (2 X 7 =14)**

(i) Operation of a Uni junction Transistor (UJT) and its uses.
(ii) FET used as a switch and its limitations.
(iii) Differential amplifier. Explain also CMRR.

Ans: **UJT:** A uni-junction transistor(UJT) is a three terminal semiconductor device having two doped regions. In the three terminals, it has emitter (E) and two bases ($B_1$and B_2). This device has only one pn junction, therefore, naming it a 'transistor' is really misnomer. However, from the outer look (packages), it resembles to a bipolar transistor and hence the name uni-junction transistor. This device has a unique characteristic that when it is triggered, the emitter current increases regeneratively until it is limited by the emitter power supply.

Construction: The Structure and symbol of UJT are shown in fig. 36.1(a) UJT consists of an n-type silicon bar which is lightly doped. Two ends connections are taken from the bar called base-one (B_1)and base-two (B_2). A heavily doped p-type region is diffused to n-type bar nearer to B_2.

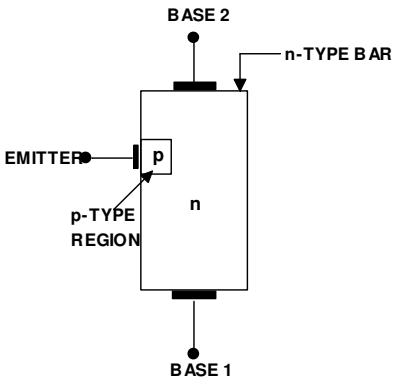


Fig. 36.1(a)

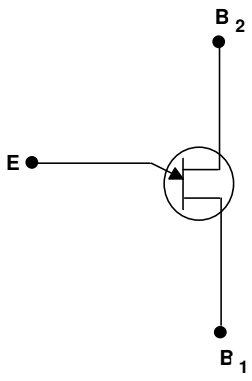


Fig.36.1(b)

Working: Make the circuit arrangement as shown in fig. 36.1(b) Normally, B_2 is kept positive w.r.t B_1. A variable positive voltage is supplied to the emitter through a switch
(i)When the emitter circuit is closed through a switch S but the emitter voltage is reduced to zero. This voltage establishes a reverse bias on the pn junction and the emitter current is cut-off.
(ii) When a +ve voltage is applied at the emitter, the p-n junction will remain reverse biased so long as the input emitter voltage is less than V_1 (=η VBB). If the input voltage applied to the emitter is increased, a stage reaches when it exceeds V_1 by V_D i.e. $V_E = V_1 + V_D$. This will bring the p-n junction in forward biased condition.
At this stage, p-type material injects holes into the n-type bar. These holes are repelled by positive B_2 terminal and are attracted towards negative B_1 terminal of the bar. This accumulation of holes in the emitter to B_1 region decreases and the resistance of this section (i.e. R_{B1}) of the bar. This results internal voltage drop from emitter to B_1 and consequently increases the emitter current I_E. This process goes on and eventually a condition of saturation is reached. This is a stage where the emitter current is limited by only emitter power. The device is now said to be in the ON state.

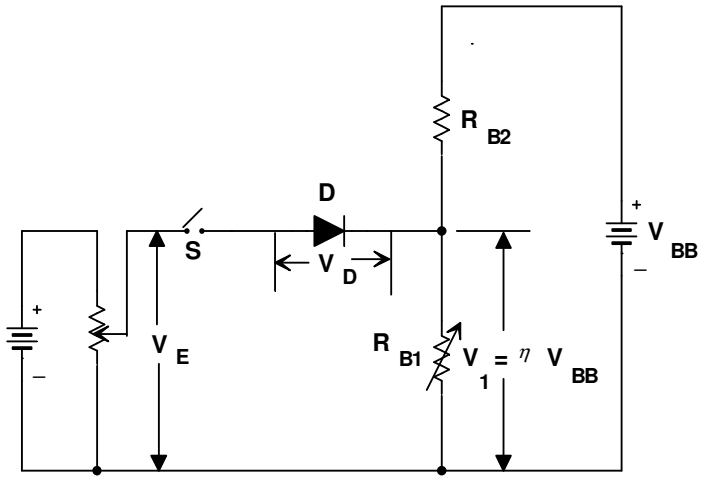


Fig. 36.2

Applications of UJT:
(i)Relaxation Oscillator
(ii)Pulse generators
(iii)Saw-tooth generators
(iv)Triggering circuits
(v)Phase control
(vi)Timing circuits.

Q.36(ii) **FET as a switch**: The circuit diagram of an N-channel FET with normal polarities is shown in fig. 36.3

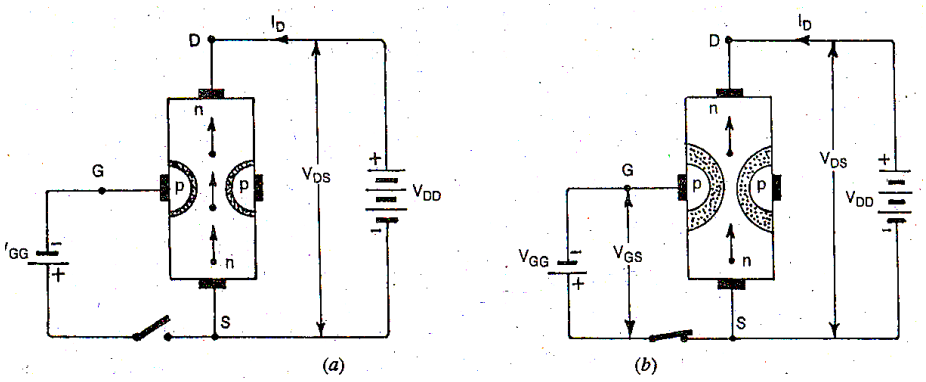


Fig. 36.3

When a voltage V_{DS} is applied across the drain and source terminals and voltage applied across the gate and source V_{GS} is zero (i.e. gate circuit is open) as shown in above fig. 36.3(a), the two PN junctions establish a very thin depletion layer. Thus a large amount of electrons will flow from source to drain through a wide channel formed between the two depletion layers. In this condition, FET acts like a closed switch.

When a reverse voltage V_{GS} is applied across the gate and source as shown in above fig.36.3(b), the width of the depletion layer is increased. This reduces the width of the conducting channel thereby decreasing the conduction (flow of electrons) through it. In this condition, FET acts like an open switch. Thus the current flowing from source to drain depends upon the width of the conducting channel which depends upon the thickness of depletion layer. The thickness of depletion layer established by the two PN junctions depends upon the voltage applied across the gate-source terminal.

Limitation of FET:

(i) It has relative small gain-bandwidth product
(ii) Greater susceptibility to damage in its handling.
(iii) It has low voltage gain, because of small tansconductance

Q36.(iii) Fig.36.4 shows the open-loop differential amplifier in which input signal V_{in1} and V_{in2} are applied to the positive and negative input terminals. Since the op-amp amplifies the difference between the two input signals, this configuration is called the differential amplifier.

Op-amp is a versatile device because it amplifies both ac and dc input signals. This means that V_{in1} and V_{in2} could be either ac or dc voltages. The source resistances R_{in1} and R_{in2} are normally negligible compared to the input resistance R_i. Therefore, the voltage drops across these resistors can be assumed to be zero, which then implies that $V_1 = V_{in1}$ and $V_2 = V_{in2}$, then the output voltage is given by

$$V_o = A\,(V_{in1} - V_{in2})$$

Thus, the output voltage is equal to the voltage gain A times the difference between the two input voltages. Also, the polarity of the output voltage is dependent on the polarity of the input difference voltages ($V_{in1} - V_{in2}$). In open-loop configurations, gain A is commonly referred to as Open-loop Gain.

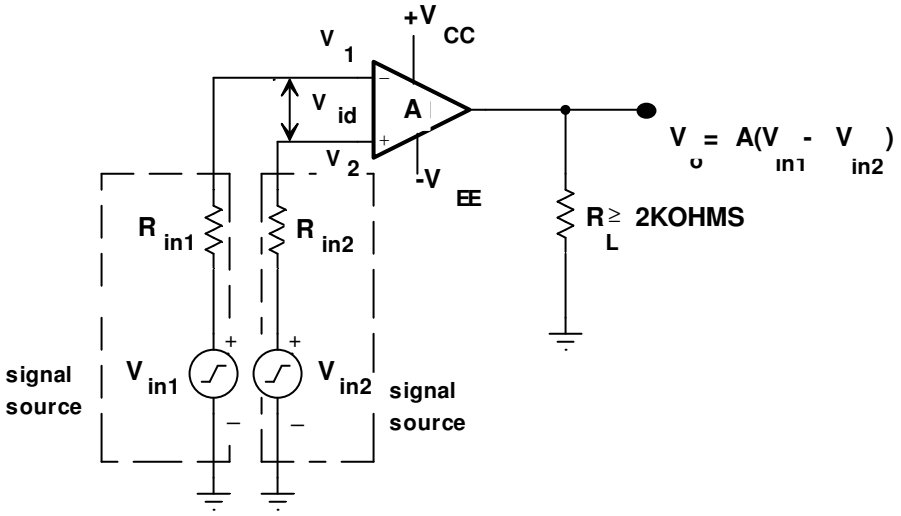


Fig. 36.4

CMRR: Common-Mode Rejection Ratio (CMRR) is defined as the ability of a differential amplifier to reject common-mode voltages such as electrical noise (or) it is also defined as the ratio of the differential voltage gain A_d to the common-mode voltage gain A_{cm}; that is,

$$CMRR = \frac{A_d}{A_{cm}}$$

The differential voltage gain A_d is the same as the large-signal voltage gain A and the common voltage gain A_{cm} is given by

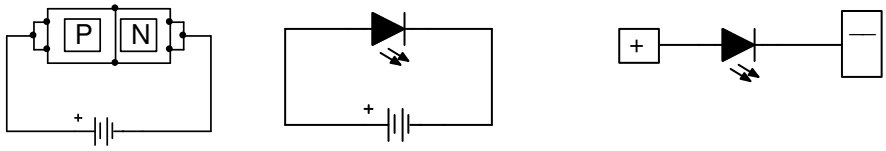
$$A_{cm} = \frac{V_{ocm}}{V_{cm}}$$

Where V_{ocm} = output common-mode voltage
V_{cm} = input common-mode voltage
A_{cm} = common-mode voltage gain

Generally the A_{cm} is very small and $A_d = A$ is very large; therefore, the CMRR is very large. Being a large value, CMRR is most often expressed in decibels (dB). The higher the value of CMRR, the better is the matching between two input terminals and the smaller is the output common-mode voltage.

Q.37 Explain the principle of operation of LED and mention the materials used for it.
Marks (7)

Ans: **Principle of operation of LED:** The operation of Light Emitting Diode (LED) is based on the phenomenon of electro-luminance, which is the emission of light from semiconductor under the influence of an electric field.



Structure **Schematic Diagram** **Schematic Symbol**
Fig. 37.1

When a P-N junction diode is forward biased, as shown in fig. 37.1, the potential barrier is lowered. The conduction band free electrons from N-region cross the barrier and enter the P-region. As these electrons enter the P-region, they fall into the holes lying in the valence band. Hence they fall from higher energy level to a lower energy level. In the process, they radiate energy. In the ordinary diodes (rectifier and signal diodes), this energy radiates in the form of heat as these diodes are made of silicon or germanium which are opaque materials and block the passage of light.

Materials used for LED's:

(i) GaAs (Gallium Arsenide) emit invisible infra red light
(ii) GaAsP(Gallium Arsenide Phosphide) emit either red or yellow light
(iii) GaP (Gallium Phosphide) emits either red or green light.

So, the above materials radiate energy in the form light (or photons) and hence they glow.

Q.38 Explain the constructional features, operation and characteristics of SCR.
Marks (10)

Ans: **Constructional Features of Silicon Controlled Rectifier (SCR):** An SCR is a pnpn semiconductor device consisting of three pn junctions J_1, J_2, and J_3 as shown in fig. 38.1 and its symbol is shown in fig.38.2. It is as if an ordinary diode (PN) and a transistor (NPN) are combined in one unit. Three terminals are taken; one from the outer P-type material called Anode (A), second from the outer N-type material called Cathode (K) and the third from the other P-type material placed in between and called Gate (G). .

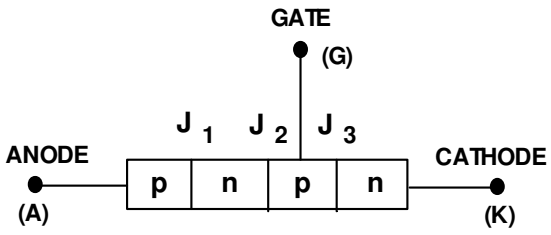


Fig.38.1

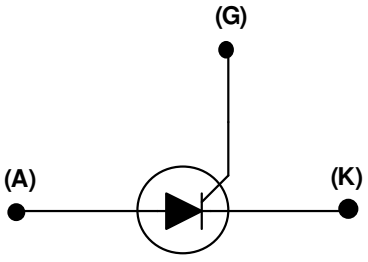


Fig.38.2

Operation of an SCR:

Action of Anode voltage: An SCR circuit shown in fig.38.3 and 38.4, where anode is made positive with respect to cathode and the gate voltage is kept at zero. With the application of this voltage, the junctions J_1 and J_3 are forward biased, whereas junction J_2 is reverse biased. Hence, the flow of current in the circuit is blocked i.e. the SCR is cut off. However, if anode to cathode voltage V is increased, a stage is reached when J2 cannot withstand this high reverse voltage and zener breakdown of junction J_2 occurs and the SCR suddenly switches to highly conducting state. In this state, the load current

is only limited by supply voltage V and load R_L.The maximum anode voltage at wh SCR switches from a non-conducting state to a conducting state without gate voltage is known as Forward Breakover voltage.

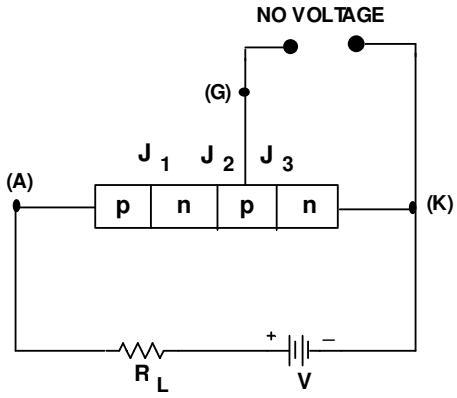


Fig.38.3

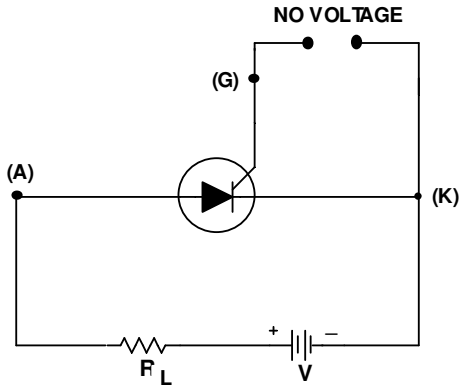


Fig.38.4

If the anode is made negative w.r.t. cathode and the gate voltage is kept at zero, junction J_1 and J_3 are reverse biased, whereas junction J_2 is forward biased. Under such conditions, the SCR does not conduct current i.e. it remains in cut off position. However, if this reverse voltage is increased, a stage reaches when junctions J_1 and J_3 cannot withstand this high reverse voltage and avalanche breakdown occurs in junctions J_1 and J_3 and SCR is turned to highly conducting state.

Action of Gate Voltage: Consider the SCR circuit shown in fig.38.5. When the anode is positive with respect to cathode i.e. when the SCR is in forward mode, the SCR does not conduct unless the forward voltage exceeds certain value, called the forward breakover voltage. In non-conducting state, the current through the SCR is the leakage current which is very small and is negligible. If a positive gate current is supplied, the SCR can become conducting at a voltage much lesser than forward break-over voltage. The larger the gate current, lower the break-over voltage. With sufficiently large gate current, the SCR behaves identical to PN rectifier. Once the SCR is switched on, the forward voltage drop across it suddenly reduced to a very small value, say about 1 volt. In the conducting or on-state, the current through the SCR is limited by the external impedance.

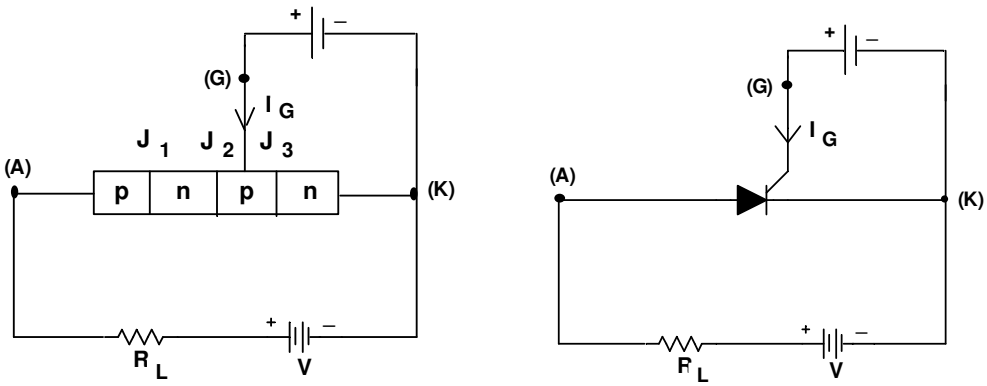


Fig.38.5

V-I Characteristics of an SCR:

Forward Characteristics: The curve between V and I when forward voltage (i.e., anode is positive with respect to cathode) is applied is known as Forward Characteristics of an SCR.

(i) When gate current is zero: As power supply voltage is increased from zero (with zero gate current), there is a small leakage current which flows through anode. This is due to leakage of minority carriers through junction J_2. This small leakage current does not affect the load at all and for all practical purposes, the load is considered to be OFF i.e. SCR is said to be in OFF state.

Now, when the power supply voltage, which is equal to voltage drop across anode and cathode of SCR (as there is little voltage drop across load on account of extremely small value of leakage current), reaches the forward breakover voltage, SCR at once begins to conduct and the voltage V across thyristor suddenly drops as shown by dotted curve AB as shown in fig.38.5. Full conduction is reached rapidly. Under such conditions most of power supply voltage appears across the load, as drop across thyristor is hardly 1 V as compared to several volts across load. The SCR now acts as truly closed switch, allowing power to flow through the load circuit. It will continue to flow as long as holding current for thyristor is maintained.

(ii) When gate current flows: The above considerations apply for zero gate current i.e., when gate circuit is open. However, when a small gate voltage is applied, the gate current starts flowing. The flow of gate current helps in making current flow across junction J_2 i.e. due to high positive potential on the anode side of junction J_2, electrons in n-type material virtually pulled into p-type. Similarly, holes in p-type are pulled across J_2 into n-type material by the negative potential on right side of J_2.

Reverse Characteristics: When anode is connected to negative and cathode to positive of power supply, the curve between V and I is called reverse characteristic shown in fig.38.6. In this case, junctions J_1 and J_3 are reverse biased while J_2 is forward biased. It is clear that by increasing the reverse voltage beyond a certain value (point D) will result in the breakdown of the junctions J_1 J_2 and SCR can no longer block the flow of current through it. However, this voltage is very high as compared to the forward voltage.

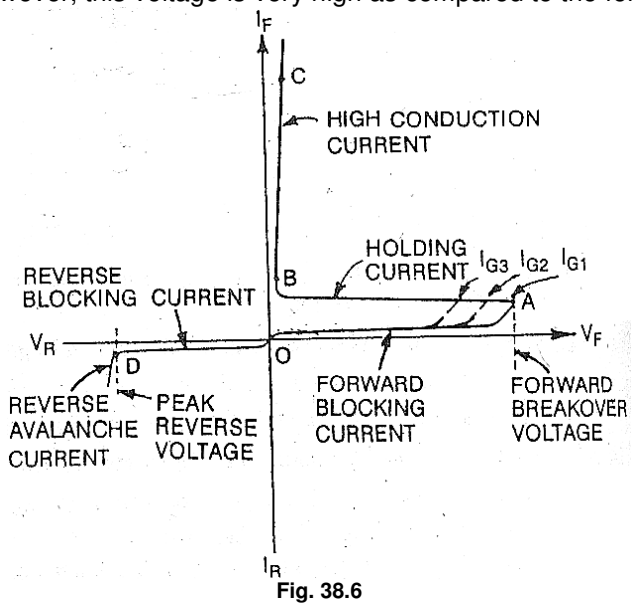


Fig. 38.6

Q.39 Mention the applications of SCR, DIAC and TRIAC. Marks (

Ans: **Applications of SCR:**

(i) It is used as Half-Wave and Full-Wave Controlled Rectifier
(ii) It is used as a Static Contactor
(iii) Use of SCR for Speed Control of DC Shunt Motors
(iv) SCRs are used in Static AC Circuit Breaker and Static DC circuit Breaker as a switch
(v) SCR are used in zero voltage switching
(vi) Used in Over-Voltage Protection
(vii) Used in Pulse Circuits
(viii) Used in Battery Charging Regulator.

Applications of Diac:

(i) It is used in Triac Lamp Dimmer Circuit
(ii) It is used in Heat Control Circuit
(iii) It is used primarily for triggering of triacs

Applications of Triac: Triacs are used in

(i) Motor Speed Regulation
(ii) Temperature control
(iii) Illumination control
(iv) Liquid level control
(v) Phase control circuits
(vi) Power switches etc.,
(vii) High Power Lamp Switching
(viii) AC Power Control

Q.40 What is electron emission and mention different types of electron emissions. Marks (5)

Ans: **Electron Emission:** The liberation of electrons from the surface of a substance (generally metals) is called electron emission. In certain materials, especially metals, the valence electrons in the outer most orbits are very loosely held by the nucleus. These loosely attached electrons, called free electrons, can be easily detached by applying some external energy.

Types of Electron Emission: The liberation of electrons from the surface of a metal is possible only when external energy supplied to the metal is equal to or more than the work function of that metal. This external energy may be supplied from a variety of sources such as heat energy, kinetic energy supplied by the bombarding electrons, light energy or the energy stored in the electric field. These electron emissions are called

(i) Thermionic emission (due to heat energy)
(ii) Secondary emission (due to kinetic energy)
(iii) Photo-electric emission (due to light energy)
(iv) High-field emission. (due to high electric field)

Q.41 Explain the construction and operation of a Mercury arc rectifier. Marks (9)

Ans: **Mercury-Arc Rectifier:**

Construction: It is a gas-filled tube employing a pool of mercury as a cathode with a side -arm glass bulb as shown in fig. 41.1. There are two main anodes A_1 and A_2, constructed from specially pure graphite in the case of small ratings and iron in larger ones, sealed into glass side arms projecting from the main bulb, above the liquid mercury cathode.

Above these arms, the glass bulb is in the form of a large dome whose function is to provide the cooling surface necessary to prevent excessive temperature rise. At the bottom, there is an auxiliary starting electrodes for the formation of the arc.

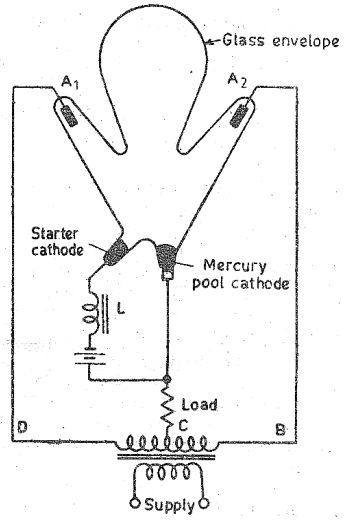


Fig. 41.1

Operation: During manufacture, the bulb is evacuated of other gases so that when it is finally sealed, it contains low pressure mercury pool vapour obtained from the mercury pool cathode. Electron emission from the mercury pool becomes possible when a *cathode spot* is formed on .the cathode pool surface. The cathode spot shows itself as a bright point of light which moves over the mercury surface, the spot being initiated by a small spark on the mercury. The spark produces the first electrons and positive ions, if one of the anodes is positive, the electrons are attracted and produce additional ions, which neutralize any negative space charge and an arc is established. The positive ion cathode sheath is very thin, so that the electric field intensity therein can reach the magnitude necessary for high-field emission. In this type of rectifier, the electron enters tbe arc through the cathode spot, which wanders on the surface of the pool of mercury. This motion is due to the forces exerted by the bombarding ions and the reaction of the vapourising gas. The ionised mercury ions that are formed are neutralized at the glass surface of the envelope and condense on the walls. The evaporated mercury returns to the pool under the action of gravity.

Q.42 Explain the construction, working and characteristics of depletion mode MOSFET. **Marks (10)**

Ans: **Construction of N-Channel Depletion MOSFET:** Fig. 42.1 shows the construction of N-channel depletion MOSFET. It consists of a highly doped P-type substrate into which two blocks of heavily doped N-type material are diffused forming the source and drain. An N-channel is formed by diffusion between the source and drain. The type of impurity for the channel is the same as for the source and drain. Now a thin layer of S_{i02} dielectric is grown over the entire surface and holes are cut through the SiO_2 (silicon-dioxide) layer to make contact with the N-type blocks (Source and Drain). Metal is deposited through the holes to provide drain and source terminals, and on the surface area between drain and source, a metal plate is deposited. This layer constitutes the gate. SiO_2 layer results in an extremely high input impedance of the order of 10^{10} to 10^{15} ohms for this area.

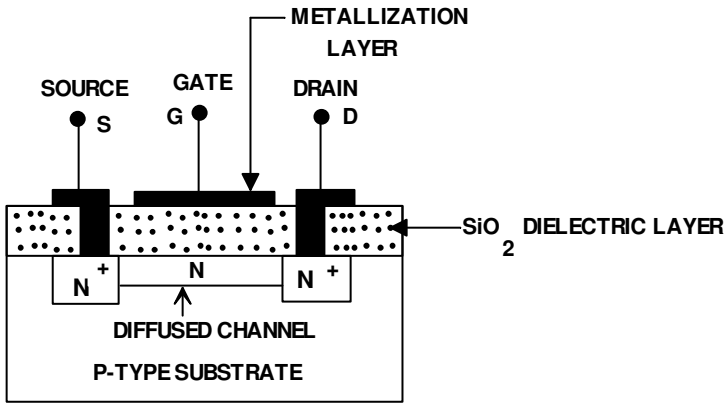


Fig. 42.1 N-CHANNEL DE-MOSFET STRUCTURE

Working: When negative gate-to-source voltage is applied, the N-channel MOSFET operates in the **depletion mode**.

When V_{GS} = 0, electrons can flow freely from source to drain through the conducting channel which exists between them. When gate is given negative voltage, it depletes the N-channel of its electrons by including positive charge in it as shown in fig. 42.2. Greater the negative voltage on the gate, greater is the reduction in the number of electrons in the channel and consequently, lesser its conductivity. In fact, too much negative gate voltage called $V_{GS(off)}$ can cut-off the channel. Hence, with negative gate voltage, a Depletion MOSFET behaves like a JFET.

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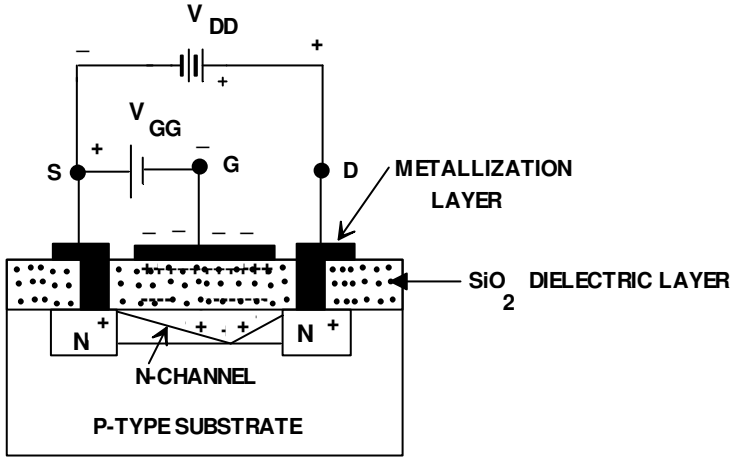
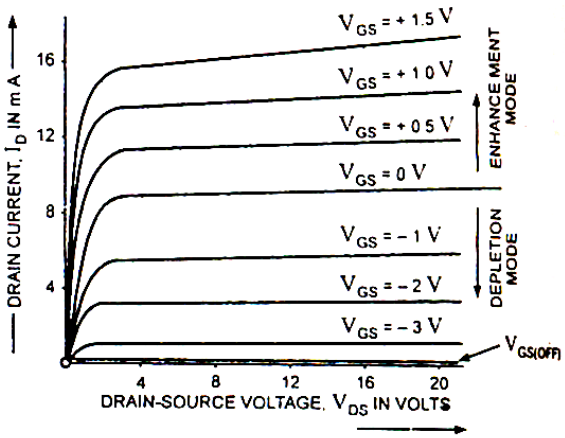


Fig 42.2 DEPLETION MODE OPERATION

Characteristics: Typical drain characteristics, for various levels of gate-source voltage, of N-channel depletion MOSFET are shown in fig.42.3. The upper curves are for positive V_{GS} and the lower curves are for negative V_{GS}. The bottom drain curve is for V_{GS} = $V_{GS(OFF)}$. For a specified drain-source voltage V_{DS}, $V_{GS(OFF)}$ is the gate-source voltage at which drain current reduces to a certain specified negligibly small value as shown in the figure. For V_{GS} between $V_{GS(OFF)}$ and zero, the device operates in depletion mode.



Drain Characteristics

Fig. 42.3

Q.43 Mention two applications each for FET and UJT. Marks (4)

Ans: **Applications of FET:**

(i) Buffer Amplifier
(ii) Low Noise Amplifier
(iii) Phase Shift Oscillator

Applications of UJT:

(i) Relaxation Oscillator
(ii) Saw-tooth generator
(iii) Pulse generators

Q.44 Explain how an op-amp is used as voltage to current converter and current to voltage converter Marks (10)

Ans: **Voltage to Current Converter:** Fig. 44.1 shows a voltage-to-current converter in which load resistor R_L is not connected to ground. The input voltage is applied to the non-inverting input terminal, by virtual ground, negative terminal of Op-amp is at same potential as applied input.

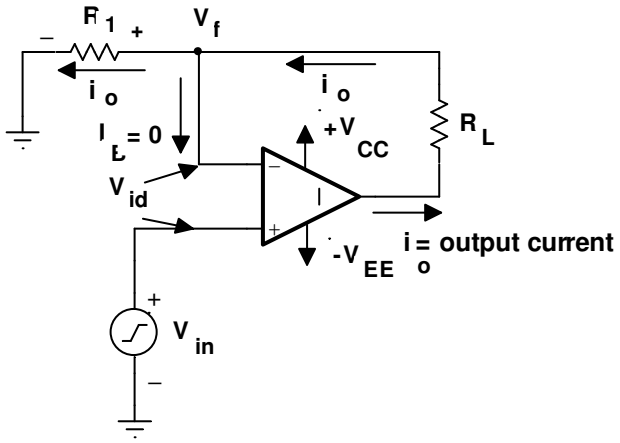


Fig.44.1

Writing Kirchhoff's voltage equation at the inverting terminal,

$$v_{in} = v_{id} + v_f$$

But $v_{id} \approx 0$ V, since A is very large in an ideal op-amp; therefore,

$$v_{in} = v_f$$

$$v_{in} = R_1 i_o$$

or

$$i_o = \frac{v_{in}}{R_1}$$

This means that in the above circuit, an input voltage v_{in} is converted into an output current of v_{in}/R_1.

Current-to-Voltage Converter:

The basic inverting operational amplifier is used as current-to-voltage converter which is shown in fig.44.2

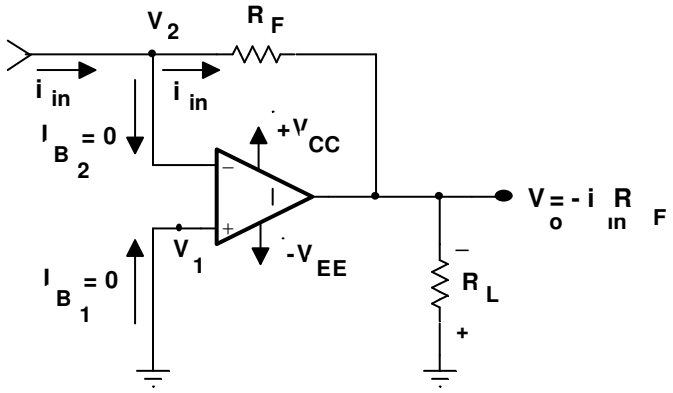


Fig.44.2

From basic fundamentals, the ideal voltage –gain of the inverting operational amplifier is given by

$$A_v = \frac{v_o}{v_{in}} = -\frac{R_F}{R_1}$$

Therefore,

$$v_o = -\left(\frac{v_{in}}{R_1}\right) R_F$$

However, in an ideal operational op-amp since, $v_1 = 0$ V and $v_1 = v_2$.

$$\frac{v_{in}}{R_1} = i_{in}$$

By substituting the this value in the equation of output voltage (v_o), we get

$$v_o = -i_{in} R_F$$

So, the above equation shows that the output voltage v_o becomes proportional to the input current i_{in}.

Q.45 Write short notes of the following: **Marks (2 X 7 =1**
(i) High frequency diodes
(iii) Thyratron

Ans: **High Frequency Diodes**: The diodes which are used at high frequencies are called High Frequency Diodes. Different types of high frequency diodes are:

(i) Tunnel Diode
(ii) PIN diode
(iii) Varactor Diode
(iv) Step-Recovery Diode
(v) Schottky Diode

(**i)Tunnel Diode**: A tunnel diode is a high conductivity two-terminal P-N junction doped heavily about 1,000 times higher than a conventional junction diode. Because of heavy doping depletion layer width is reduced to an extremely small value of the order of 10^{-5} mm, reverse breakdown voltage is also reduced to a very small value (approaching zero) resulting in appearance of the diode to be broken for any reverse voltage, and a negative resistance section is produced. The reduced depletion layer can result in carriers 'punching through' the junction with the velocity of light even when they do not possess enough energy to overcome the potential barrier. The result is that large forward current is produced at relatively low forward voltage (less than 100 mv). Such a mechanism of conduction in which charge carriers (possessing very little energy) punch through a barrier directly instead of climbing over it is called tunneling phenomenon. That is why such diodes are called the Tunnel Diodes.

Applications: The tunnel diodes are used a High Frequency Amplifier, High Frequency Oscillator or a Switch.

(**ii)PIN Diode**: In this diode a high resistivity (of the order of 0.1 Ω-m) intrinsic layer is sandwitched between and N-regions. The high resistance of the intrinsic layer provides the possibility of larger electric field between the P- and N-regions and therefore, electron-hole pair generation is enhanced enabling PIN diode to process even very weak input signals. Because of more separation between P-and N-regions, the capacitance C_{pn} reduced, because the capacitance decreases with the increase in separation of P-and N-regions. It allows the diode a faster response time making it suitable for use as Microwave Switch.

Applications: It is used as a switch at frequencies exceeding 300 MHZ

(**iii)Varactor Diode**: The varactor [also called the varicap, voltcap, epicap, VVC (voltage-variable capacitance) or tunning] diode is a semiconductor, voltage-dependent, variable capacitor. Basically, it is just a reverse-biased P-N junction diode whose mode of operation is based on its transition capacitance. The P- and N-regions (away from the space-charge region) are essentially low resistance areas because of high concentration of majority carriers. The space-charge or depletion region, which is depleted of majority carriers, serves as a dielectric. The P- and N-regions act as the plates of the capacitor and the depletion region acts as an insulating dielectric. The reverse biased P-N junction thus possesses junction capacitance, called the transition capacitance C_T. The value of junction capacitance is given as, $C_T = \frac{\in A}{W}$

Where $\in$ is the permittivity of the semiconductor material A is the area of the PN junction and W is the width of the space-charge region

Applications: (i) Varactor diode is used as a FM Modulator
(ii) It is used in AM Receivers

(iv)Step-Recovery Diode: It is also a voltage dependent variable capacitor diode but with unusual doping profile. It has concentration of charge carriers decreasing near the junction and therefore, phenomenon, called the reverse snap-off is caused. It operates as an ordinary diode at low frequency i.e. it conducts in forward direction but not in reverse direction. But when driven forward-to-reverse by a high frequency (above a few MHz) signal it does not recover immediately. Even during negative half cycle of the input signal, it keeps conducting for a while after which the reverse current suddenly drops to zero. The reverse current exists during the negative half cycle for a while because of the stored charge in the depletion region during the forward bias period, which takes some time to drain away from the junction. It looks as though the diode has suddenly snapped open during the early part of the reverse cycle. This snap-off current of a step-recovery diode is rich in harmonics and can be filtered go give a sinusoidal wave of a higher frequency

Applications: (i)These diodes are useful in Frequency Multipliers
(ii) These are also employed in Pulse and Digital circuits.

(v)Schottky Diode: At lower frequencies, an ordinary diode can easily turn off when the bias changes from forward to reverse. But with the increase in frequency (above 10 MHZ) the diode reaches a point where it cannot turn off fast enough to prevent noticeable current during part of the reverse half cycle. The effect is called the charge storage.
This effect is eliminated in Schottky diode. Such a diode has no depletion layer eliminating the stored charges at the junction. Because of lack of charge storage the Schottky diode can switch off faster than an ordinary diode.

Applications: The most important application of this diode is in Digital Computers.

Q.45.ii) **UJT:** A uni-juction transistor (UJT) is a three terminal semiconductor device having two doped regions. In the three terminals, it has emitter (E) and two bases ($B_1$and B_2). This device has only one pn junction, therefore, naming it a 'transistor' is really misnomer. However, from the outer look (packages), it resembles to a bipolar transistor and hence the name uni-juction transistor. This device has a unique characteristic that when it is triggered, the emitter current increases regeneratively until it is limited by the emitter power supply.

Construction: The Structure and symbol of UJT are shown in fig.45.1. UJT consists of an n-type silicon bar which is lightly doped. Two ends connections are taken from the bar called base-one (B_1) and base-two (B_2). A heavily doped p-type region is diffused to n-type bar nearer to B_2.

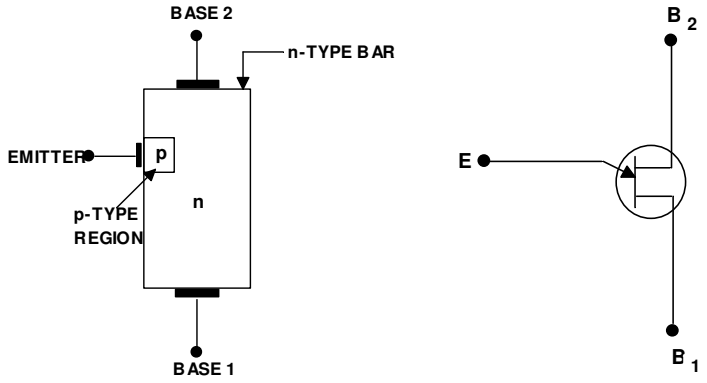


Fig. 45.1

Working: Make the circuit arrangement as shown in fig.45.2. Normally, B_2 is kept positive w.r.t B_1. A variable positive voltage is supplied to the emitter through a switch S.
(i) When the emitter circuit is closed through a switch S but the emitter voltage is reduced to zero. This voltage establishes a reverse bias on the pn junction and the emitter current is cut-off.
(ii) When a +ve voltage is applied at the emitter, the p-n junction will remain reverse biased so long as the input emitter voltage is less than V_1 (=η V_{BB}). If the input voltage applied to the emitter is increased, a stage reaches when it exceeds V_1 by V_D i.e.V_E = $V+V_D$. This will bring the p-n junction in forward biased condition. At this stage, p-type material injects holes into the n-type bar. These holes are repelled by positive B_2 terminal and are attracted towards negative B_1 terminal of the bar. This accumulation of holes in the emitter to B_1 region decreases and the resistance of this section (i.e. R_{B1}) of the bar. This results internal voltage drop from emitter to B_1 and consequently increases the emitter current I_E. This process goes on and eventually a condition of saturation is reached. This is a stage where the emitter current is limited by only emitter power. The device is now said to be in the ON state.

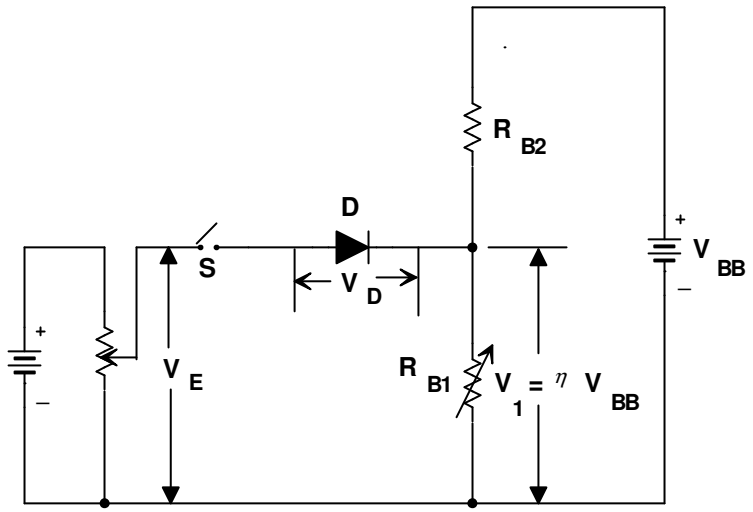
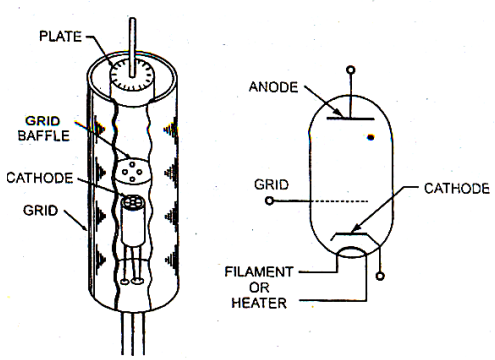


Fig. 45.2

Applications of UJT : (i)Relaxation Oscillator
(ii)Pulse generators
(iii)Saw-tooth generators

(iv)Triggering circuits
(v)Phase control
(vi)Timing circuits.

Q.45.iii)Thyratron: The trade name of a hot-cathode gas triode is thyratron. A thyratron consists of three electrodes, namely cathode, anode and control grid. These electrodes are enclosed in a glass envelope containing some inert gas at low pressure. The cut-away view and schematic symbol of the tube are shown in fig.45.3(a) and 45.3(b). It consists of a metal cylinder surrounding the cathode with a perforated disc known as grid baffle near the center. Thus, the control grid acts as an electrostatic shield between cathode and anode except for the holes in the grid baffles.



(a) Construction *(b) Symbolic Representation*

Fig. 45.3

Operation: When a cathode is heated, a large number of free electrons are emitted form its surface. If the control grid is kept at sufficient negative potential the electrons do not acquire necessary energy to cross the grid baffles to reach at the anode. Hence the plate current is substantially zero. As the negative grid potential is reduced, some of the emitted electrons reach to the anode through the holes of the grid baffles and constitute a small current. These electrons do not posses enough speed and energy to cause ionization of gas. However, if the negative potential on grid is further reduced gradually, the electrons acquire more speed energy. At some grid potential, called grid voltage, ionization of the gas occurs and the plate current rises to a large value. So, the firing (gas ionization) of the tube can be obtained at any desired potential by controlling the negative potential on the control grid.

Applications: Thyratron is used as (i) Switch (ii) controlled rectifier.

Q.46 Differentiate between a current source and a voltage source. Give their Graphical representation. How can they be converted from one to another ? Marks (6)

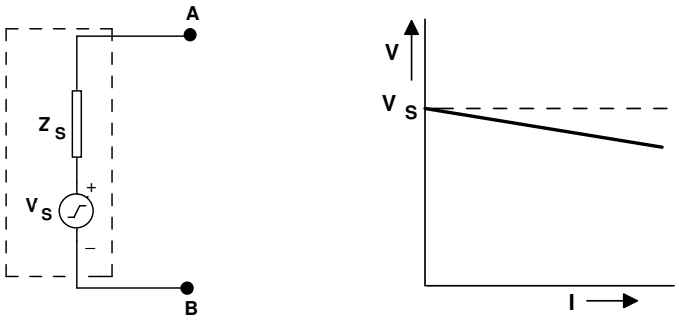
Ans: Differences between Current source and Voltage source:

(i) When the value of load resistance (or impedance is very large as compared to the internal resistance (or impedance) of the source, the source is treated as a voltage source. Whereas, when the value of load resistance (or impedance) is very small as compared to the internal resistance (or impedance) of the source, the source is treated as a current source.

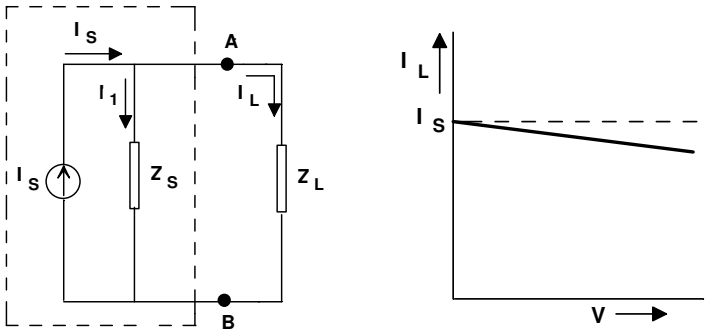
(ii) A voltage source has almost constant terminal voltage whereas a current source has almost constant load current.

(iii) A voltage source behaves as a constant voltage source irrespective of load Current whereas a current source behaves as a constant current source irrespective of the value of load resistance.

Graphical Representation of Voltage Source:



Graphical Representation of Current Source:



Conversion of Voltage Source into Current Source and vice versa: Consider an ac source connected to load impedance Z_L *shown in below fig.46 (a).* The source can either be treated as a voltage source or a current source as shown in fig.46(b) and fig.46c). The voltage-source representation consists of an ideal voltage source V_s in series with source impedance Z_{S1}. The current-source representation consists of an ideal current source I_s in parallel with source impedance Z_{S2}. These are the two representations of the same source. Both types of representations must appear the same to the externally connected load impedance Z_L. They must give the same results. In fig.2 (b), if the load impedance Z_L is reduced to zero (i.e. the terminals *A* and *B* are short-circuited) the current through this *short* is given as

$$I_L(short-circuit) = \frac{V_S}{Z_{S1}} \quad \text{---------- (i)}$$

Both the representations (voltage-source and current-source) must give the same results. This means that current source in Fig.46(c) must also give the same current (as given by equation (i)) when terminals *A* and B are shorted. But the current obtained by shorting the terminals (A) and (B) of Fig.46(c) *is* simply the source current I_S (the source impedance Z_{S2} connected in parallel with a short-circuit*).* Therefore, the current I_s of the equivalent current source must be the same as that given by the equation (1) i.e.

$$I_L(short-circuit) = I_S = \frac{V_S}{Z_{S1}} \quad \text{---- (1)}$$

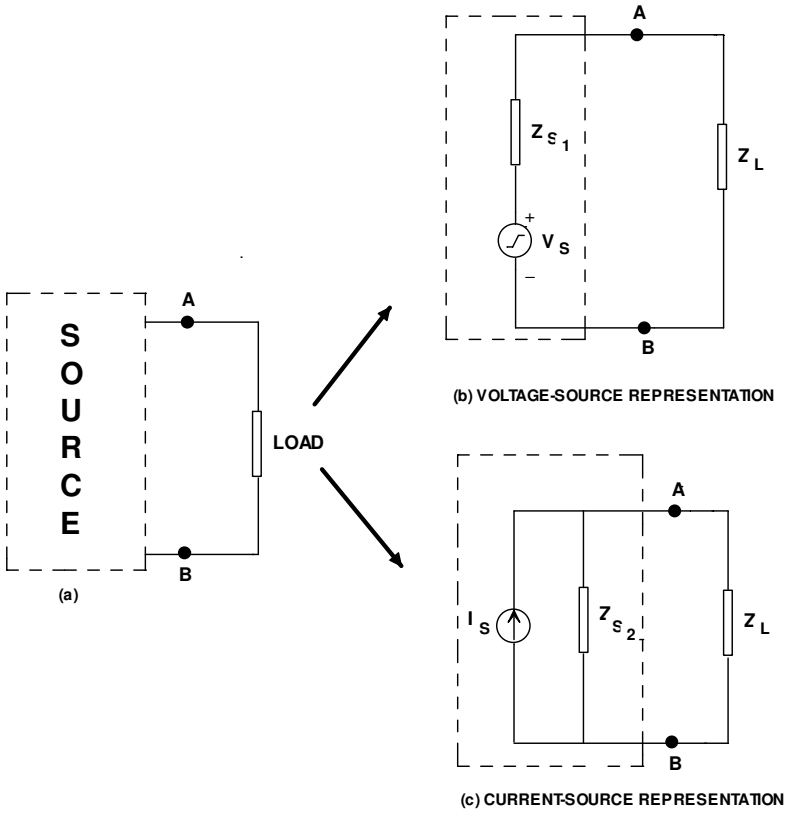


Fig .46(a, b, c)

Again the two representations of the source must give the same terminal voltage when the Load impedance Z_L is disconnected from the source (i.e. when the terminals A and B are open-circuited. In fig (b) the open circuit terminal voltage is simply V_s. There is no voltage drop across the internal impedance Z_{SI}. When the terminals A and B are open-circuited, the whole of the current I_s flows through the impedance Z_{S2}. The terminal voltage is then the voltage drop across this impedance. That is V_T (open-circuit) = $I_s Z_{s2}$ -------- (2) Therefore, if the two representations of the source are to be equivalent, then the equation must be $V_T = V_s$

Using equations (1) and (2), we get $I_S Z_{S1} = I_S Z_{S2}$

$Z_{S1} = Z_{S2} = Z_S$ (say) or

Then both equations (1) and (2) reduces to $V_S = I_S Z_S$ Hence, in both the representation of the source, the source impedance is faced by the same load resistance Z_S at terminals AB. Thus it establishes the equivalence between the voltage source representation and current source representation, under short-circuit and open-circuit conditions.

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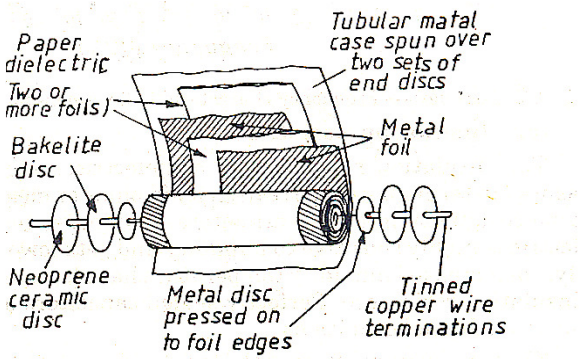
Q.47 Classify the capacitors on the basis of dielectrics used and discuss the functionl Of one one of them. Marks (5)

Ans: **Classification of Capacitors:** The capacitors are classified on the basis of dielectric used are

1. Fixed Capacitors:
(i) Paper Dielectric Capacitors
(ii) Mica Dielectric Capacitors
(iii) Ceramic Dielectric Capacitors
(iv) Glass Dielectric Capacitors
(v) Plastic Dielectric Capacitors
(vi) Electrolytic Capacitors
(vii) Air Dielectric Capacitors
(viii) Vacuum Capacitors

2. Variable Capacitors:
(i) Air Dielectric Capacitors
(ii) Mica Dielectric Capacitors
(iii) Plastic Dielectric Capacitors
(iv) Ceramic Dielectric capacitors

Metal foil impregnated paper capacitor These types of capacitors are constructed by rolling impregnated paper insulation between metal electrodes. Electrodes are usually aluminum (high conductivity, low cost) but could also be of tin (cheaper, less conductive) or copper (costly, better conductive). The thickness of paper used varies from 7.5 microns (1 micron. =one millionth of a matter) to 25 microns and the thickness of metal foil used is around 7 microns. Voltage stress of impregnated paper varies from 15 to 25 v/micron.



Construction of a metal foil impregnated paper capacitor.

These types of capacitors are normally manufactured to a tolerance of ± 20% of the desired capacitance within the same batch. Their best manufacturing tolerance can be ± 5%. They have a moderate power factor (0.005 to 0.01 at 10KHz). Their temperature coefficient is positive and ranges from + 100 to + 200 ppm/°C. (ppm per degree centigrade means change in capacitance per million parts of original capacitance with one degree rise in temperature). The typical voltage rating is about 300 V (r.m.s) at 50 Hz. Capacitance range is usually from 1000 pF to 0.5 μF. They are normally used in radio frequency *(i.e.* between 10 kHz and 300 GHz) applications. The maximum temperature withstanding capacity is 100°C.

Q.48 Briefly explain the different processes by which electron emission takes place from the Surface of metals. Marks (4)

Ans: **Methods of Electron Emission :**

(i) Thermionic Emission: The method of electron emission from a metal surface to which heat energy is supplied is called thermionic emission. At normal temperature, the energy possessed by the free electrons in the metal is not sufficient to cause them to escape from the surface. However, when heat energy is supplied to the metal, some of the heat energy is converted into kinetic energy which accelerates the motion of free electrons. When the temperature is raised sufficiently, these electrons acquire sufficient energy equal to the work function of the metal. Consequently, they overcome the restraining forces (surface barrier) and escape from the metal surface.

(ii)Secondary Emission: The emission of electrons from a metallic surface by the bombardment of high-speed particles (generally electrons) is called secondary emission. When high-speed electrons emitted by a source suddenly strike a metallic surface, they may transfer all or a part of their kinetic energy to the free electrons in the metal. If the energy of these incident electrons is sufficiently high, some of the free electrons may be dislodged from their parent atoms and escape from the metal surface. This phenomenon is called secondary emission.

(iii)Photo-electric Emission: The emission of electrons from a metallic surface by the application of light energy is called Photo-electric emission. When a beam of light strikes at the surface of certain metal of low work function such as potassium, sodium and cesium, the electrons may be emitted from their surface, if the quantum of energy carried by the photons is equal to or greater than the work function of the metal. Such a phenomenon is termed as photo-electric emission.

(iv)High-Field Emission: The emission of electrons from a metallic surface by the application of strong electric field is known as High field emission. When a positively charged high voltage electrode is placed near to a metal surface, an intense electric field is set between the electrode and the metal surface which exerts an attractive force on the free electrons in the metal. If the electric field is of sufficient intensity, it succeeds in overcoming the restraining forces of the metal surface and hence the free electrons are emitted from the metal surface.

Q.49 Draw and explain triode characteristics. What are μ, g_m and r_p ? How can these be determined from the characteristics. Marks (8)

Ans: **Characteristics of Triode**:

These are three types namely (i) Plate characteristics (ii) Mutual or transfer characteristics and (iii) Constant current or amplification characteristics.

(**i)Plate Characteristics (Plate current-Plate Voltage Characteristic**: The curve drawn between plate current and plate voltage, keeping grid potential constant, is known as plate characteristics. The characteristics can be obtained by keeping grid potential Eg constant at a particular value, varying the plate voltage in steps, noting the corresponding plate currents and Plotting the results so obtained. The process is repeated at different grid potentials. The plate characteristics for a typical triode as shown in fig.49.1 the curves being nonlinear in the lower portion close to plate current cut-off and fairly linear at higher voltages. The curvature at the low plate current is due to space charge. At higher plate currents there will be a bend again because of saturation. The portion of the characteristics between upper and lower bends is most useful for the purpose of amplification of signals.

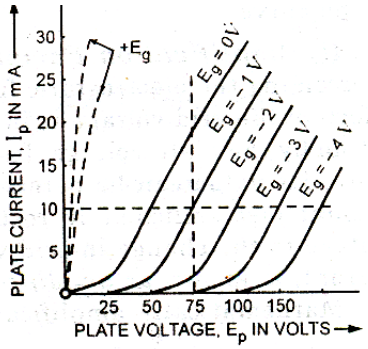
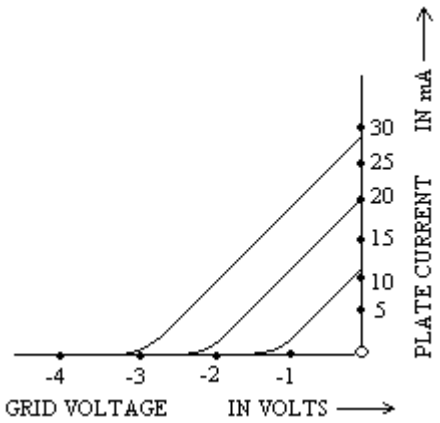


Plate Characteristics of a Triode

Fig. 49.1

(ii) Transfer or Grid or Mutual Characteristics: Transfer Characteristics are the curves drawn between plate current and grid voltage, the plate voltage being kept constant. The transfer characteristics can be obtained by keeping plate voltage Ep constant at a particular value varying the grid potential, noting the corresponding plate currents, as shown in fig. 49.2

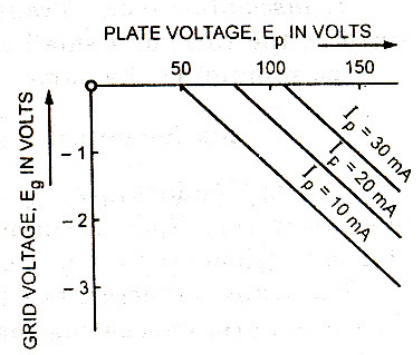


Transfer or Mutual Characteristics of a Triode

Fig. 49.2

When the grid is positive, it helps the plate to attract the electrons hence plate current is increased. When the grid is negative with respect to cathode it retards the action of plate and hence plate current is reduced. It is to be noted that each curve intersects the grid voltage axis at a specific point that indicates the value of the negative grid voltage required to make the plate current zero at the particular value of applied voltage to plate. This is also called cut-off bias.

(iii)Constant Current or Amplification Characteristics: The curve drawn between plate voltage and grid voltage, plate current being kept constant, is known as constant plate current characteristics. For obtaining data for this characteristics the circuit diagram shown in fig. 49.3 is used. First of all the plate is given a suitable high potential and then grid voltage is changed until the highest plate current for which it is desired to obtain the characteristic is obtained. Now plate potential is reduced in steps and at each step the grid voltage is readjusted so that the same plate current is obtained. This is repeated with different plate currents and curves are plotted as shown in fig.49.3



Constant Plate Characteristics of a Triode

Fig. 49.3

Amplification Factor (μ) and Determination of μ from Static characteristics: It is a measure of the relative effectiveness of the control grid in overcoming the electrostatic field produced by the plate. Its value depends to a large extent on the spacing between the grid and plate. Its value can be determined by changing the plate voltage in the opposite direction by an amount just sufficient to restore the previous plate current value. Mathematically amplification factor, μ is defined as ratio of small change in plate voltage to small change in grid voltage i.e.,

$$\mu = -\frac{\delta E_p}{\delta E_g}$$

The negative sign indicates that the changes in two voltages are oppositely directed. Obviously, amplification factor μ is nothing but the slope of constant plate current characteristic.

Plate Resistance (r_p) and determination of r_p from static characteristics: When current flows through a tube from plate to cathode, there is a voltage drop across the tube and electrical energy is converted into heat at the rate of $E_p I_p$ watts where E_p and I_p are plate voltage and plate current respectively. Plate resistance is the resistance offered by the tube to the ac component of the plate current. Mathematically plate resistance r_p is defined as ration of small change in plate voltage to small change in plate current i.e.

$$r_p = \frac{\delta E_p}{\delta I_p}$$

The coefficient r_p is often called a dynamic or incremental plate resistance. The coefficient r_p is also obtained by taking reciprocal of the slope of the plate characteristic curve.

Tran conductance (gm) and determination of gm from static characteristic: It is defined as the ratio of a small change in plate current to the small change in grid voltage, the plate voltage remaining the same i.e.,

Mathematically, $g_m = \frac{\delta I_p}{\delta E_g}$ its value can be easily determined from the slope of mutual characteristic of the tube.

Q.50 Distinguish between majority and minority carriers in a semiconductor. Define mobility of charge carriers. Marks (5)

Ans: **Distinguish between majority and minority carriers:**

(i) Majority Carriers are the charge carriers which are maximum in number. For example in n-type semiconductor the majority charge carriers are electrons and in p-type semiconductor, the majority charge carriers are holes as shown in fig.50.1, whereas Minority Carriers are the charge carriers which are minimum in number. For example in n-type semiconductor, the minority charge carriers are holes and in p-type semiconductor, the minority charge carriers are electrons as shown in fig.50.2.

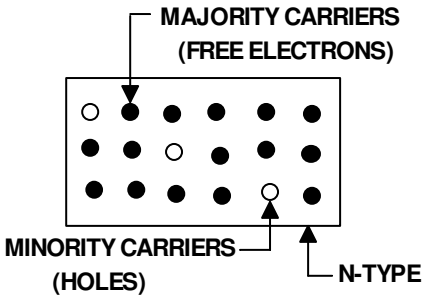


Fig. 50.1

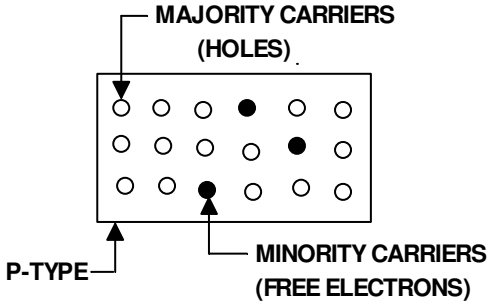


Fig.50.2

(ii) Most of the current conduction in a semiconductor is due to majority carriers, whereas, the current due to minority carriers is very small, so, it almost negligible.

Mobility of charge carriers: When a steady electric field E volt/meter is applied to a metal, the electrons move towards the positive terminal of the applied voltage. In their way, they continuously collide with other free electrons and rebound in a random fashion. Each collision being inelastic i.e., the electrons lose some kinetic energy.

After the collision, the electrons are accelerated by the electric field and gain certain component of velocity in the direction opposite to that of electric field (- E). They lose some of their energy at the next collision. Thus the applied electric field does not stop collision and random motion but makes the electrons to drift towards the positive terminal. So, the drift velocity v is proportional to the applied electric fied E, i.e., $V = \mu_e E$ Where μ_e is called mobility which is defined as the Average Particle Drift velocity per unit electric field and is expressed in m^2/Vs.

Q.51 Discuss how a depletion layer is formed in a P-N diode and how does it vary with biasing ? Draw V-I characteristics of P-N junction diode. Marks (7)

Ans: **Formation of Depletion Layer in a P-N junction Diode**: The two types of extrinsic semiconductors are p-type and n-type as shown in fig.51(a) The p-type semiconductor is having negative acceptor ions and positively charged holes. Whereas, the n-type semiconductor is having positive donor ions and negatively charged electrons.

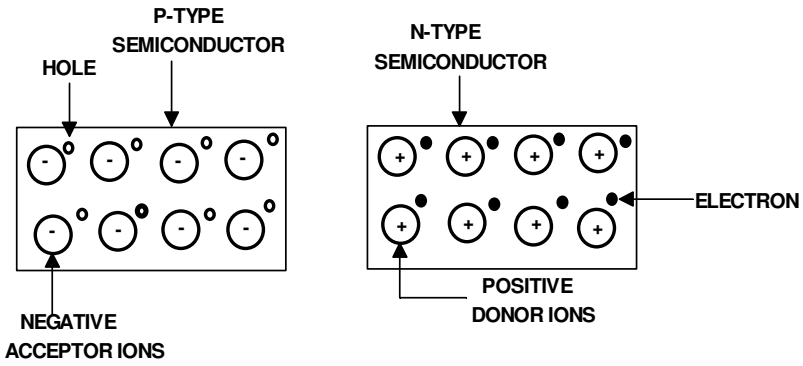


Fig. 51(a)

When these two semiconductors are joined together and suitably treated, they from a pn junction. The moment they form a pn junction, some of the conduction electrons from n-type material diffuse over to the p-type material and undergo electron-hole recombination with the holes available in the valence band. Simultaneously holes from p-type material diffuse over to the n-type material and undergo hole-electron combination with the electrons available in the conduction band. In this process, some of the free electrons move across the junction from n-type to p-type, leaving behind positive donor ions as they are robbed of the free electrons. This establishes a positive charge on the n-side of the junction. Simultaneously, the free electrons which cross over the junction recombine with the holes of p-type and uncover some of the negative acceptor ions as shown in fig.51(d) This establishes a negative charge on the p-side of the junction. This process of diffusion continues till a sufficient number of donor and acceptor impurity ions are uncovered and establish a requisite potential difference (i.e. nearly 0.3 V in case the pn junction is formed of germanium semiconductor and 0.7 V for silicon pn junction). After this, further diffusion is prevented because now positive charge on n-side repels holes to cross from p-type to n-type and negative charge on p-side repels free electrons to enter from n-type to p-type.

A potential difference created across the junction acts as a barrier which restricts further movement of charge carriers (i.e. holes and electrons) is called a Potential Barrier or Junction Barrier V_o. Thus, a region around the junction from which the charge carriers (free electrons and holes) are depleted is called Depletion Layer.

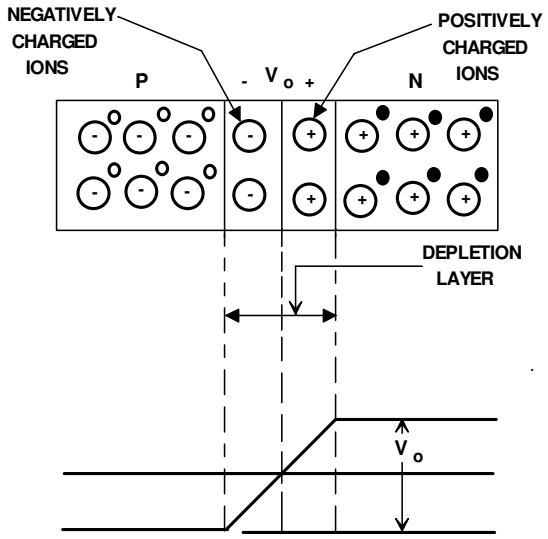


Fig. 51(b)

Behaviour of a PN junction Diode under Biasing:

When a pn junction is connected across an electric supply (potential difference), the junction is said to be under biasing.

Forward Biasing: When the positive terminal of a d.c source or battery is connected to p-type and negative terminal is connected to n-type semiconductor of a pn junction as shown in fig.51(c), the junction is said to be in forward biased. In this circuit, the holes on the P-side being positively charged particles are repelled from the positive bias terminal and driven towards the junction. Similarly, the electrons on the N-side are repelled from the negative bias terminal and driven towards the junction. The result is that the depletion region is reduced in width and the barrier potential is also reduced. Once the potential barrier is eliminated by the forward voltage, a conducting path is established for flow of current.

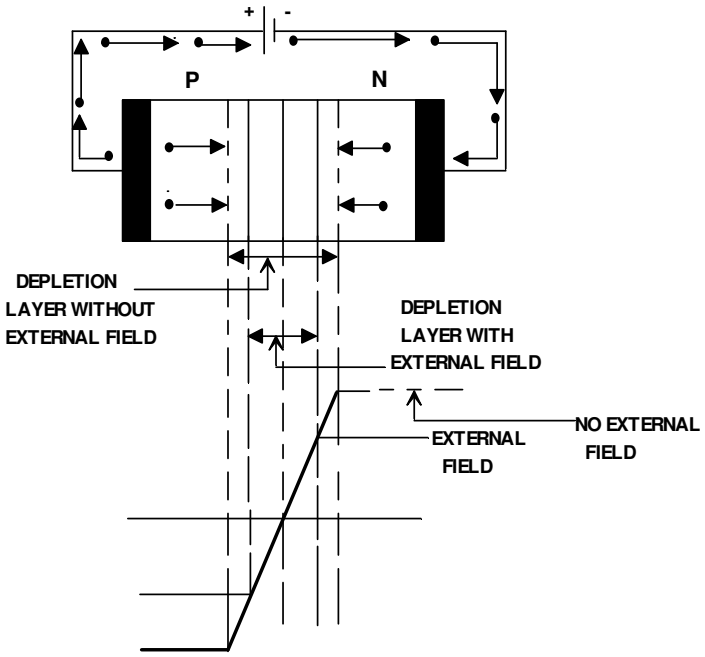


Fig. 51(c)

Reverse Biasing: When the positive terminal of a d.c. source or battery is connected to n-type and negative terminal is connected to p-type semiconductor of a pn junction, as shown in fig.51 (d), the junction is said to be in reverse biased. In this circuit arrangement, the electrons form the N-side are attracted to the positive bias terminal and holes form P-side are attracted from the negative bias terminal. Thus, the depletion region is widened and the barrier potential is increased by the magnitude of the applied bias. With the increased barrier potential, there is no possibility of majority carrier current flow across the junction. Thus the P-N junction is in non-conducting state.

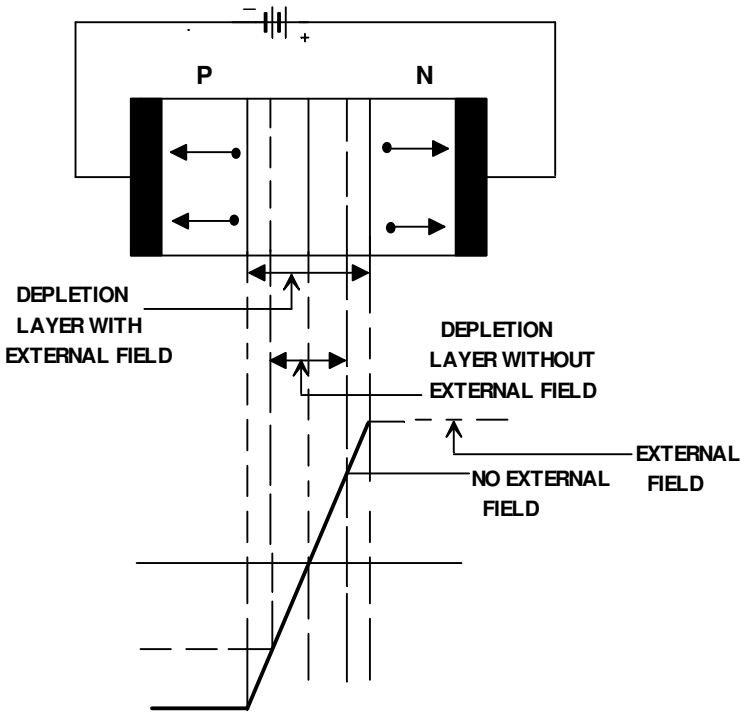


Fig. 51 (d)

V-I characteristics of P-N junction diode are shown in fig. 51(e)

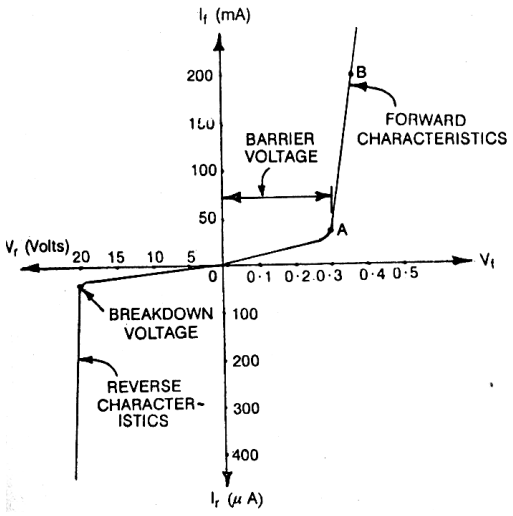


Fig. 51(e)

Q.52 What is cut-in voltage in semiconductor ? Marks (

Ans: **Cut-in voltage**: The forward voltage (0.3V for Ge and 0.7V for Si diodes) at which the current through the diode or pn junction starts rising abruptly is known as cut-in voltage or knee voltage of a diode.

Q.53 What is zener diode and how does it regulate the voltage ? What happens to the series current, load current and zener current when the d.c. input voltage of a zener regulator increases ? Marks (6)

Ans: **Zener Diode:** Zener diode is specially designed silicon diode which is optimized to operate in the breakdown region.Zener diode is used as a voltage regulator: Fig.53.1 shows the circuit arrangement. The zener diode of zener voltage V_z is reverse connected across the R_L across which constant voltage ($V_o = V_z$) is desired. A resistor R is connected in series with the circuit which absorbs the output voltage fluctuations so as to maintain constant voltage (V_o) across the load.

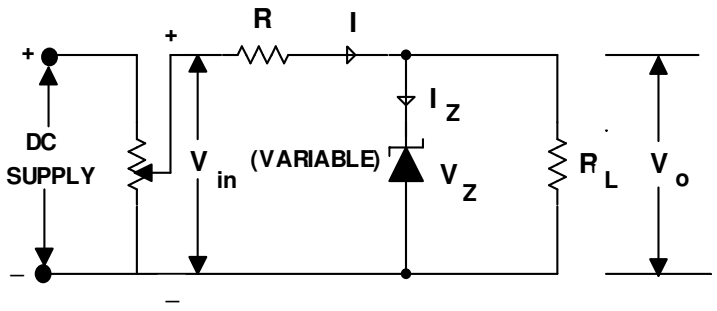


Fig. 53.1

When the supply voltage V_S increases, the current through both the zener diode and load resistance R_L increases.

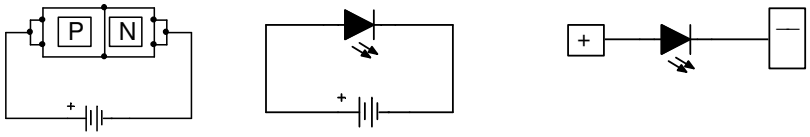
At the same time, however, the current through the diode increases more than proportionately. As a result, a greater voltage drop will occur across the series resistor R_S and the output voltage V_{OUT} (voltage across the diode or load resistance R_L) will become very close to the original value. When the supply voltage V_{IN} is less than zener voltage V_Z of the zener diode, no current flows though the diode, because the diode is reverse biased and the same voltage appears across the load. When d.c. input voltage of a zener regulator increases, series current I, load current I_L and zener current I_Z increases.

Q.54 What is LED ? Give its principle of working and applications. Marks (4)

Ans: **LED:** LED (Light Emitting Diode) is a Forward Biased P-N junction diode which emits light under the influence of an electric field. The structure, schematic diagram and symbol of LED are shown in fig.54(i), 54(ii) and 54(iii).

Principle of working: When P-N junction diode is forward-biased, the potential barrier is lowered. The conduction band free electrons from n-region cross the barrier and enter the p-region. As these electrons enter the p-region, they fall into the holes lying in the valence band. Hence they fall from a higher level to a lower energy level. In the process, they radiate energy. In the ordinary diodes (rectifier and signal diodes) this energy

radiates in the form of heat, as these diodes are made of silicon or germanium which a opaque material and block the passage of light.



(i) Structure (ii) Schematic Diagram (iii) Schematic Symbol

Fig. 54

LED's are made from gallium arsenide phosphide (GaAsP) and gallium phosphide (GaP) and these radiate energy in the form light (or photons) and hence they glow.

Applications: LEDs that emit visible light (such as red, green, blue etc.) find their applications in the following areas
(i)Instrument Display panel indicator
(ii)Digital watches
(iii)Calculators
(iv)Multimeters
(v)Intercom
(vi)Telephone switch boards
Infrared LED's find applications in remote control schemes, object detectors etc.

Q.55 What is varactor diode ? On what factor its operation is based ? Give its applications. Marks (4)

Ans: **Varactor diode:** The varactor diode [also called the varicap, voltcap, epicap, VVC (voltage-variable capacitance) or tunning] is a voltage-dependent, variable capacitor. Basically, it is a reverse-biased P-N junction diode whose mode of operation is based on its transition capacitance.

Operation based factor: The P- and N-regions (away from the space-charge region) are essentially low resistance areas because of high concentration of majority carriers. The space-charge or depletion region, which is depleted of majority carriers, serves as a dielectric. The P- and N-regions act as the plates of the capacitor and the depletion region acts as an insulating dielectric. The reverse biased P-N junction thus possesses junction capacitance, also called the transition capacitance C_T. The junction capacitance is given as

$$C_T = \frac{\in A}{W}$$

Where $\in$ is the permittivity of the semiconductor material. A is the area of the PN junction and W is the width of the space-charge region. With increase in reverse-bias potential,
The width of the space charge region increases, which in turn reduces the Transition Capacitance C_T as shown in fig.55.1

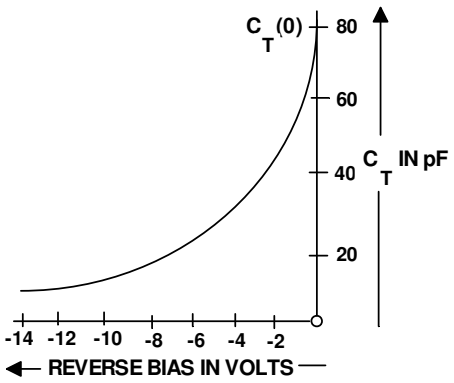


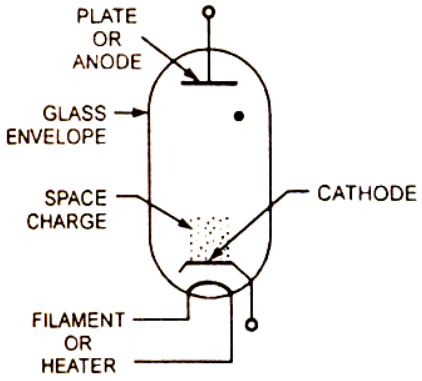
Fig.55.1

Applications: Varactor diodes are used in
(i) FM Modulators
(ii) High Frequency Control Devices
(iii) Adjustable Band pass Filters
(iv) Parametric Amplifiers.

Q.56 Discuss the working of a Thyratron. Bring out its practical applications.

Marks (6)

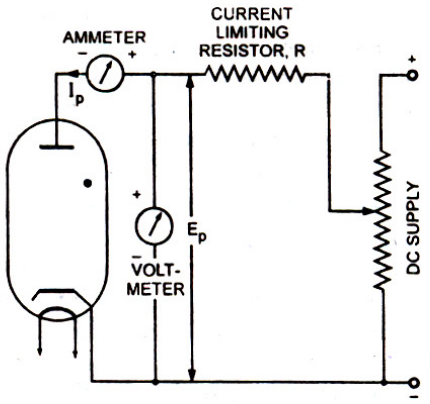
Ans: **Gas Diode:** The gas-filled diode or phanotron is shown in fig.56.1, consists of an oxide coated thermionic cathode with a graphite or metal plate enclosed in a glass bulb. After complete evacuation of the tube, a drop of liquid of mercury is introduced and the tube is sealed off so that the bulb is filled with mercury vapours during operation.



Symbolic Representation of a Phanotron

Fig.56.1

Operation: The plate is held at positive potential and cathode at negative potential in a phanotron is shown in fig.56.2



Circuit Diagram For Determination of Plate Characteristics of a Phanotron

Fig. 56.2

When cathode is heated a large number of electrons are emitted. As the plate voltage of a gas-filled diode is gradually increased from zero, the tube remains non-conducting until a certain critical plate voltage, called the ionizing or striking voltage reaches. Before plate voltage attains a critical value, the gas is not ionized and the tube conducts a very small current and behaves like a vacuum diode. As the plate attains critical voltage, which is usually 15 V, the gas gets ionized and plate current immediately attains its full value determined by the circuit impedance. The tube is then said to be fired or ignited. Now, further increase in plate voltage will cause an increase in current resulting in larger drop across the load, the voltage drop across the tube remaining the same about 15 V.

Characteristics: The plate characteristics of a gas-filled diode are shown in below fig.56.3 Initially with the increase in plate voltage, the plate current raised slowly. But at ionization potential, the plate current rises sharply. However, drop across the tube remains constant. The extra voltage is dropped across the external series resistance R.

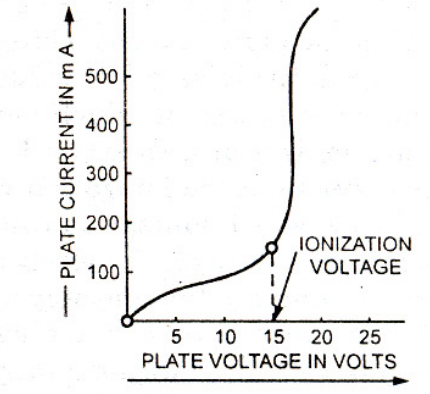


Plate Characteristic of Phanotron

Fig. 56.3

Working of Thyratron: When cathode is heated, a large number of free electrons are emitted from its surface. If the control grid is kept at sufficient negative potential the electrons do not acquire necessary energy to cross the grid baffles to reach the anode. Hence the plate current is approximately zero. As the negative grid potential is reduced, some of the emitted electrons reach the anode through the holes of the grid baffles and constitute a small current. These electrons do not possess enough speed and energy to cause ionization of the gas. However, if the negative potential on grid is further reduced

gradually, the electrons acquire more speed and energy. At some grid potential, call critical grid voltage, ionization of the gas occurs and the plate current rises to a large value.
At the critical grid voltage, the gas ionizes, creating free electrons and positive gas ions. The positive ions tend to neutralize the space charge which reduces the internal resistance of the tube, resulting in large plate current. In addition, the positive ions are attracted by the negative grid. These positive ions neutralize the effect of negative charge on the grid and the grid loses all its control and the tube behaves as a gas diode.

Practical Applications: Thyratron has two main fields of applications:
(i)As an electronic switch to handle heavy currents: In a thyratron, when the grid voltage is made equal to critical grid voltage, the tube fires and the anode circuit is closed. Thus, to switch on or off, an electrical device (d.c.motor, lamp etc.) may be connected in the anode circuit.
(ii)As a grid controlled rectifier when voltage control is required: In thyratron, the output d.c. voltage can be changed easily by changing the grid voltage (the change in grid voltage changes the firing angle).

Q.57 Explain the working of glass bulb mercury arc rectifier. Marks (4)

Ans: **Working of Mercury Arc Rectifier**: Mercury Arc Rectifier is shown in fig.57.1. Electron emission from the mercury pool becomes possible when a cathode spot is formed on the cathode-pool surface. The cathode spot shows itself as a bright point of light which moves over the mercury surface, the spot being initiated by small spark on mercury.
The spark produces the first electrons and positive ions, if one of the anodes is positive, the electrons are attracted and produce additional ions which neutralize any negative space charge and an arc is established. The positive ion cathode sheath is very thin, so that the electric field intensity therein can reach the magnitude necessary for high-field emission. In this type of rectifier, the electron enters the arc through the cathode spot, which wanders on the surface of the pool of mercury.
This motion is due to the forces exerted by the bombarding ions and the reaction of the vaporizing gas. The ionized mercury ions that are formed are neutralized at the glass surface of the envelope and condense on the walls. The evaporated mercury returns to the pool under the action of gravity.

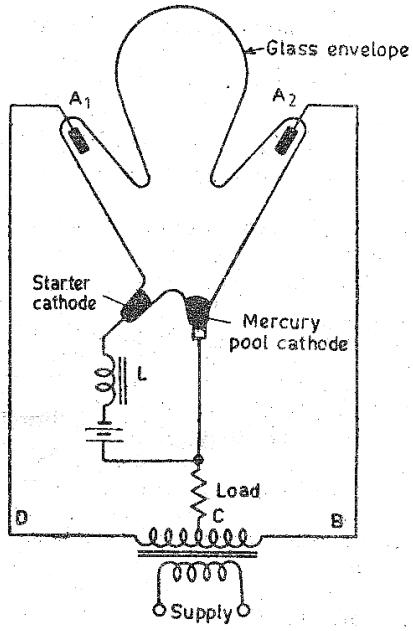


Fig. 57.1

Q.58 Distinguish between forward active, saturation, cut-off and reverse active operation of a transistor. Marks (4)

Ans: **I.Forward Active**: In this condition, base-emitter junction is forward biased, whereas the base-collector junction is reverse biased. When the transistor is an active region, collector current is proportional to the emitter current. Generally, transistor is operated in this region for amplification,

II.Saturation: In this condition, both base-emitter and base-collector junctions are forward biased. When the transistor is in saturation, the collector current becomes independent of the base current and is limited by external circuitry. The transistor acts like a closed switch.

III.Cut-Off: In this condition, both junctions are reverse biased. The emitter does not emit carriers into the base and no carriers are collected by the collector (except a little thermally generated minority carrier). Thus, the transistor acts like an open switch.

IV Reverse Active: In this condition, the base-emitter junction is reverse biased, whereas the base-collector junction is forward biased. As the collector is not doped to the extent as the emitter is therefore, it cannot supply (emit) as many majority carriers to the base. Hence, in this case very poor transistor action is achieved.

Q.59 Sketch the CE-configuration transistor output characteristics of a transistor and explain thesignificance of these curves. Indicate the active, cut-off and saturation regions. Marks (7)

Ans: **Output Characteristics of a Transistor in CE-Configuration:** In CE configuration, the curve plotted between collector current I_C and collector-emitter voltage V_{CE} at constant base current I_B is called output characteristic, shown in fig. 59.1.

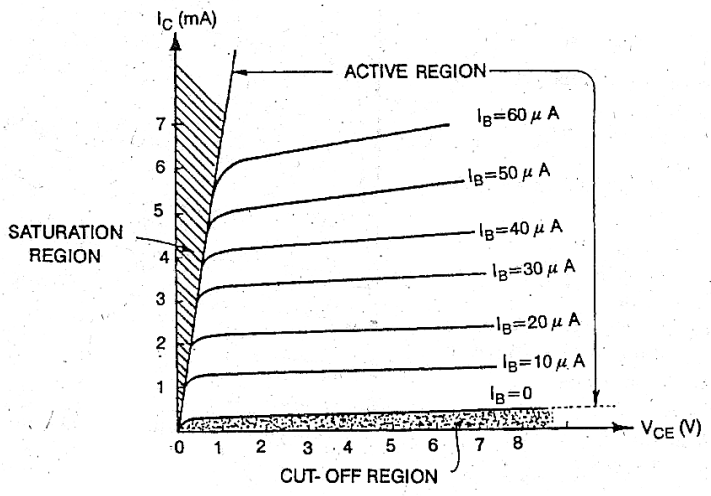


Fig. 59.1

(i) In the active region, Ic increases slightly as V_{CE} increases. The slope of the curve is little bit more than the characteristics of CB configuration. Hence, the output resistance (r_o) of this configuration is less as compared to CB configuration.

(ii) Since the value of I_C increases with the increase in V_{CE} at constant I_B, the value of β also increases $\left(\because \beta = \frac{I_C}{I_B} \right)$

(iii) When V_{CE} falls below the value of V_{BE} (i.e. below a few tenths of a volt.), I_c decreas rapidly. In fact, at this stage, the collector-base junction is also forward biased and the transistor works in saturation region, where I_c becomes independent of input current I_B.
(iv) In the active region, $I_c = \beta I_b$, hence a small change in base-current I_B produces a large change in output current (I_C)
(v) When the input current $I_B = 0$, the collector current I_C is not zero but its value is equal to the reverse leakage current I_{CEO} (i.e. collector emitter current when base is open).

Q.60 Prove that in a transistor operating in CE-configuration, the active region, collector current I_C is given by $I_C = \beta I_B + (\beta + 1) I_{CO}$ **Marks (3)**

Ans: **Proof:** In CE configuration, the input current is IB and the output current IC. These currents are related by the equations:

$I_E = I_B + I_C$ and $I_C = \alpha I_E + I_{CBO} = \alpha (I_B + I_C) + I_{CBO}$

Or $I_C (1 - \alpha) = \alpha I_B + I_{CBO}$ $\quad I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$

In CE configuration, if the base circuit is open (i.e., $I_B = 0$), the collector current will be the current to the emitter. This current is abbreviated as I_{CEO} that means collector-emitter current with base open.

Hence, $$I_{CEO} = \frac{1}{(1-\alpha)} I_{CBO} = (\beta + 1) I_{CBO} \left[\because \frac{1}{1-\alpha} = \beta + 1 \right]$$

and the basic current amplification factor β in terms of α is given by the equation

$$\beta = \frac{\alpha}{1-\alpha}$$

By substituting these values in the above equation, we get total collector current as

$I_C = \beta I_B + (\beta + 1) I_{CBO}$ **Hence Proved**.

Q.61 Define the three FET parameters g_m, r_d and μ. Prove that $\mu = g_m \times r_d$ **Marks (5)**

Ans: **FET Parameter:**

Transconductacce: It is defined as the ratio of change in drain current to the change in gate-source voltage at constant drain-source voltage and is denoted by g_m. Thus,

Transconductance, $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ at constant V_{DS}

AC Drain Resistance: It is defined as the ratio of change in drain-source voltage to change in drain current at constant gate-source voltage and is denoted by r_d.

Thus, AC drain resistance, $r_d = \frac{\Delta V_{DS}}{\Delta I_D}$ at constant V_{GS}

Amplification Factor (μ): It is defined as the ratio of change in drain-source voltage to the change in gate-source voltage at constant drain current and is denoted by μ.

Thus, Amplification Factor, $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$ at constant I_D

Proof: Amplification Factor is given by $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$

$$= \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$=r_d \times g_m$

=AC drain resistance X transconductance

Hence Proved

Q.62 Describe briefly the construction of a MOSFET in enhancement mode. Draw its characteristics. Marks (7)

Ans: **Construction of an N-Channel Enhancement MOSFET:** The fig.62.1 shows the construction of an N-channel E-MOSFET. It consists of a highly doped P-type substrate into which two blocks of heavily doped N-type material are diffused forming the source and drain. The type of impurity for the channel is the same as for the source and drain.

Now a thin layer of Sio_2 dielectric is grown over the entire surface and holes are cut through the Sio_2 (silicon-dioxide) layer to make contact with the N-type blocks (Source and Drain.). Metal is deposited through the holes to provide drain and source terminals. This layer constitutes the gate. Sio_2 layer results in an extremely high input impedance of the order of 10^{10} to 10^{15} ohms for this area.

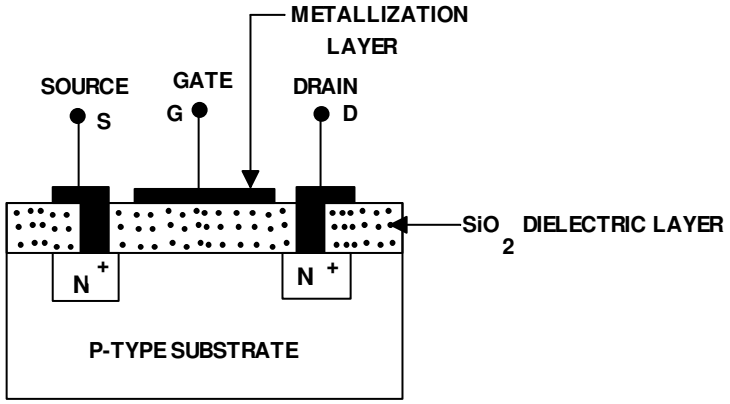
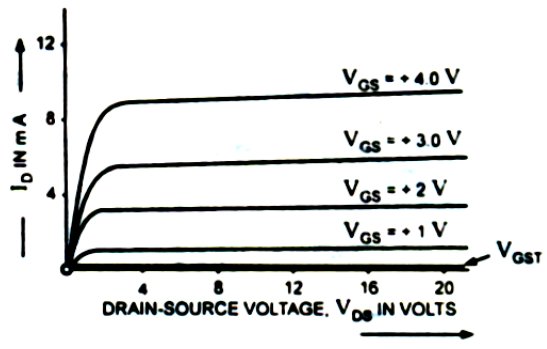
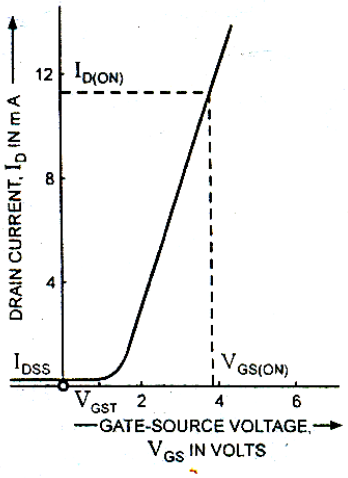


Fig. 62.1 N-CHANNEL E-MOSFET STRUCTURE

Characteristics of enhancement mode MOSFET



Drain Characteristics



Transfer Characteristic

Q.63 Explain how FET can be used as a switch. Marks (2)

Ans: **FET as a Switch:** When a voltage V_{DS} is applied across the drain and source terminals and voltage applied across the gate and source voltage V_{GS} is zero (i.e., gate circuit is open), the two pn junctions establish a very thin depletion layer. Thus a large amount of electrons will flow from source to drain through a wide channel between the two depletion layers. In this condition FET acts like a closed switch. When a reverse voltage V_{GS} is applied across the gate and source, the width of the depletion layer is increased. This reduces the width of the conducting channel thereby decreasing the conduction through it. At a sufficiently large reverse voltage, depletion width increases enough to cutoff two ends of the channel. In this condition, the FET acts like an open switch.

Q.64 Give the basic structure and working of an SCR. Marks (6)

Ans: **Constructional Features of Silicon Controlled Rectifier (SCR):** An SCR is a pnpn semiconductor device consisting of three pn junctions J_1,J_2,J_3 as shown in fig.64.1 is as if an ordinary diode (PN) and a transistor (NPN) are combined in one unit. Three terminals are taken; one from the outer P-type material called Anode (A), second from the outer N-type material called Cathode (K) and the third from the other P-type material placed in between placed in between and called Gate (G).

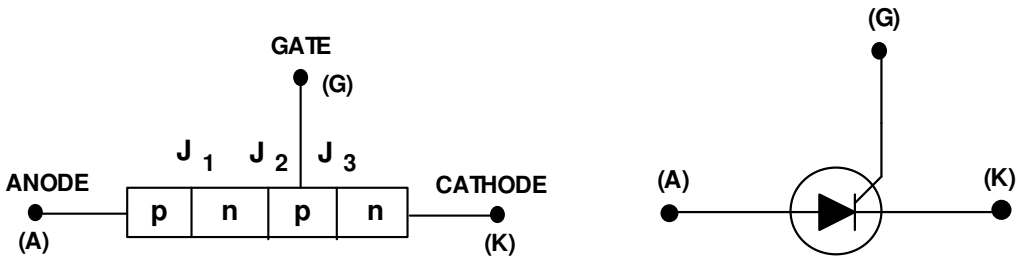


Fig. 64.1

Working of an SCR:

Action of Anode voltage: An SCR circuit shown in fig. 64.2 where anode is made positive w.r.t. cathode and the gate voltage is kept at zero. With the application of this voltage, the junctions J_1 and J_3 are forward biased, whereas junction J_2 is reverse biased. Hence, the flow of current in the circuit is blocked i.e. SCR is cut off. However, if anode to cathode voltage V is increased, a stage is reached when breakdown of junction J_2 occurs and the SCR suddenly switches to highly conducting state. In this state, the load current is only limited by supply voltage V and load R_L.

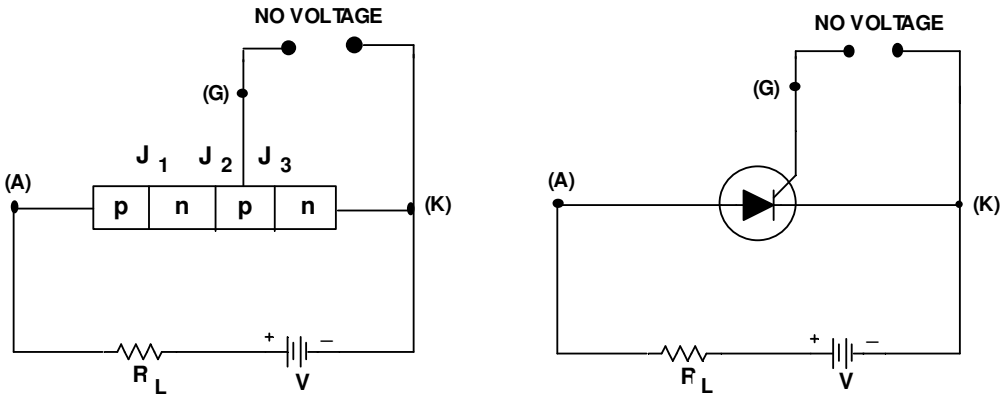


Fig.64.2

If the anode is made negative w.r.t. cathode and the gate voltage is kept at zero, junction J_1 and J_3 are reverse biased, whereas junction J_2 is forward biased. Under such conditions, the SCR does not conduct current i.e. it remains in cut off position. However, if this reverse voltage is increased, a stage reaches when breakdown of junction J_1 and J_3 occurs and SCR is turned to highly conducting state.

Action of Gate Voltage: Consider the SCR circuit shown in fig. 64.3, where anode is positive w.r.t. cathode. Let us suppose that anode voltage V is less than forward breakdown voltage, so that SCR does not conduct. If now a small positive voltage is applied to the gate, the gate current I_g starts flowing in the gate circuit. The flow of gate current helps in making current flow across junction J_2 i.e., in breaking it down. This switches the SCR to highly conducting state at the anode voltage which is quite less than forward breakdown voltage. Hence, gate voltage has the ability to trigger the SCR at a low value of anode voltage, but its all control on the SCR current after triggering. Therefore, in order to turn the SCR to OFF position, the anode voltage has to be reduced to zero.

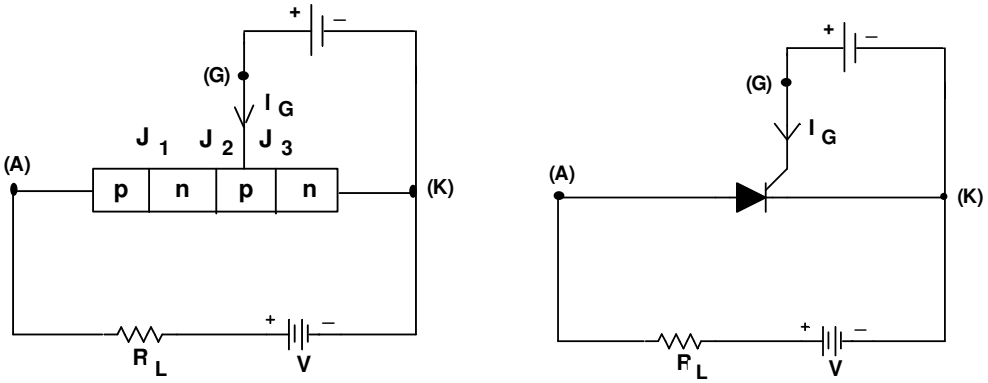


Fig. 64.3

Q.65 Draw and discuss its volt-ampere characteristics. Marks (5)

Ans: **V-I Characteristics of an SCR:** The V-I characteristics of an SCR is shown in fig. 65.1

Forward Characteristics: The curve between V and I when forward voltage (i.e., anode is positive w.r.t.cathode) is applied is known as Forward Characteristics of an SCR.

When gate current is zero: As power supply voltage is increased from zero (with zero gate current), there is a small leakage current which flows through anode. This is due to leakage of minority carriers through junction J_2. This small leakage current does not affect the load at all and for all practical purposes, the load is considered to be OFF i.e. SCR is said to be in OFF state.Now, when the power supply voltage, which is equal to voltage drop across anode and cathode of SCR (as there is little voltage drop across load on account of extremely small value of leakage current), reaches the forward break over voltage, SCR at once begins to conduct and the voltage V across thyristor suddenly drops as shown by dotted curve AB as shown in fig.65.1. Full conduction is reached rapidly. Under such conditions most of power supply voltage appears across the load, as drop across thyristor is hardly 1 V as compared to several hundred volts across load.
The SCR now acts as truly closed switch, allowing power to flow through the load circuit. It will continue to flow as long as holding current for thyristor is maintained.

When gate current flows: The above considerations apply for zero gate current i.e., when gate circuit is open. However, when a small gate voltage is applied, the gate current starts flowing. The flow of gate current helps in making current flow across junction J_2 i.e., in breaking it down. Due to high positive potential on the anode side of the junction, electrons in n-type material virtually pulled into p-type. Similarly, holes in p-type are pulled across J_2 into n-type material by the negative potential on right side of J_2.

Reverse Characteristics: When anode is connected to negative and cathode to positive of power supply, the curve between V and I is called reverse characteristic shown in fig. 65.1. In this case, junctions J_1 and J_3 are reverse biased while J_2 is forward biased. It is clear that by increasing the reverse voltage beyond a certain value (point D) will result in the breakdown of the junctions J_1 J_2 and SCRs can no longer block the flow of current through it. However, this voltage is very high as compared to the forward voltage.

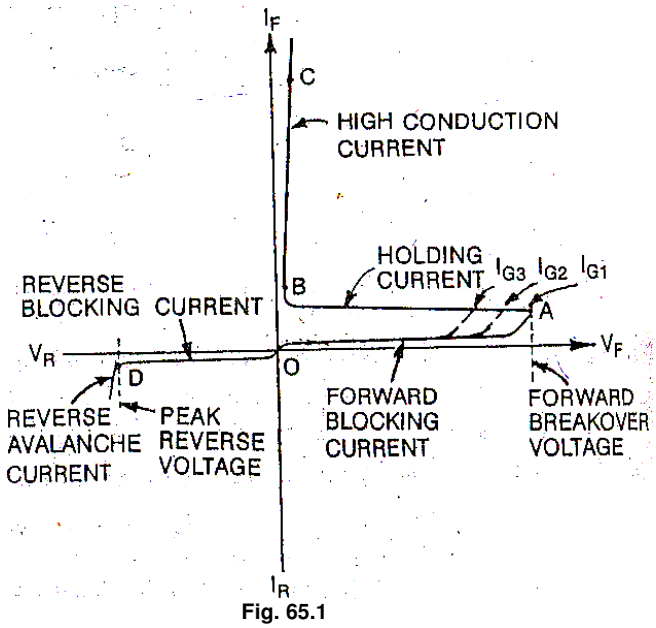


Fig. 65.1

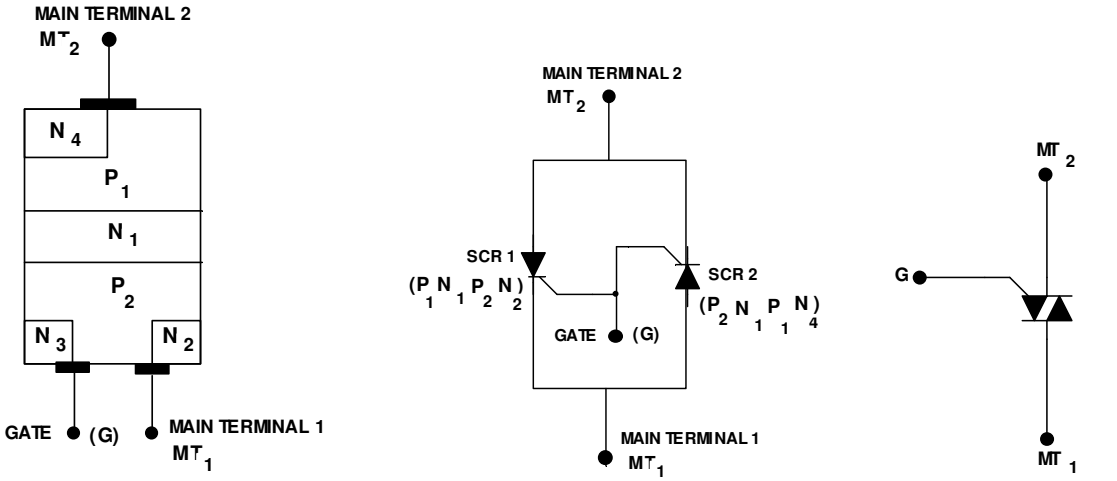
Q.66 What are the applications of SCR ? **Marks (3)**

Ans: **Applications of SCR:**

(i) It is used as Half-Wave and Full-Wave Controlled Rectifier
(ii) It is used as a Static Contactor
(iii) Use of SCR for Speed Control of DC Shunt Motors
(iv) SCRs are used in Static AC Circuit Breaker and Static DC circuit Breaker as a switch
(v)SCRs are used in zero voltage switching
(vi)Used in Over-Voltage Protection
(vii)Used in Pulse Circuits
(viii)Used in Battery Charging Regulator.

Q.67 Describe the basic structure of TRIAC. Draw and discuss its volt-ampere characteristics. **Marks (5)**

Ans **Basic Structure of TRIAC:** A triac shown in fig.67. basically consists of two SCRs connected in inverse parallel with gate common. In external appearance, the triac is similar to an SCR, but triac is bi-directional device. The internal layers and doping are arranged so that current can flow in either direction. The gate terminal G makes ohmic contacts with both the N and P materials. This permits trigger pulse of either polarity to start conduction. Since the triac is a bilateral device, the term "anode" and 'cathode' has no meaning, and therefore, terminals are designated as Main Terminal 1 (MT1) and main terminal 2 (MT2) and gate G.



(a) Basic Structure **(b) Electrical Equivalent Circuit** **(c) Schematic Symbol**

Fig.67 TRIAC

V-I Characteristics of TRIAC: Typical V-I characteristics of a triac are shown in fig.67.4. The triac has on and off characteristics similar to SCR but the characteristic is applicable to both positive and negative voltages. Because triac consists of two SCRs connected in parallel but opposite in directions.

Forward Characteristics:

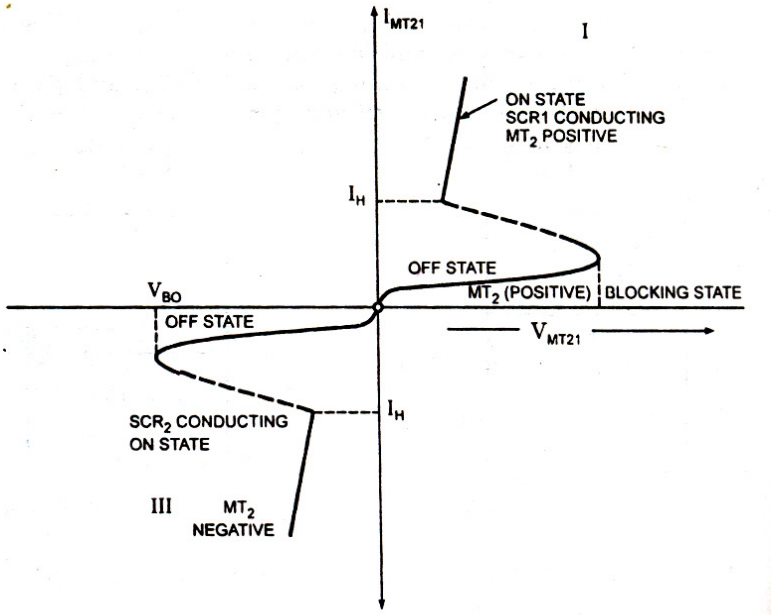
Terminal MT2 and gate are positive with respect to terminal MT1: When terminal MT2 is positive with respect to terminal MT1. The two junctions P_1-N_1(1^{st} diode) and P_2-N_2(3^{rd} diode) are forward, whereas junction N_1-P_2(2^{nd} diode) is reverse biased. So there is a blockage of current flow across the triac. This state is called Blocking State. When a small positive gate voltage (G_1) is applied to the P_2 -terminal of second diode, the gate

current starts flowing. The flow of gate current helps in making current flow across t junction J_2 i.e., in breaking it down. Triac at once begins to conduct and the voltage V across SCR1 suddenly drops. Full conduction is reached rapidly. Under such conditions, most of power supply voltage appears across load. The SCR1 is a truly closed switch, allowing power to flow through the load circuit

Reverse Characteristics:

Terminal MT2 and gate is Negative with respect to terminal MT1: When terminal MT2 is Negative w.r.t. terminal MT1, the two junctions J_1 (P_2-N_1) and J_3 (P_1-N_4) are forward biased, whereas junction J_2 (N_1-P_1) is blocked. So there is blockage of current flow across the SCR2.

This state is called Blocking Stage. When a small negative gate voltage (G_2) is applied to the N1 terminal of second diode, the gate current starts flowing. The flow of gate current helps in making current flow across the junction J_2.i.e. in breaking it down. This state is called Conducting state. As soon as the SCR2 begins to conduct, the voltage V across SCR2 is hardly –1V as compared to several hundred volts across the load. The SCR2 now acts as a truly closed switch, allowing power to flow through the load circuit.



V-I Characteristic of a Triac

Fig. 67 .4

Q.68. What is an IC ? What are its special features ? Why is it so commonly used in electronic circuits ? Marks (5)

Ans: **Integrated Circuit (IC):** It is a complete electronic circuit consisting of both the active and passive components (including their interconnections) fabricated on an extremely tiny single chip of silicon.

Special Features of ICs:

(i) No component of an integrated circuit can be removed or replaced since all the components are the integral part of a small semiconductor chip.

(ii) No component of an integrated circuit is projected above the surface of the chip since they are formed within the chip.

(iii) The size of an IC is extremely small and once needs a microscope to see the connections between the components.

(iv) In IC technology, all the circuit elements (transistors, diodes, resistors, capacito etc.) including their interconnections are fabricated at the same time.

ICs are commonly used because of following advantages

(i) Extremely small-thousands times smaller than discrete circuit.
(ii) Very small weight owing to miniaturized circuit.
(iii) Very low cost because of simultaneous production of hundred of similar circuits on a small semiconductor wafer.
(iv) More reliable because of elimination of soldered joints and need for fewer inter-connections.
(v) Low power consumption because of their smaller size.
(vi) Easy replacement as it is more economical to replace them and repair is not possible.
(vii) Increased operating speeds because of absence of parasitic capacitance
(viii) Improved functional performance as more complex circuits can be fabricated for achieving better characteristics.

Q.69 Describe the various steps in the fabrication of a typical monolithic integrated circuit. Marks (4)

Ans: **Various steps in the fabrication of a typical monolithic IC:**

Step 1. A part of SiO_2 layer is etched off by a photolithographic etching process, exposing the epitaxial layer as shown in below fig.69(i)a. The remaining SiO_2 layer serves as a mask for the diffusion. The wafer is then put into a furnace for the diffusion of acceptor (trivalent) impurities (in this case, boron) onto the epitaxial layer. The acceptor impurities change the exposed epitaxial layer from n-type semiconductor into p-type semiconductor. The process continuous till p-type impurities reach the p-type substrate. This forms an island of n-type material under SiO_2 layer as shown in fig.69(i)b

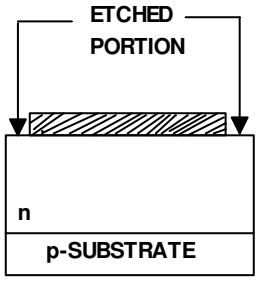


Fig.69(i) a

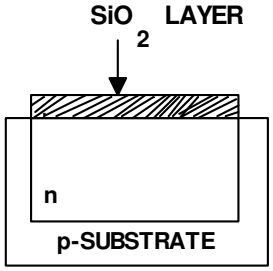


Fig.69(i) b

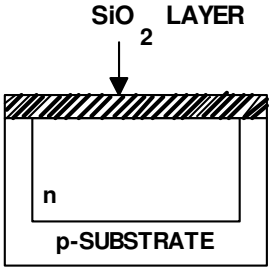


Fig.69(i) c

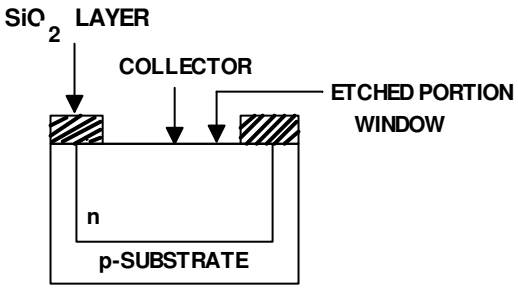


Fig.69(i) d

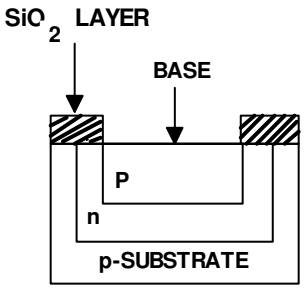


Fig.69(i) e

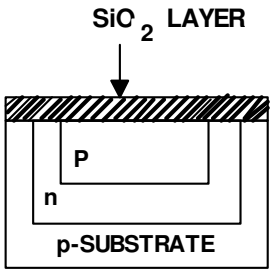


Fig.69(i) f

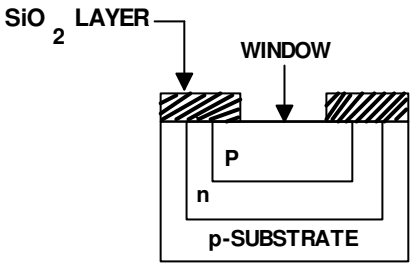


Fig.69(i) g

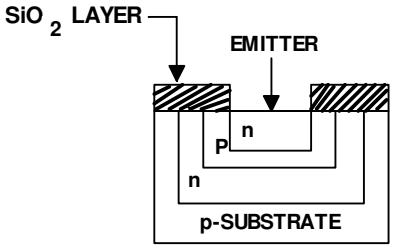


Fig.69(i) h

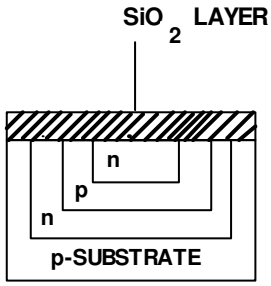


Fig.69(i) i

Step 2. Thereafter pure oxygen is passed over the wafer to form to complete silicon dioxide (SiO_2) layer as shown in fig.69(i)c

Step 3. Then, a hole is etched off at the center of the SiO_2 layer exposing the epitaxial layer as shown in fig.69(i)d

Step 4. The wafer is again (for the second time) put into the furnace for the diffusion of acceptor impurities onto the epitaxial layer exposed for the diffusion. The process continuous till we get an island of p-type material as shown in fig.69(i)e

Step 5. Again, for the second time, pure oxygen is passed over the wafer to form a complete layer of silicon dioxide (SiO_2) as shown in fig.69(i)f

Step 6. Thereafter, a small hole (called window) is etched off at the center of the SiO_2 layer exposing the p-type epitomical layer as shown in fig.69(i)g

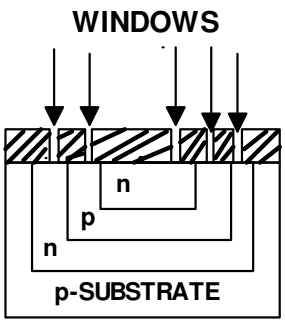


Fig.69(ii)a

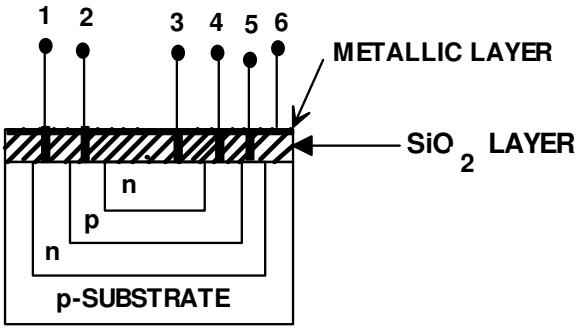


Fig.69(ii)b

Step 7. The wafer is again (for the third time) put into the furnace for the diffusion of donor (pentavalent) impurities (phosphorus) onto the p-type epitaxial layer exposed for

diffusion. The process continuous till we get as island of n-type material as shown fig.69(i)h

Step 8. For the last time, pure oxygen is passed over the wafer to form a complete insulating layer of silicon dioxide (SiO_2) as shown in fig.69(i)i

Step 9. For the formation of various components and their interconnection, the newly formed SiO_2 layer is again etched off at various points. This exposes the different epitaxial layer shown in fig.69(ii)a. A thin film of metal, such as aluminium, is evaporated over the wafer as shown in fig.69(ii)b. The newly formed windows are filled in with metal making connections to various epitaxial layers.

Step 10. For the formation of various components and their interconnection, the regions of the metallic layer not needed are etched off.

Q.70 List the main characteristics of an ideal Op-amp. Marks (4)

Ans: **Characteristics of an ideal Operational Amplifier:**

(i) Infinite voltage gain A

(ii) Infinite input resistance R_i so that almost any signal source can drive it and there is no loading of the preceding stage.

(iii) Zero output resistance R_o, so that output can drive an infinite number of other devices.

(iv) Zero output voltage when input voltage is zero.

(v) Infinite bandwidth so that any frequency signals from 0 to $\propto$ HZ can be amplified without attenuation.

(vi) Infinite common-mode rejection ration, so that the output common-mode noise voltage is zero.

(vii) Infinite slew rate so that output voltage changes occur simultaneously with input voltage changes.

Q.71 Describe how an Op-amp may be used as Marks(4)

(i) Voltage to current converter.
(ii) Current to voltage converter.
(iii) an integrator.
(iv) a differentiator.

Ans: **(i)** **Voltage to Current Converter**: Fig.71(a) shows a voltage-to-current converter in which load resistor R_L is floating (not connected to ground). The input voltage is applied to the non-inverting input terminal, and the feedback voltage across R_1 drives the inverting input terminal. This circuit is also called a current-series negative feedback amplifier because the feedback voltage across R_1 (applied to the inverting terminal) depends on the output current i_o and is in series with the input difference voltage v_{id}.

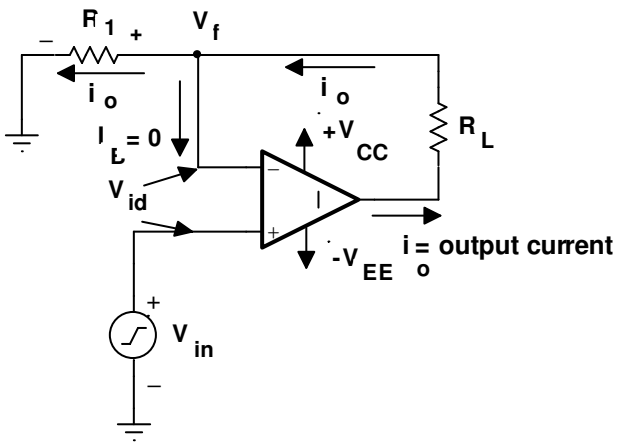


Fig.71(a)

Writing Kirchhoff's voltage equation for the input loop,

$V_{in} = V_{id} + V_f$

But $v_{id} \approx 0$ V, since A is very large in an ideal op-amp; therefore,

$V_{in} = V_f$

$v_{in} = R_1 i_o$ or $i_o = \frac{v_{in}}{R_1}$

This means that in the above circuit, an input voltage v_{in} is converted into an output current of v_{in}/R_1.

(ii) Current-to-Voltage Converter:

The basic inverting operational amplifier is used as current-to-voltage converter which is shown in fig.71(b)

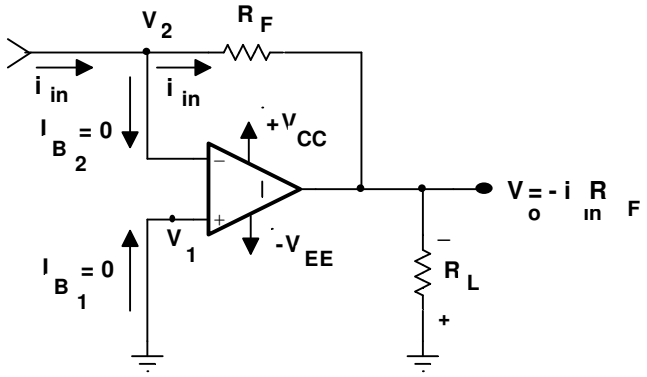


Fig.71(b)

From basic fundamentals, the ideal voltage –gain of the inverting operational amplifier is

Given by $A_v = \frac{v_o}{v_{in}} = -\frac{R_F}{R_1}$

Therefore, $$v_o = -\left(\frac{v_{in}}{R_1}\right)R_F$$

However, in an ideal operational op-amp since, v1 = 0 V and $v_1 = v_2$.

$$\frac{v_{in}}{R_1} = i_{in}$$

By substituting the this value in the equation of output voltage (v_o), we get

$$v_o = -i_{in}R_F$$

So, the above equation shows that the output voltage v_o becomes proportional to the input current i_{in}.

(iii) **Op-amp as an Integrator:** A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator or the integration amplifier. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_F is replaced by a capacitor C_F as shown in fig.71(c)

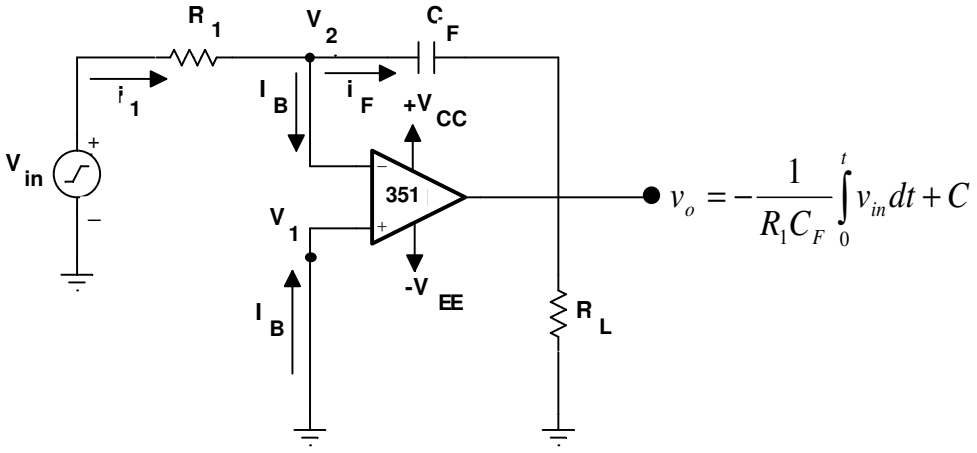


Fig.71(c)

The expression for the output voltage v_o can be obtained by writing Kirchoff's current equation at node v_2 i.e. $i_1 = I_B + i_F$

Since I_B is negligibly small, $i_1 \approx i_F$

The relationship between current through and voltage across the capacitor is given by

$$i_c = C\frac{dv_c}{dt}$$

Therefore,

$$\frac{v_{in} - v_2}{R_1} = C_F\left(\frac{d}{dt}\right)(v_2 - v_o)$$

However, in an ideal op-amp $v_1 = v_2 \approx 0$ because A is very large. Therefore,

$$\frac{v_{in}}{R_1} = C_F\left(\frac{d}{dt}\right)(-v_o)$$

The output voltage can be obtained by integrating both sides with respect to time

i.e. $$\int_0^t \frac{v_{in}}{R_1}dt = \int_0^t C_F \frac{d}{dt}(-v_o)dt$$

$$= C_F(-vo) + vo\big|_{t=0}$$

Therefore, $$v_o = -\frac{1}{R_1 C_F}\int_0^t v_{in}dt + C$$

Where C is the integration constant and is proportional to the value of the output voltagev_o at time t = 0 seconds the above equation indicates that the output voltage is directly proportional to the negative integral of the input voltage and inversely proportional to the time constant R.

(iv) Fig.11(e) shows the differentiator or differentiation amplifier. As its name implies, the circuit performs the mathematical operation of differentiation; that is, the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier, if an input resistor R_1 is replaced by a capacitor C_1.

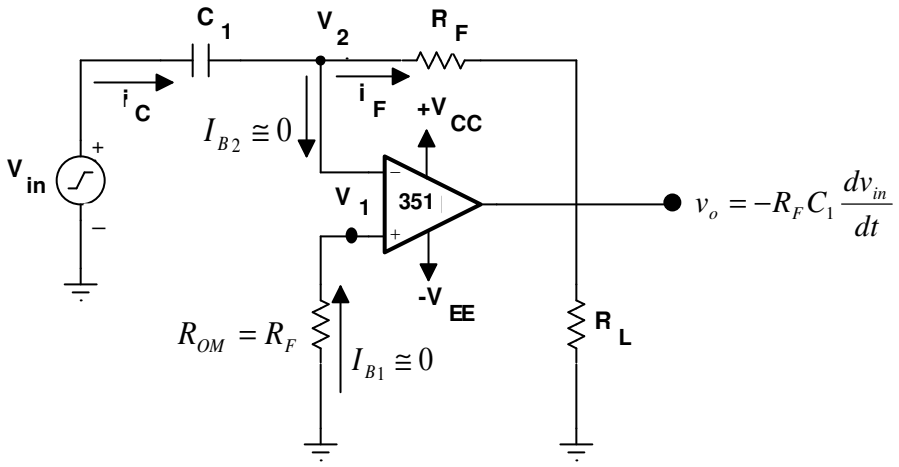


Fig.71 (d)

The expression for the output voltage can be obtained from Kirchoff's current equation written at node v_2 as follows:

$$i_C = i_B + i_F$$

Since $I_{B \cong 0}$, $i_C = i_F$

$$C_1 \frac{d}{dt}(v_{in} - v_2) = \frac{v_2 - v_o}{R_F}$$

But $v_1 = v_2 \cong 0$ V, because A is very large. Therefore, $C_1 \frac{dv_{in}}{dt} = -\frac{v_o}{R_F}$

$$v_o = -R_F C_1 \frac{dv_{in}}{dt}$$

Thus the output v_o is equal to the $R_F C_1$ times the negative instantaneous rate of change of the input voltage v_{in} with time.

Q.72 Explain the conduction of current in a good conductor. Why does a conductor has low resistance ? Marks (7)

Ans: **Conduction of current in a good conductor:** The substances (like copper, aluminum, silver etc.) which allow the passage of current through them are known as conductors. In case of conducting materials, there is no forbidden energy gap (i.e., the energy gap between valence band and conduction band) and the valence and conduction bands overlap, as shown in fig.72.1

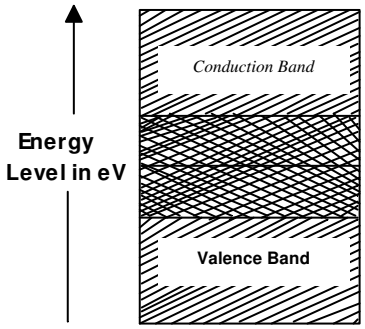


Fig.72.1

The orbits in the conduction band are very large. An electron in the conduction band experiences almost negligible nuclear attraction. In fact, an electron in the conduction band does not belong to any particular atom. But it moves randomly throughout the solid. This is the reason that electrons in the conduction band are called the free electrons. Due to overlapping of valence and conduction bands, a slight potential difference across the conductor causes the free electrons to constitute heavy flow of electric current through them. Conductor has low resistance, because its valence and conduction band overlaps. So, its conductivity becomes high.

Q.73 What is intrinsic semiconductor. How do we make it extrinsic semiconductor, and why so ? Marks (7)

Ans: **Intrinsic Semiconductor:** An intrinsic semiconductor is one which is made of the semiconductor material in its extremely pure form.

Making of Extrinsic Semiconductor from Intrinsic Semiconductor: Although an intrinsic semiconductor is capable to conduct a little current even at room temperature but as it is, it is not useful for the preparation of various electronic devices. However, the electrical conductivity of intrinsic semiconductor can be increased many times by adding very small amount of impurity (of the order of one atom per million atoms of pure semiconductor) to it in the process of crystallization. This process is called doping and the doped material is called impurity or extrinsic semiconductor.

The purpose of adding impurity in the semiconductor crystal is to increase the number of free electrons or holes to make it conductive. If a small amount of pentavalent impurity (having 5 valence electrons), such as arsenic, antimony, bismuth or phosphorus etc. are added to a pure semiconductor a large number of free electrons will exist in it and it is called N-type (donor type) extrinsic semiconductor. If a small amount of trivalent impurity (having 3 valence electrons), such as boron, gallium, indium or aluminium etc.

are added to a pure semiconductor, a large number of holes will exist in it and it is cal the P-type (acceptor) semiconductor.

Q.74 Explain the Zener and Avalanche effects. Give differences between them. **Marks (7)**

Ans: **Avalanche Breakdown:** The minority carriers, under reverse biased conditions, flowing through the junction acquire a kinetic energy which increases with the increase in reverse voltage. At a sufficiently high reverse voltage (say 5v or more), the kinetic energy of minority carriers becomes so large that they knock out electrons from the covalent bonds of the semiconductor material.

As a result of collision, the liberated electrons in turn liberate more electrons and the current becomes very large leading the breakdown of the crystal structure itself. This phenomenon is called Avalanche Breakdown.

Zener Breakdown: Under a very high reverse voltage, the depletion region expands and the potential barrier increases leading to a very high electric field ($3X10^7$ V/m) across the junction. The electric field will break some of the covalent bonds of the semiconductor atoms leading to a large number of free minority carriers, which suddenly increases the reverse current. This is called the Zener effect. The breakdown occurs at a particular and constant value of reverse voltage called the breakdown voltage.

Differences between Zener and Avalanche Breakdown:

(i) Diode junctions that breakdown below 5 V are caused by Zener effect whereas Junctions that experience breakdown above 5 V are caused by Avalanche effect.

(ii) The Zener breakdown occurs in heavily doped junctions (P-type semiconductor moderately doped and N-type heavily doped), which produce Narrow depletion layers, whereas Avalanche breakdown occurs in lightly doped junctions, which produce wide depletion layers.

(iii) With the increase in junction temperature, Zener breakdown voltage is reduced while the Avalanche breakdown voltage is increases.

(iv) The zener diodes have a negative temperature coefficient while Avalanche diodes have a positive temperature coefficient.

Q.75 With the help of a neat diagram, explain the operation of a Bridge Rectifier. What is PIV for the diode used here **Marks (7)**

Ans: **Operation of a Full-Wave Bridge Rectifier:** Fig (75.1) shows the circuit of a Full-Wave Bridge Rectifier. The circuit consists of four diodes D_1, D_2, D_3 and D_4 connected to form a bridge. When a.c. supply is switched on, the alternating voltage V_{in} appears across the terminals AB of secondary winding of transformer.

During positive half cycle of secondary voltage, the end A becomes positive and end B is negative (see fig.75.3). This makes diodes D_1 and D_3 forward biased and diodes D_2 and D4 reverse biased. Therefore, diodes D_1 and D_3 conduct while diodes D_2 and D_4 do not conduct. Thus, current (I) flows through diode D_1, load resistor R_L (from M to L), diode D3 and the transformer secondary as shown in fig (75.3). The wave shape of current through R_L is shown in fig.75.2. (b)

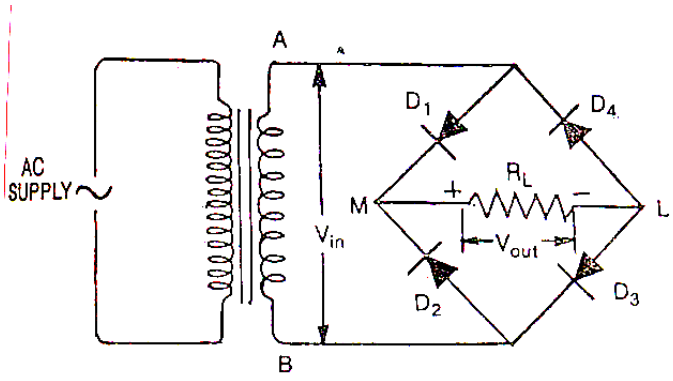


Fig. (75.1)

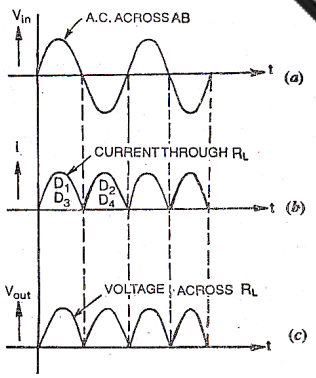


Fig. (75.2)

During negative half cycle, the end A becomes negative and end B positive (see Fig. (75.4). This brings diodes D_2 and D_4 under forward bias and diodes D1 and D3 under reverse bias. Therefore, diodes D_2 and D_4 conduct while diodes D_1 and D_3 do not. Thus, current (i) flows through diode D2, load resistor R_L (from M to L), diode D4 and the transformer secondary as shown in fig. (75.4). The wave shape of current is shown in fig.75.2 (b)

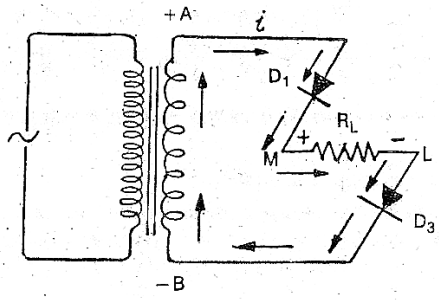


Fig.(75.3)

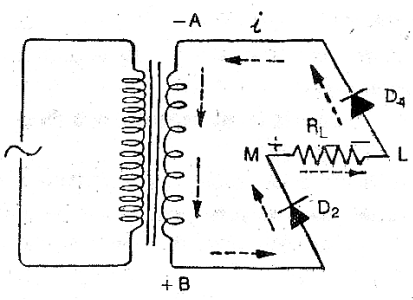


Fig (75.4)

The current flowing through load resistor R_L is in the same direction (M to L) during both the half cycles. Hence, rectified output voltage V_{out} is obtained across the load resistor R_L. The wave shape of output voltage is shown in fig.75.2(c)

Peak Inverse Voltage: The maximum possible value of reverse bias voltage coming across the diode is called the Peak Inverse Voltage.

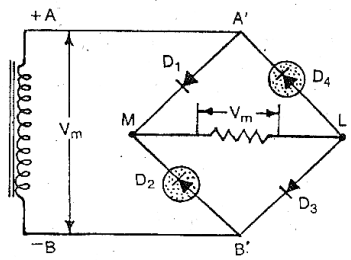


Fig (75.5)

Fig (75.5) shows the instant when secondary voltage attains its maximum value and terminal A is positive and B is negative. At this instant, diodes D_1 and D_3 are forward biased and conducting current. Therefore, terminal M attains the same voltage as that of A' or A whereas, L attains the same voltage as that of B' or B. Hence, the diode D_2 and D_4 are reverse biased and the voltage across both of the diodes is V_m

Thus, the P.I.V. required for diodes in a Bridge Rectifier is at least Vm.

$$P.I.V = V_m$$

Q.76 Explain the functioning of a capacitor filter used with the rectifiers. Marks (

Ans: **Function of a Capacitor Filter used with the Rectifiers:** A Shunt Capacitor filter is shown in fig. 76.1 In this case, a capacitor C of large value is connected in parallel with the load resistance and hence the name Shunt Capacitor Filter. The capacitor offers a low reactance path to a.c. component and allows it to pass through but it acts as an open circuit to d.c. component. Hence, all the d.c.current passes through the load.

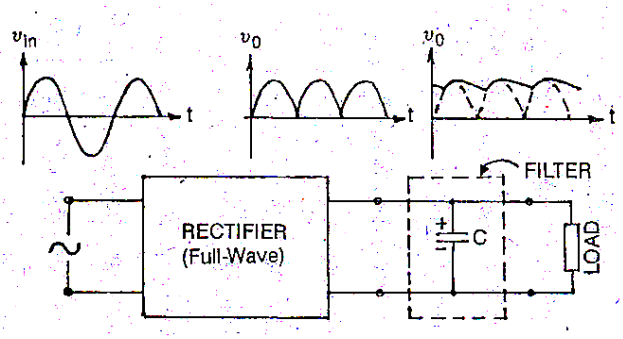


Fig.76.1

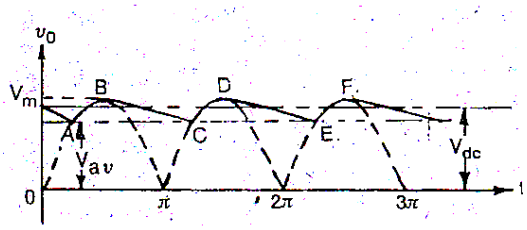


Fig.76.2

Working: The working of a shunt capacitor filter can be explained with the help of a wave diagram shown in Fig.76.2. The dotted pulsating wave shows the output of a full-wave rectifier. When the rectifier voltage is increasing, the capacitor is charged to $+V_m$ (see curve AB). At point B, the rectifier voltage tries to fall but the charged capacitor immediately tries to send the current back to the rectifier. In this process, the rectifier diodes are reverse biased and stop giving supply to the load. Thus, the capacitor discharges (B to C) through the load. The capacitor continues to discharge until the source voltage (the dotted curve) becomes more than the capacitor voltage (point C). The diode starts conducting and the capacitor is again charged to peak value $+V_m$ (point D). During this time (C to D), the rectifier supplies the charging current i_c and load current i_L. So, capacitor not only removes the a.c. component from the output but it also improves the output voltage. The smoothness and magnitude of output voltage depends upon the time constant CR_L. The longer the time period, the steadier is the output voltage. This can be achieved by using a large value of capacitor.

Q.77 Define static and dynamic resistances for a diode. What are its uses ? Marks (7)

Ans: **(i) Static or D.C. Forward Resistance:** The opposition offered by a diode to the direct current flow in forward bias condition is known as d.c. forward resistance. It is measured by taking the ratio of d.c. voltage across the diode to the d.c. current flowing through it. Refer to the characteristic of a diode shown in fig 77.1, for operating point P, the forward voltage is OA and the corresponding forward current is OB.

$$R_F = \frac{OA}{OB}$$

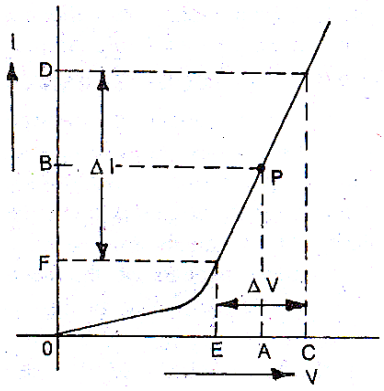


Fig.77.1

(ii) Dynamic or A.C. Forward Resistance: The opposition offered by a diode to the changing current flow in forward bias condition is known as its a.c forward resistance. It is measured by the ratio of change in voltage across diode to the resulting change in current through it. Refer to the forward characteristics of a diode shown in fig 77.b(1). For an operating P, the a.c forward resistance is determined by varying the forward voltage (CE) on both sides of operating point equally and measuring the corresponding forward current (DF).

$$r_f = \frac{CE}{DF} = \frac{\Delta V}{\Delta I}$$

Uses: Dynamic resistance of diode is useful in small signal amplifiers, while static resistance is useful when diode is used for large signals as in making a switch.

Q.78 Write short notes on any TWO of the following: Marks (2 X 7 =14)

(i) Differentiation between Passive and Active components.
(ii) IC resistors.
(iii) Op-amp as an Adder.

Ans: (i) Differentiation between Passive and Active Components:

Passive Components: The electronic components which are not capable of amplifying or processing an electrical signal are called passive components such as resistors, capacitors and inductors.

Resistor: Resistor is a component, used to limit the amount of current or divide the voltage in an electronic circuit. The ability of a resistor to oppose the current is called resistance. It receives the electrical energy from active components and converts it into heat. The unit of resistance R is ohm for which the symbol is Ω. The resistors are used in all electronic circuits. Symbols of resistor and variable resistor are shown in fig.78.1

RESISTOR VARIABLE RESISTOR

Fig. 78.1

Capacitors: The two conducting plates separated by an insulating material (called dielectric) forms a capacitor shown in fig. 78.2 the basic purpose of a capacitor is to store charge. The capacity of a capacitor to store charge per unit potential difference is called its capacitance. The unit of capacitance is farads (F). A capacitor is a component which offers low impedance to a.c. but very high impedance to d.c. Capacitors are used for coupling, bypassing and filtering.

CAPACITOR VARIABLE CAPACITOR

Fig. 78.2

Inductors: The electronic component (mostly a coil) which opposes the change of current in circuit is called an inductor. The ability of the coil or inductor due to which it opposes the change of current flowing through it is known as its inductance. The basic function of an inductor is, it receives the electrical energy from active components and stores in a magnetic field. The unit of inductance is henrys . An inductor is a component which offers high impedance to a.c. but very low impedance (opposition) to d.c. The symbols of inductor and variable inductor are shown in fig. 78.3

INDUCTOR VARIABLE INDUCTOR

Fig. 78.3

Active Components: The electronic components which are capable of amplifying or processing an electrical signal are called active components such as vacuum tubes, gas tubes and semiconductor (solid state) devices. Some examples are given below:

(i)Transistor (BJT): It is used as an amplifier and oscillator.

Fig. 78.4

(ii)Field-effect Transistor (FET): It is used as an amplifier and oscillator.

Fig. 78.5

(iii)Tube Devices:

Vacuum diode is used as rectifier and detector
Vacuum Triode is used as an amplifier and oscillator
Vacuum Pentode is used as an amplifier and oscillator

Vacuum Triode Vacuum Tetrode

Fig. 78.6

(iv)Diodes:

Junction diode: It is used as rectifier, detector and in switching circuits

Light Emitting Diode: It emits visible light and is used in instrument displays, digital watches, calculators etc.

Fig. 78.7

Ans.78(ii) **IC Resistors:** The IC resistors are of the following four types:

(i)Diffused Resistors
(ii) Pinch Resistors
(iii) Thin Film Resistors and
(iv) Thick Film Resistors.

Diffused Resistors: In IC resistors, the resistance value can be controlled by varying the concentration of doping impurity and depth of diffusion. The range of resistor values that may be produced by the diffusion process varies from ohms to hundreds of kilo-ohms. The typical tolerance, however, may be no better than ± 5 %, and may even be as high as ± 20 %. On the other hand, if all the resistors are diffused at the same time, then the tolerance ratio may be good. Most resistors are formed during the base diffusion of the integrated transistor as shown in fig. 78.8. This is because it is the highest resistivity region and diffused resistors are formed simultaneously with transistors, diodes and diffused capacitors. No additional steps in the manufacturing process are necessary. For low resistance values, emitter region is used as it has much lower resistivity.

Resistors for ICs can also be produced by using thin-film and thick film resistors. But these techniques require additional steps in the integrated circuit fabrication.. In this process, a metal film is deposited on a glass or S_iO_2 surface. The resistance value can be controlled by varying thickness, width and length of the film. Since diffused resistors can be processed while diffusing transistors, the diffusion technique is the cheapest and, therefore, the most widely used.

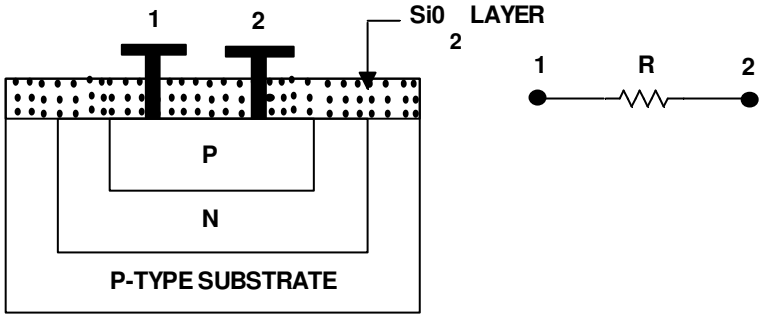


Fig. 78.8 IC Diffused Resistor

Ans.78(iii) **Summing Amplifier**: Fig. 78.9 shows the inverting summing amplifier. It is an inverting configuration with three inputs V_a, V_b and V_c. Depending on the relationship between the feedback resistor R_F and the input resistors R_a, R_b, and R_c, the circuit can be used as a summing amplifier.

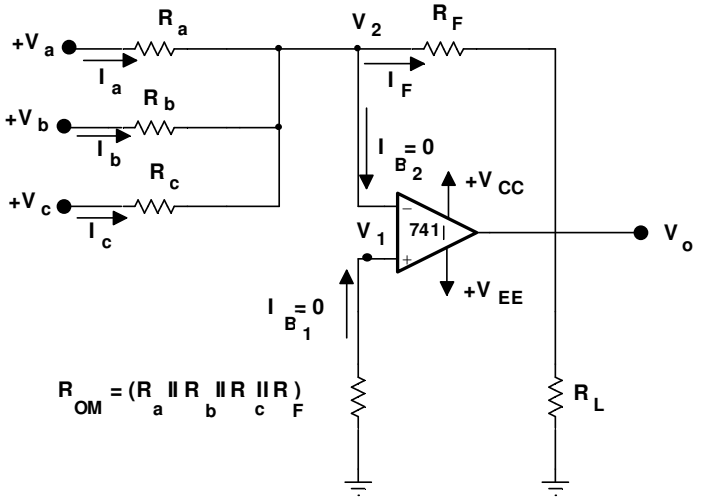


Fig. 78.9

The circuit's function can be verified by examining the expression for the output voltage V_o, which is obtained from Kirchhoff's current equation written at node V_2. Referring to the above fig, $I_a + I_b + I_c = I_B + I_F$

Since R_i and A of the op-amp are ideally infinity, $I_B = 0$ A and $V_1 = V_2 \cong 0$ V
Therefore,

$$\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c} = -\frac{V_o}{R_F}$$

or

$$V_o = -\left(\frac{R_F}{R_a}V_a + \frac{R_F}{R_b}V_b + \frac{R_F}{R_c}V_c\right)$$

If in the circuit above circuit, $R_a = R_b = R_c = R$, then the above equation can be written as

$$Vo = - (Va + Vb + Vc)$$

This means that the output voltage is equal to the negative sum of all the inputs times the gain of the circuit R_F/R; hence the circuit is called a summing amplifier, Obviously, when the gain of the circuit is 1, that is $R_a = R_b = R_c = R_F$, the output voltage is equal to the negative sum of all input voltages.

Q.79 Name the various types of emissions. Explain in detail the photoelectric emission. Marks (7)

Ans: **Types of Electron Emission:**
(i) Thermionic Emission
(ii) Secondary Emission
(iii) Photo-electric Emission
(iv) High-field Emission

Photo-Electric Emission: The emission of electrons from a metallic surface by the application of light energy is called Photo-electric emission.

When a beam of light strike at the surface of certain metals of low work funct such as potassium, sodium and cesium, the electrons may be emitted from their surface if the quantum of energy carried by the photons is equal to or greater than the work function of the metal. Such a phenomenon is termed as Photo-electric emission and the emitted electrons are known as Photoelectrons.

Operation: Photoelectric emission is utilized in photo tubes as shown in below fig. 79.1 The emitter E and anode A are enclosed in an evacuated glass envelope. The anode is connected to the positive terminal of the battery and emitter (cathode) is connected to the negative terminal. When light of suitable intensity and frequency supplied by the source S falls on the emitter, the photoemission starts from the emitter. These photoelectrons are attracted by the positive anode and constitute a current in the outer circuit. The current will exist in the circuit as long as suitable intensity and frequency of light falls on the emitter.

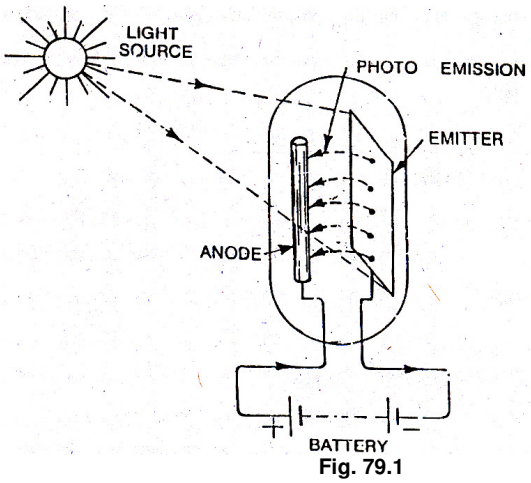


Fig. 79.1

The amount of photoelectric emission depends upon the intensity of light falling upon the emitter and the frequency of radiations. The amount of energy of a photon is given by the relation**:**

$$E = h f \text{ ------ (1)}$$

Where, E = the energy of photon in joules
h = Plank's constant in joules-second
f = frequency of photon in Hz.

A part of this energy is used in knocking out an electron from the metal surface and the rest of it appears as the kinetic energy of the emitted electron. Therefore,

$$E = hf = e\phi + \frac{1}{2}mv^2 \text{ -------(2)}$$

Where, e = electron charge (i.e. 1.602 x 10^{-19} C)
ϕ = work function of emitter in eV
m = mass of an electron (i.e. 9.106 x 10^{-31} kg)
v = velocity at which electron comes out of the surface in m/s

The expression (2) shows that the photoemission from a metal surface is possible only when the frequency of the incident light exceeds a certain threshold value. This is obtained by putting v = 0 in expression (2) i.e., $f_c = \frac{e\phi}{h}$ and the corresponding wavelength of the incident light is called threshold wave length,

i.e., $\lambda_C = \frac{ch}{e\phi}$ where, c = velocity of light.

Q.80 Explain the operation of a Liquid Crystal Display (LCD). Where are LCD's used ?
Marks (7)

Ans: **Operation of a Liquid Crystal Display (LCD):** An LCD does not radiate any illumination. It only reflects or transmits incidents illumination. Liquid crystal is organic fluid shaped like small cigars and sealed between two glass sheets having a transparent conducting surface. When a low frequency low voltage is applied, the crystal molecules rearrange their orientation to produce the display.

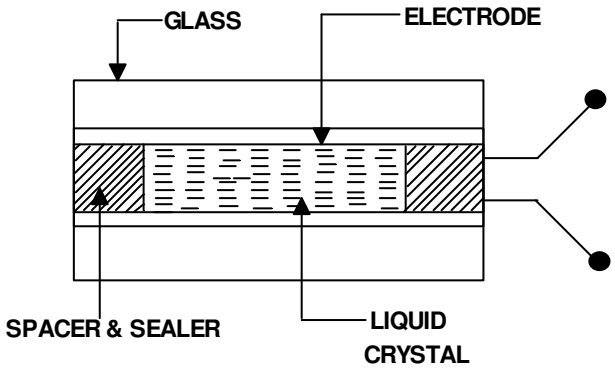


Fig.80.1(a)

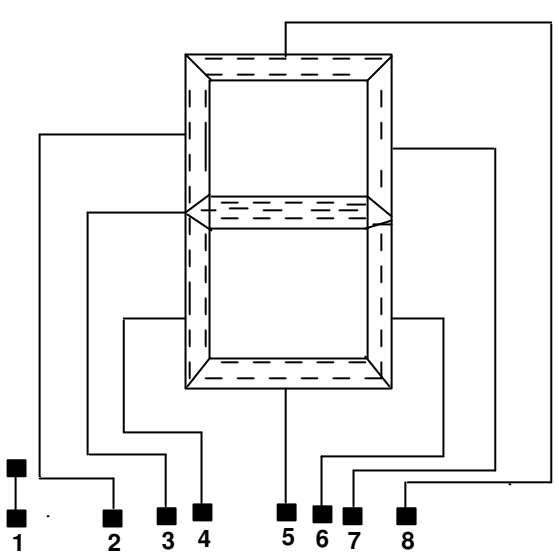


Fig.80.1(b)

LCD is a field effect device. The key to its operation is the liquid crystal or organic fluid sandwitched between two glass plates. An ac voltage is applied across the fluid from the top metallized segments to the metallized back plane. When affected by the magnetic field of ac voltage, the fluid transmits light differently and the energized element appears as black on a silvery background. It uses a polarizing filter on the top and bottom of the display as shown in fig. 80.1(a) & 80.1(b) The back plane and the segments are internally wired to contacts on the edge of LCD. Fig. 80.1(a) & 80.1(b) shows only two of those contacts.

Uses of LCD's:

(i) Field-effect LCDs are normally used in watches and portable instruments where source of energy is a prime consideration.

(ii) Thousands of tiny LCDs are used to form the picture elements (pixels) of the screen in one type of B & W pocket TV receiver.

Q.81 Explain in detail, the operation of a JFET. Marks (7)

Ans: **Principle of Operation of N-Channel JFET:** The circuit diagram of an N-channel JFET with normal polarities is shown in fig. 81.1

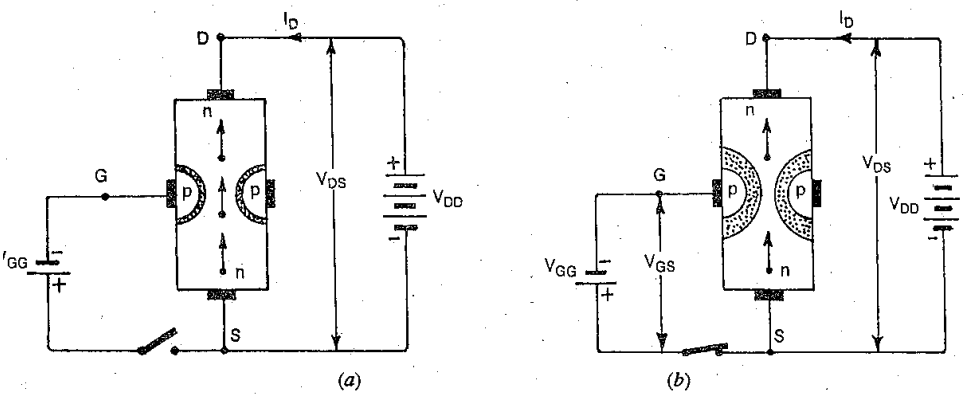


Fig. 81.1

When a voltage V_{DS} is applied across the drain and source terminals and voltage applied across the gate and source V_{GS} is zero (i.e. gate circuit is open) as shown in above fig. 81.1(a), the two PN junctions establish a very thin depletion layer. Thus a large amount of electrons will flow from source to drain through a wide channel formed between the two depletion layers.

When a reverse voltage V_{GS} is applied across the gate and source as shown in above fig. 81.1(b), the width of the depletion layer is increased. This reduces the width of the conducting channel thereby decreasing the conduction (flow of electrons) through it. Thus the current flowing from source to drain depends upon the width of the conducting channel which depends upon the thickness of depletion layer. The thickness of depletion layer established by the two PN junctions depends upon the voltage applied across the gate-source terminal. Hence, it is clear that the current from source to drain can be controlled by the application of potential (i.e. electric field) on the gate. That is why, the device is called Field Effect Transistor.

Q.82 Draw the circuit of a Full-wave Phase Controlled Rectifier using SCR. Explain its Working. What are its advantages over a diode rectifier circuits ? Marks (7)

Ans: **SCR as a Full-Wave Controlled Rectifier:** The circuit of an SCR as full-wave center-tap rectifier is shown in fig. 82.1. The circuit is exactly like the ordinary centre tap circuit using two diodes. Here, two SCRs have been used in place of diodes. R_L is load across which d.c. output appears. The gates of both the SCRs get their supply from the different sources as shown in fig. 82.1(a). By changing resistances r_1 and r_2, the gate current can be changed.

Working: Let us assume that the secondary voltage of transformer is less than forward breakover voltages of the SCRs. Then, it is clear that when both gate circuits are open ($I_g = 0$), no part of ac cycle can pass either through SCR 1 or SCR 2. Hence no voltage appears across the load i.e., output is zero.

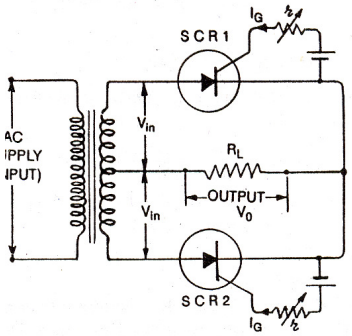


Fig. 82.1(a)

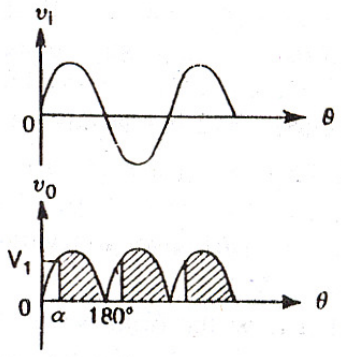


Fig. 82.1(b)

Let us suppose that now we close the gate circuits and pass gate current such that forward breakover voltage is V_1 ($V_1 < V_m$ i.e., ½ the secondary voltage). Then, in the first half cycle when upper end of transformer secondary is positive and lower end negative, SCR 1 will conduct from α to 180° as shown in fig. 82.2(b) i.e., it will allow the shaded portion of half cycle to pass through the load. Under such conditions, SCR 2 does not conduct.

Similarly, in the next half cycle, SCR 2 will conduct from (180 + α) to 360°, whereas SCR 1 does not. The current through the load is in the same direction (i.e.,dc) in both half cycles. By changing the gate current, we can vary the conduction angle and hence, the output voltage.

Advantages of Full-Wave Phase Controlled Rectifier using SCR over a Diode Rectifier Circuit: (i) In an ordinary full-wave rectifier, the rectifier (diode) conducts for the whole positive and negative half-cycle of ac, whereas, SCR can be made to conduct for whole or any part of the positive and negative half-cycle of ac by adjustment of gate current. Thus, the output voltage can be controlled by adjusting the gate current. Hence SCR operates as Controlled Rectifier.

Q.83 Using as Op-amp, explain the circuits for

(i) an integrator

(ii) a unity gain amplifier (with least components)

(iii) a current to voltage converter

Ans: **(i) Op-amp as an Integrator:** A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator or the integration amplifier. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_F is replaced by a capacitor C_F as shown in fig 83.1

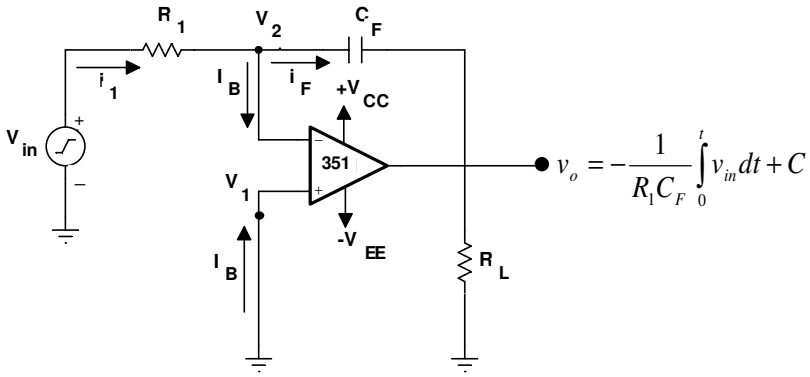


Fig. 83.1

The expression for the output voltage v_o can be obtained by writing Kirchhoff's current equation at node v_2 i.e., $i_1 = I_B + i_F$

Since IB is negligibly small, $i_1 \approx i_F$

The relationship between current through and voltage across the capacitor is given by

$$i_c = C\frac{dv_c}{dt}$$

Therefore,

$$\frac{v_{in} - v_2}{R_1} = C_F\left(\frac{d}{dt}\right)(v_2 - v_o)$$

However, in an ideal op-amp v1 = v2 ≈ 0 because A is very large. Therefore,

$$\frac{v_{in}}{R_1} = C_F\left(\frac{d}{dt}\right)(-v_o)$$

The output voltage can be obtained by integrating both sides with respect to time i.e.,

$$\int_0^t \frac{v_{in}}{R_1}dt = \int_0^t C_F\frac{d}{dt}(-v_o)dt$$

$$= C_F(-vo) + vo\big|_{t=0}$$

Therefore,

$$v_o = -\frac{1}{R_1C_F}\int_0^t v_{in}\,dt + C$$

Where C is the integration constant and is proportional to the value of the output voltage v_o at time t = 0 seconds. The above equation indicates that the output voltage is directly proportional to the negative integral of the input voltage and inversely proportional to the time constant R_1C_F.

(ii) **<u>Unity gain amplifier</u>:** When the non-inverting amplifier is configured for unity gain, it is called a voltage follower because the output voltage is equal to and in phase with the input. In other words, in the voltage follower the output follows the input.
The unity gain amplifier using non-inverting op-amp configuration is shown in fig. 83.2
In this circuit, the input voltage is fed to the non-inverting terminal and all the output voltage is fed back into the inverting terminal of the op-amp.

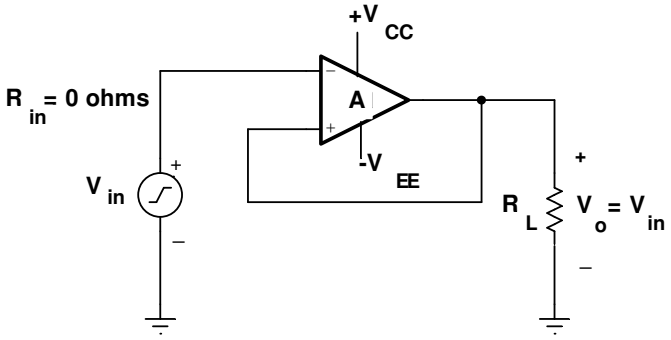


Fig. 83.2

The close loop gain of a non-inverting op-amp is given by the equation

$$A_V = 1 + \frac{R_F}{R_1}$$

In the above diagram $R_F = R_1 = 0\Omega$
Therefore, the gain $A_V = 1$.

(iii) **Current-to-Voltage Converter:** The basic inverting operational amplifier is used as current-to-voltage converter, which is shown in fig. 83.3

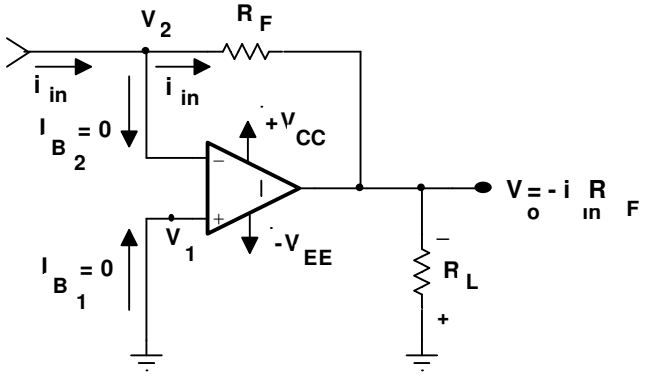


Fig. 83.3

From basic fundamentals, the output voltage in fig. 83.3 is given by

$V_o = -R_F i_{in}$, because $V_1 = V_2 = 0V$ in an ideal operational amplifier.

So, the above equation shows that the output voltage v_o becomes proportional to the input current i_{in}.

Q.84 By using a common collector NPN transistor configuration, explain how we Obtain (i) voltage gain (ii) current gain (iii) impedance matching Marks(10)

Ans: **(i) Voltage Gain:** Fig. 84.1(a) shows the Common Collector NPN transistor amplifier. Since the emitter resistor is not by-passed by a capacitor, the ac equivalent circuit of Common Collector Configuration will be as shown in below fig. 84.1(b). The ac resistance r_E of the emitter circuit is given by:

$r_E = r'_e + R_E$ where $r'_e = \frac{25mV}{I_E}$

Note that input voltage is applied across the ac resistance of the emitter circuit i.e., (r'_e + RE). Assuming the emitter diode to be ideal

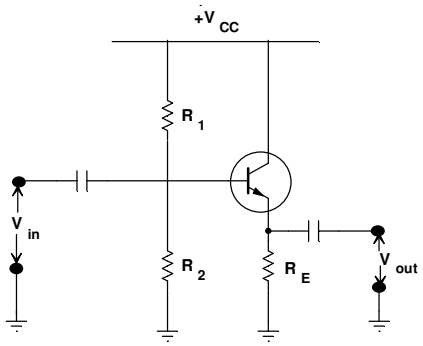


Fig. 84.1(a)

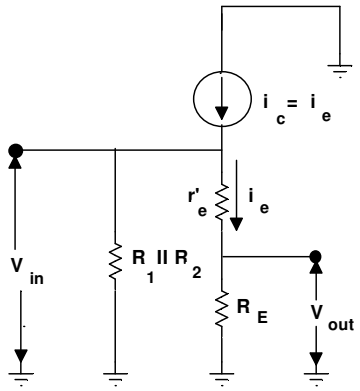


Fig. 84.1(b)

Output Voltage $V_{out} = i_e . R_E$
Input Voltage $V_{in} = i_e (r' + R_E)$
Therefore, Voltage Gain of Common Collector Configuration

$$A_V = \frac{V_{out}}{V_{in}} = \frac{i_e R_E}{i_e (r'_e + R_E)} = \frac{R_E}{r'_e + R_E}$$

Or $$A_V = \frac{R_E}{r'_e + R_E}$$

In most practical applications, $R_E >> r'_e$ so that $A_V \cong 1$
In practice, the voltage gain of a Common Collector Configuration is between 0.8 and 0.999.

(ii) Current Gain: Assuming $R_1 \,||\, R_2 >> r_{E,}$ the current gain is given as

$$\gamma = \frac{\Delta I_E}{\Delta I_B} = \frac{\Delta I_E}{\Delta I_E - \Delta I_C} = \frac{\frac{\Delta I_E}{\Delta I_E}}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{1}{1-\alpha} \quad (\because \alpha = \frac{\Delta I_C}{\Delta I_E})$$

$$= \beta + 1$$

(iii) Input Impedance of Common Collector Configuration: As for CE amplifier, the input impedance of common collector configuration is the combined effect of biasing resistors (R_1 and R_2) and the input impedance of transistor base [$Z_{in\ (base)}$]. Since these resistances are in parallel to the ac signal, the input impedance Z_{in} of the emitter follower is given by (refer to fig. 10.1(b)

$$Z_{in} = R1 \,\|\, R2 \,\|\, Z_{in\ (base)}$$

where $Z_{in\ (base)} = (\beta + 1)\ (re' + R'_E)$

$$r'_e = \frac{25mV}{I_E} \quad \text{and } R'_E = R_E \,\|\, R_L$$

In a Common Collector Configuration, the impedance of base [i.e., $Z_{in\ (base)}$] is gener very large as compared to R1 parallel to R2. Consequently, $Z_{in\ (base)}$ can be ignored. As result, approximate input impedance of the common collector configuration is given by:

$$Zin = R1 \parallel R2$$

(iv) Output Impedance of Common Collector Configuration:

The output impedance of a circuit is the impedance that the circuit offers to the load. When load is connected to the circuit, the output impedance acts as the source impedance for the load. Fig. 84.2 shows the circuit of Common Collector Configuration. Here R_s in the output resistance of amplifier voltage source.

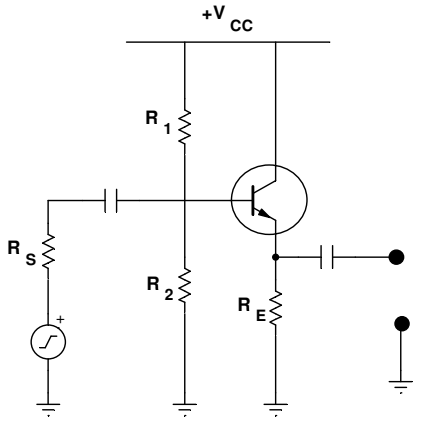


Fig. 84.2

The output impedance Z_{out} of the common collector configuration is given by

$$Z_{out} = R_E \parallel \left(r'_e + \frac{R'_{in}}{\beta} \right)$$

Where $R'_{in} = R1 \parallel R2 \parallel Rs$

In practical circuits, the value of R_E is large enough to be ignored. For this reason, the output impedance of common collector configuration is approximately :

$$Z_{out} = r'_e + \left(\frac{R'_{in}}{\beta} \right)$$

So, the Common Collector Configuration has High Input Impedance (hundreds of kilo-ohms) and Low Output Impedance (tens of ohms). It is a good impedance matching device.

Q.85 How is a BJT biased for stability ? **Marks (4)**

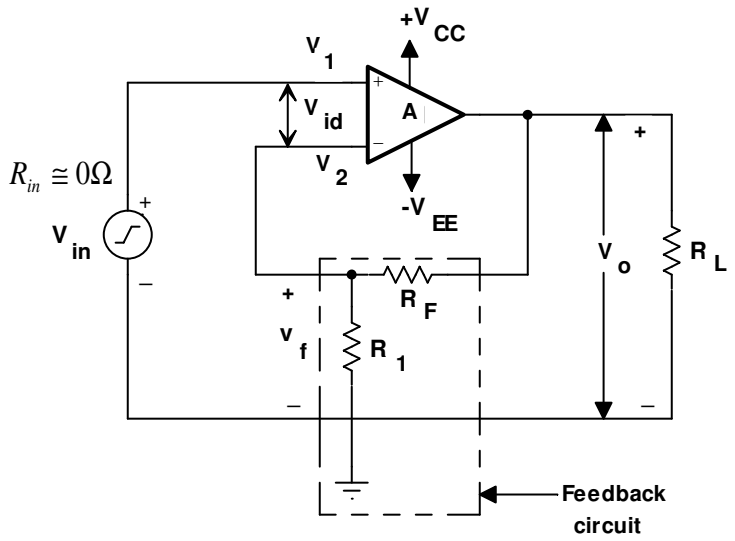
Ans: **Requirements of Biasing Circuit for Stability:** A biasing network associated with a BJT should fulfill the following requirements:

(i) Establish the operating point in the middle of the active region of the characteristics, so that on applying the input signal, the instantaneous operating point does not move either to the cut-of region or to the saturation region, even at the extreme values of the input signal.
(ii) Stabilize the collector current Ic against temperature variations.
(iii) Make the operating point independent of transistor parameters so that replacement of transistor by another of the same type in the circuit does not shift the operating point.

Q.86 Draw the schematic diagram of an ideal non-inverting Op-amp with voltage Series feedback and derive an expression for the voltage gain. **Marks(6)**

Ans: **Expression for the Closed Loop Voltage Gain of a Non-inverting Op-amp:**

The circuit diagram of an Ideal Non-inverting Op-amp with voltage series feedback is



shown in fig.86(a)

Fig. 86(a)

The closed loop voltage gain is given by $A_F = \frac{v_o}{v_{in}}$ (or) the output voltage is given by

$$v_o = A\,(v_1 - v_2) \quad (\because v_{in} = v_1 - v_2)$$

Referring to the fig.11(a), we see that $v_1 = v_{in}$

$$v_2 = v_f = \frac{R_1 v_o}{R_1 + R_F} \quad \text{since} \quad R_i >> R_1$$

Therefore, $$v_o = A\left(v_{in} - \frac{R_1 v_o}{R_1 + R_F}\right)$$

Rearranging the above equation, we get $$v_o = \frac{A(R_1 + R_F)v_{in}}{R_1 + R_F + AR_1}$$

Thus $$A_F = \frac{v_o}{v_{in}} = \frac{A(R_1 + R_F)}{R_1 + R_F + AR_1} \quad \text{(exact)}$$

Generally, A is very large (typically 10^5).

Therefore,

$AR_1 >> (R_1 + R_F)$ and $(R_i + R_F + AR_1) \approx AR_1$

Thus

$$A_F = \frac{v_o}{v_{in}} = 1 + \frac{R_F}{R_1} \quad \text{(ideal)}$$