ROLL NO.

Code: DE60/DC68 Subject: MICROPROCESSORS & MICROCON

Diplete - ET/CS

Time: 3 Hours JUNE 2013

Max. Marks: 100

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions, answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

Q.1	Choose the correct or the best altern	native in the following: (2	2×10
	a. Which of the following is not an advantage of an assembly language program		
	(A) Less error prone		
	(B) No need of compiler		
	(C) Less tiresome to work with		
	(D) Same program works on any computer		
	b. Which of the following addressing mode is not provided in 8085.		
	(A) Register addressing mode	(B) Indirect addressing mode	
	(C) Indexed addressing mode		
	c. TRAP is a		
	(A) Only level sensitive interrupt	(B) Non-maskable interrupt	
	(C) maskable interrupt	(D) Software interrupt	
dpin of 8251 is a general purpose of used to send MODEM control condition			i
	(A) TxRDY	(B) \overline{RD}	
	(C) \overline{CS}	(D) \overline{DTR}	
	e. Intel 8085A is fabricated using	technology.	
	(A) NMOS	(B) PMOS	
	(C) HMOS	(D) CMOS	

ERS

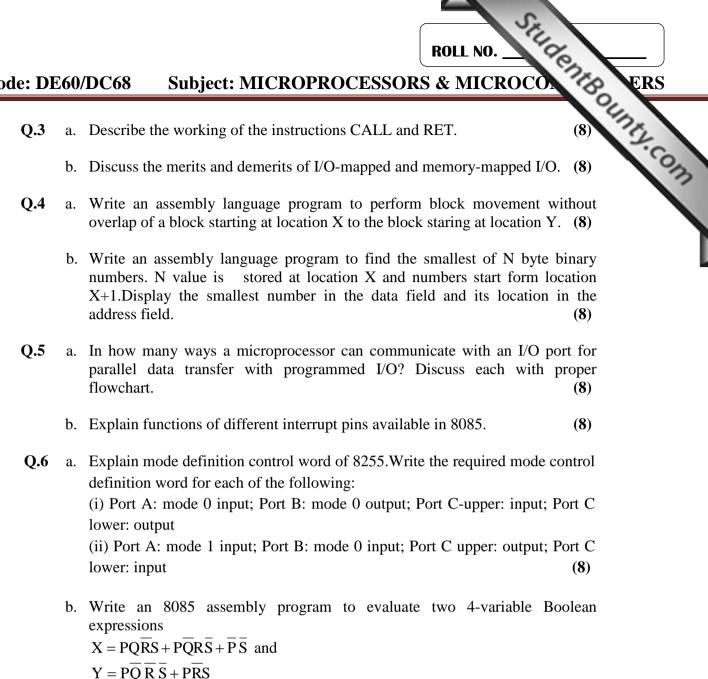
Code: DE

60	0/DC68 Subject: MICROPR	OCESSORS & MICROCO		
f.	Which of the following statements microprocessor	is true for NOP instruction in 80		
	(A) This instruction is not used in the p(B) It halts program execution(C) Address and data bus are placed in(D) Its one byte instruction			
g.	. 8257 DMA controller is in master mod	3257 DMA controller is in master mode when		
	(A) Processor is reading data from 825(B) Processor is programming 8257(C) Processor is in active mode(D) Processor is in HOLD state	7		
h.	Intel 8255 chip is to be interfaced for sending data to LED display that updates display based on latched output. Which mode of operation for 8255 is most suitable for this operation?			
		3) Mode 1 D) None of these		
i.	is an 8-bit register of 8259 in active interrupt requests.	is an 8-bit register of 8259 interrupt controller that keeps track of etive interrupt requests.		
	<u> </u>	B) Interrupt request register D) Slave register		
j.	Maximum external RAM addressability in 8051 is			
		B) 1MB D) 128 byte		
Answer any FIVE Questions out of EIGHT Questions. Each question carries 16 marks.				

- **Q.2** a. Distinguish between following pair of instructions of 8085 **(8)**
 - (i) LXI H, 123H and LHLD 1234H
 - (ii) SPHL and PCHL
 - (iii) XRA M and ORA M
 - (iv) RRC and RLC
 - b. What is PSW? Write a 8085 assembly program to exchange contents of accumulator and flag register. **(8)**

2

Subject: MICROPROCESSORS & MICROCO. **Code: DE60/DC68**



Q.7 a. What is the need for interrupt controller in microcomputer system? Draw a neat functional pin diagram of Intel 8259 and state function of various pins. (8)

b. What is the need for DMA data transfer in microcomputer system? State the function of following pins of DMA controller 8257

(i) Ready

(ii) HLDA

(iii) HRQ

(iv) IOW

(v) TC

(vi) MR

Q.8 a. Discuss the need of a programmable interval timer in microcomputer system. In how many modes of operation a counter can be configured to work?

b. Briefly explain mode 2 operation of 8253

using logic controller interface.

(4)

(8)

(8)

ROLL NO.

Code: DE60/DC68 Subject: MICROPROCESSORS & MICROCOA

c. Discuss in brief what information is indicated on Intel 8251 USART control port to configure it for transmission / reception in asynchronous mode? (8)

Q.9 a. What is a microcontroller? What are its applications? (4)

- b. Explain the function and byte usage for following instructions in IC8051 (4)
 - (i) MUL A B

(ii) CLR C

(iii) SWAP A

(iv) XCH A, 31H

c. Describe (with suitable examples) all the addressing modes available in 8051.

(8)