

Q.2 a. Perform the following conversions:

(i) $(2496)_{10} = (?)_8$

(ii) $(CF3D)_{16} = (?)_{10}$

(iii) $(11011.0111)_2 = (?)_{10}$

Answer:

i. $(2496)_{10} = 2496/8$ is 312 with remainder 0
 $312/8$ is 39 with remainder 0
 $39/8$ is 4 with remainder 7
 $4/8$ is 0 with remainder 4
 Result $(4700)_8$

ii. $(CF3D)_{16} = 12 \times 16^3 + 15 \times 16^2 + 3 \times 16^1 + 13 \times 16^0$
 $= (53053)_{10}$

iii. $(11011.0111)_2 = 011\ 011\ .\ 011\ 100$
 $(3\ \ 3\ .\ 3\ 4)_{10}$

b. Draw the functional diagram of a digital computer and explain the function of each block.

Answer: Page Number 16 of Text Book

c. Give examples of parallel and serial transmission in digital systems.

Answer: Page Number 13-14 of Text Book

Q.3 a. What is the need to minimize a Boolean expression? What are the methods used to achieve these.

Answer:

To reduce the hardware requirement, resulting in the same truth table.
 Various methods:

- I. Using theorems and postulates
- II. K-Map
- III. Tabular forms

b. Minimize the following Boolean expressions and write the truth tables to show that the minimized expressions will produce the same output as the expanded expressions.

(i) $F = m_0 + m_2 + m_5 + m_7 + m_8 + m_{10} + m_{13} + m_{15}$

(ii) $y = (A' + B)(A' + B + D)(C + D')$

Answer:

b. Minimize the following Boolean expressions and write the truth tables to show that the minimized expressions will produce the same output as the expanded expressions.

i. $F = m_0 + m_2 + m_5 + m_7 + m_8 + m_{10} + m_{13} + m_{15}$ — ①

	$\bar{B}A\bar{B}\bar{A}$	$\bar{B}A\bar{B}A$	$\bar{B}A\bar{B}\bar{A}$	$\bar{B}A\bar{B}A$
$D\bar{C}$	1	0	0	1
$D\bar{C}$	0	1	1	0
$D\bar{C}$	0	1	1	0
$D\bar{C}$	1	0	0	1

$F = AC + \bar{A}\bar{C}$ — ②

ALSO TO WRITE TT FOR equation ① and ②

ii. $Y = (A' + B)(A' + B' + D)(C + D')$

DC

1	0	0	1
1	0	0	1
1	0	1	1
0	0	0	0

$Y = \bar{A}C + \bar{A}BC + \bar{A}CD + BC + BCD + \bar{A}\bar{D} + \bar{A}B\bar{D}$

$Y = (\bar{A} + B)(C + \bar{D})(\bar{A} + D)$ — ③

TRUTH TABLE — ③

Q.4 a. Draw the logic diagram of eight bit serial in/parallel out shift register and explain its operation.

Answer: Page Number 443, 444 & 445 of Text Book

b. What is meant by multiplexer? List out its various applications.

Answer: Page Number 443, 444 & 445 of Text Book

Q.5 a. Distinguish between asynchronous and synchronous Flip Flops. Convert an asynchronous RS flip flop into synchronous latch.

Answer: Page Number 176-181 of Text Book

b. Design a decade counter using JK Flip Flops and draw its timing diagram.

Answer: Page Number 299 of Text Book

c. What is the need of Schmitt trigger devices, explain with waveforms.

Answer: Page Number 214-215 of Text Book

Q.6 a. Build a Full Adder using two Half Adders and prove that the addition of two numbers results in subtraction when 2's complement is used.

Answer: Page Number 264-265 of Text Book

b. If a single bit Full Adder takes 8sec for addition, calculate the total addition time taken to add two numbers having hundredth weight. Suggest a method of speeding up the addition.

Answer:

Ans: $t_d = 8\text{nsec}$ Hundredth weight addition of decimal requires 3 4bit parallel adders. Thus total delay is sum of delays of each of the adders Which will amount to $(4 \times 3) \times 8 = 96\text{nsec}$
To reduce the delay Carry look ahead circuit to be used. (Explanation)

Q.7 a. Design a seven segment decoder that is required to drive an active low seven segment display.

Answer:

D3	D2	D1	D0	a'	b'	c'	d'	e'	f'	g'
0	0	0	0	0	1	1	1	1	1	1
0	0	0	1	1	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	1	0	1	0	1	0	0
0	1	0	1	0	1	0	0	1	0	0
0	1	1	0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	1	1	0	0

$$a = \bar{D}_3 \bar{D}_2 \bar{D}_1 D_0 + D_2 \bar{D}_0$$

	D'0D'1	D0D'1	D0D1	D'0D1
D'2D'3	0	1	0	0
D2D'3	1	0	0	1
D2D3	x	x	x	x
D'2D3	0	0	x	x

$$b = D_0 \bar{D}_1 D_2 + \bar{D}_0 D_1 D_2 + \bar{D}_0 \bar{D}_1 \bar{D}_2 \bar{D}_3$$

	D'0D'1	D0D'1	D0D1	D'0D1
D'2D'3	1	0	0	0
D2D'3	0	1	0	1
D2D3	x	x	x	x
D'2D3	0	0	x	x

$$c = \bar{D}_0 \bar{D}_2 \bar{D}_3 + \bar{D}_0 \bar{D}_1 \bar{D}_3$$

	D'0D'1	D0D'1	D0D1	D'0D1
D'2D'3	1	0	0	1
D2D'3	1	0	0	0
D2D3	x	x	x	x
D'2D3	0	0	x	x

$$d = \bar{D}_0 \bar{D}_2 \bar{D}_3 + D_0 D_3 + D_0 D_1 D_2$$

	D'0D'1	D0D'1	D0D1	D'0D1
D'2D'3	1	1	0	0
D2D'3	0	0	1	0
D2D3	x	x	x	x
D'2D3	0	1	x	x

$$e = \bar{D}_1 D_3 + D_0$$

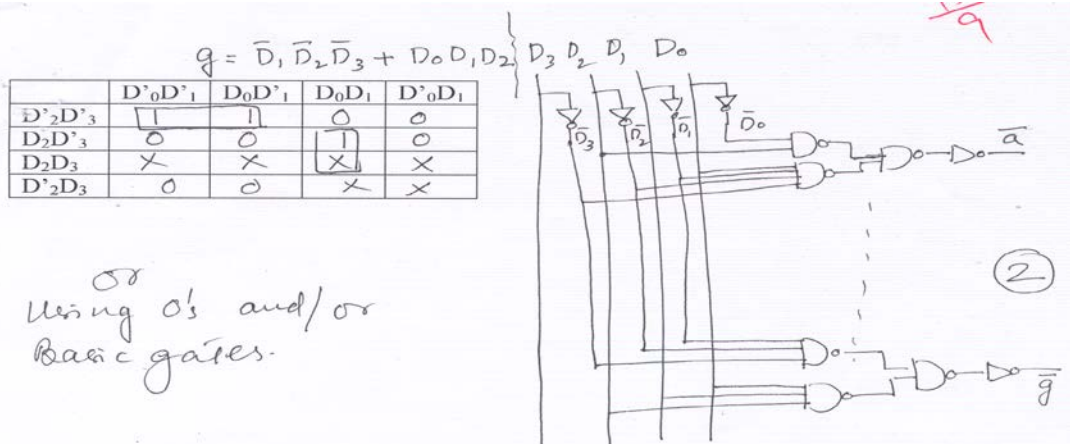
	D'0D'1	D0D'1	D0D1	D'0D1
D'2D'3	1	1	1	0
D2D'3	1	1	1	0
D2D3	x	x	x	x
D'2D3	0	1	x	x

$$f = \bar{D}_2 \bar{D}_3 + D_0 D_1$$

	D'0D'1	D0D'1	D0D1	D'0D1
D'2D'3	1	1	1	1
D2D'3	0	0	1	0
D2D3	x	x	x	x
D'2D3	0	0	x	x

- b. What are the advantages and disadvantages of a synchronous counter over an asynchronous counter?

Answer:



- c. How many AND gates are required to decode completely all of the states of a MOD-32 binary counter? What are the inputs to the gate that decodes for the count of 21?

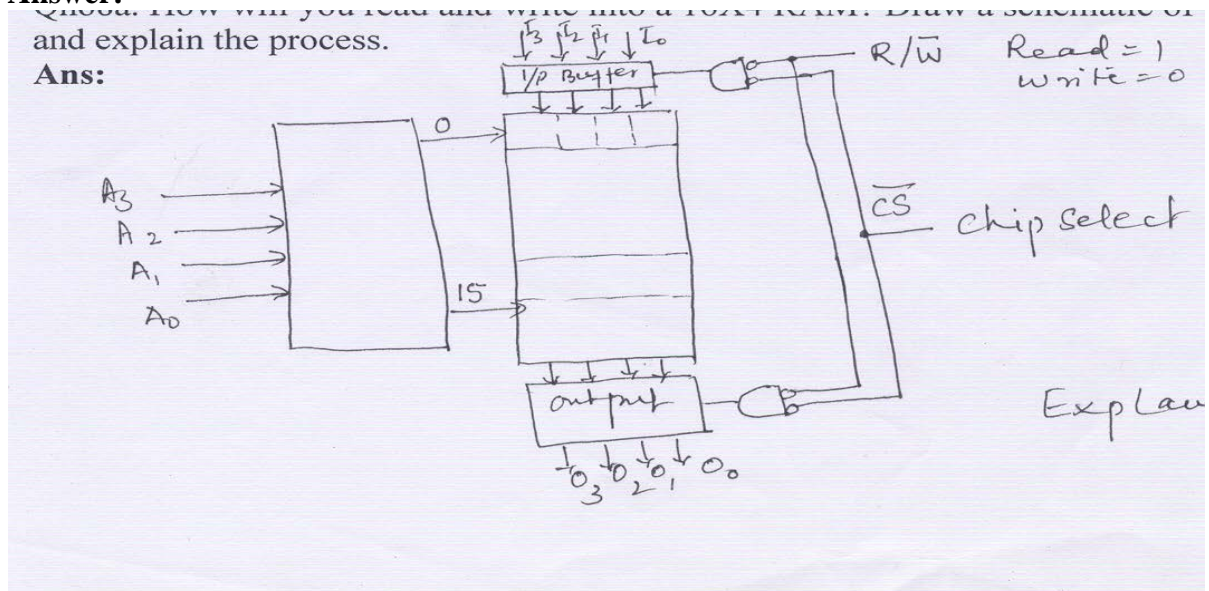
Answer: Page Number 391 of Text Book

- Q.8** a. How will you read and write into a 16×4 RAM? Draw a schematic of this RAM and explain the process.

Answer:

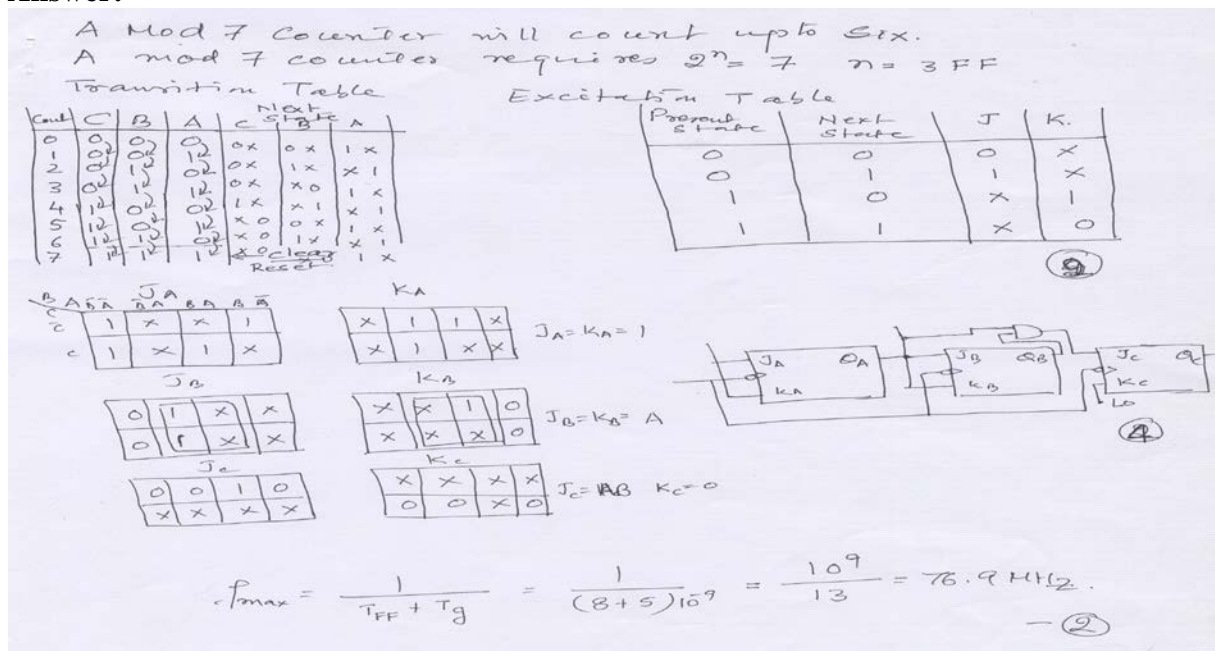
and explain the process.

Ans:



- b. Design a mod 7 synchronous counter and calculate its maximum frequency of operation if the flip flop delay time is 8 nano sec. and gate delay time is 5 nano sec.

Answer:



- Q.9** Explain the principle of the following:
- (i) Magnitude Comparator
 - (ii) CPU and memory interface
 - (iii) Johnson Counter
 - (iv) DRAM

Answer:

- (i) Page Number 524-527 of Text Book
- (ii) Page Number 630-632 of Text Book
- (iii) Page Number 342-344 of Text Book
- (iv) Page Number 671-674 of Text Book

TEXT BOOK

Digital Systems – Principles and Applications, Ronald J Tocci, Neal S. Wildmer,
Gregory L. Moss, Ninth Edition, Pearson Education, 2008