Q.2 a. In a microprocessor, what is the use of a register? What are the advantages & disadvantages of using registers over a memory location? What is the speciality of register A (accumulator) over other general purpose registers in 8085?

Answer:

Register is nothing but a group of flip flops where each flip flop can store a bit of information. The size of register in in 8085 is 8 bit to store 8 bits of information.

The advantages of registers over memory locations are as follows:

- Faster access to the contents as compared to that of memory location
- Instructions involving register operands will be shorter in length and are executed faster compared to instructions involving memory locations
- In instructions involving register operands the number of bits that are free to specify the operation are less, thereby reducing number of possible instructions

The disadvantages of registers are

- During interrupt service subroutine (ISS) the register values will have to be stored in memory called stack. Upon return from ISS, these are restored back which eventually hampers speed.
- Use of too many registers can occupy space available for control unit and ALU.

Significance of A-Among the other GPRs this is the most important .In an arithmetic operation involving two operands ,one has to be in this register. The result of the arithmetic operation will be stored in A. In logical operation involving two operands one has to be in accumulator. Also some operations like complementing, decimal adjustment can be performed only on the accumulator

b. Explain the pin diagram of 8085 with description.

Answer: Page Number 29 of Text Book

Q.3 a. Explain the instructions using example:
(i) PC (ii) CM
(iii) IR (iv) CNC

Answer: Page Number 101 of Text Book

b. What is the need for input output ports in microcomputer systems? Discuss merits and demerits of input-output mapped with respect to memory mapped input-output in 8085.

Answer:

Need for input output ports in microcomputer systems:

CPU and main memory are very fast as compared to mechanical input /output device. In such cases it is essential that data lines of the computer are not kept engaged for along time during communication with input/output device as the overall speed of the

computer system will drastically get reduced so there is need of input/output orts in microcomputer system.

Merits and demerits of input-output mapped with respect to memory mapped input-output in 8085-

- In I/O mapped scheme I/O devices are treated as I/O and memory as memory whereas in memory mapped I/O scheme both I/O and memory are treated as memory.
- Only In and OUT instructions are used for addressing I/O mapped I/O ports but large number of instructions can be used for communication with a memory mapped I/O. All instructions used to access memory can be used to access memory mapped I/O.
- Using I/O mapped I/O only accumulator can communicate with an I/O port. With memory mapped I/O any register can communicate with memory mapped I/O port.
- In memory mapped I/O device address is 20 bits whereas in I/O mapped it is 8/16 bits
- For I/O mapped total devices that can be shared with 1MB memory is 65535 input and 65535 output devices whereas for 1 MB memory total devices will be A MB as its is shared between memory and I/O
- Only data transfer operations are possible with direct data from I/O devices whereas in memory mapped I/O both arithmetic/logical operations are also possible on direct data from I/O device.
- In I/O mapped scheme decoding of 8/16 bits address is only required so hardware is less whereas in memory mapped I/O scheme decoding of 20 bits is needed so hardware is more.
- The control signals used in I/O mapped scheme are $\overline{IOR}$ & $\overline{IOW}$ whereas in memory mapped I/O it is $\overline{MEMR}$ and $\overline{MEMW}$

Q.4 a. Write an assembly language program to multiply two one byte binary numbers stored at locations X and Y. Display the 16 bit result in the address field.

Answer:

```
            ORG C 100H
      X:    DB 05H              ; Assuming the number to be 05H

            ORG C200H
      Y:    DB 04H              ; Assuming other number to be 04H
            ORG C 000H
      Z:    EQU C300H
CURAD :     EQU FFF7H
UPDAD:      EQU 06BCH
            LXI H,X             ;HL is loaded with C100H
            MOV E,M             ;content of E is 05H
            MVI D,00H           ;content of DE is 05H
            LXI H,Y             ; HL is loaded with C200H
            MVI A,M             ; Accumulator content is 04H
```

```
                LXI H, 000H      ;HL becomes 000H
                CPI 00H          ;04H Vs 00H
                JZ EXIT          ;No jump
AGAIN:          DAD D            ;HL =0005H     | 000H   | 000FH | 0014H
                DCR A            ; A= 03H       | 02H    | 01H   | 00H
                JNZ  AGAIN       ; jump         |jump    |jump   |no jump
EXIT:           SHLD Z           ; C3000H= 14 H and C301H =000H
                SHLD CURAD       ; FFF7H=14 H   and FFF8H= 00H
                CALL UPDAD       ; Display 0014 in the address field.
                HLT              ; program terminated.
```

b. Write an 8085 assembly language program to find the HCF of two 8 bit numbers. The numbers are stored at location X & Y. Display the numbers in the address field, and their HCF in the data field.

Answer:Page Number 187 of Text Book

Q.5 a. What is the need for masking and interrupt? Discuss SIM and RIM instruction in 8085.

Answer:

Need for Masking an interrupt: If a microprocessor is interrupted with RST65 and is executing ISS for the same; then even with DI instruction in the beginning of ISS, all interrupts except TRAP are disabled. So even if another interrupt request of higher priority like RST 7.5 cannot be used in the middle of the execution of ISS of RST6.5.To solve such problem and selectively disable the interrupts; concept of masking is used.

An interrupt pin that is masked cannot interrupt even if it is activated and interrupts are generally activated using EI instruction .While one which is unmasked can interrupt when interrupt pin is activated and interrupts are in general enabled using EI instruction.

SIM Instruction: SIM stands for Set Interrupt mask –is a single byte instruction used for

- Masking/unmasking RST 7.5, RST 6.5 and RST 5.5
- Reset 0 RST7.5 Flip-flop
- Perform serial output of data.

When Sim instruction is executed contents of accumulator decide the action to be taken. On execution of SIM the bitwise content of the accumulator decide the effective action to be taken as

D7	D6	D5	D4	D3	D2	D1	D0
SOD	SOE	X	R7.5	MSE	M7.5	M6.5	M5.5

The bits that are used for masking/unmasking are

Bit 3- If it is 0 SIM instruction is not used for masking/unmasking

Bit2- If MSE is 1 and M7.5 is 1 RST 7.5 is masked. And if If MSE is 1 and M7.5 is 0 RST 7.5 is unmasked.

Bit 1- If MSE is 1 and M6.5 is 1 RST 6.5 is masked. And if If MSE is 1 and M6.5 is 0 RST 6.5 is unmasked

Bit 0- If MSE is 1 and M5.5 is 1 RST 5.5 is masked. And if If MSE is 1 and M5.5 is 0 RST5.5 is unmasked.

RIM instruction: RIM stands for read interrupt mask**.** It's a single byte instruction used for

- checking masked status of RST 7.5, RST 6.5 or RST 5.5
- Checking enable/disable interrupt
- Pending status of interrupt
- Perform serial input of data.

Meaning of accumulator contents that decide execution of RIM instruction is as shown

D7	D6	D5	D4	D3	D2	D1	D0
SID	IP7.5	IP6.5	IP5.5	IE	M7.5	M6.5	M5.5

First three least significant bits provide mask status of interrupts. Its value if is 1 then corresponding interrupt is masked.

If bit 3(IE) is 1 then interrupt system is enabled .the rest three bits indicate pending status of interrupts-If bit 4,5 or 6 is having value equal to 1 then RST 5.5,RST 6.5 and RST 7.5 requests are respectively pending. On execution of RIM instruction data on the SID pin of 8085 gets loaded in this bit position.

b. Explain the mode definition control word of 8255.Configure port A and port B as input port and port C as output port when 8255 is connected as I/O mapped I/O(mode 0). What will be the mode definition control word?

Answer:

Mode definition control word: The contents of control word get latched in mode definition control port if MS bit of control port is 1.If MS bit is 0 then contents of the control port get latched in port C bit set/reset control port.

D7	D6	D5	D4	D3	D2	D1	D0
1	MA2	MA1	PAI	PCu1	MB	PBI	PCII

Bit 7 must be 1 to indicate that the control port contains mode definition control word. The meaning of bits of control port when it contains mode definition control word is as follows

- Bit 0 (PCII)- =1 Port C lower as input (PC_{3-0}); and if =0 port C (PC_{3-0}) as output
- Bit 1 (PBI)- =1 port B as input; and if =0 port B as output
- Bit 2 (MB)- =1 port B in mode 1 and if =0 port B in mode 0
- Bit 3(PCu1)- =1 Port C (PC_{7-4})upper as input ; if =0 Port C upper as output
- Bit 4 (PAI) =1 port A as input ; if =0 port A as output
- Bits (6,5)(MA2,MA1) 00 = Port A in mode 0;
  01= Port A in mode 1;
  10 = Port A in mode 2;

  11 = Port A in mode 2;

For port A and port B as input port and port C as output port when 8255 is connected as I/O mapped I/O (mode 0) the control word will be

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	0

Q.6 a. Explain keyboard & display mode set command of 8279.

Answer: Page Number 384, 385 of Text Book

b. Write an 8085 assembly language program to implement a decimal counter using logic controller interface. The starting count should be accepted from interface and displayed on the interface.

Answer:

Assembly language program to implement a decimal counter using logic controller interface.;; *The program follows an infinite loop till user wants to enter a valid two digit BCD value at PORT B. Its value is then displayed at PORT A. After every 0.5s delay the count value is incremented by 1 and its decimal is sent to PORT A. Once the count value rolls over from 00 to 99 the operation repeats endlessly*

```
        ORG C000H
PA      EQU D8H
PB      EQU D9H
PC      EQU DAH
CTRL    EQU DBH
DELAY                   EQU 04BEH
MVI A,  10001010B
OUT     CTRL            ;Configure 8255 ports
```

;;Next instructions ensure the control transfer Only after valid 2-bit BCD data input

```
AGAIN :                 IN PB
        ANI 0FH
        CPI 0AH
        JNC AGAIN
        IN      PB
        ANI   F0H
        CPI     A0H
        JNC AGAIN
        IN      PB
REPEAT: OUT  PA         ;; Display the count  data /value
        PUSH PSW
        LXI DFFFH
        CALL DELAY      ;Generate 0.5 s delay
        POP PSW
        ADI 01H
```

```
        DAA             ;Increment value of the counter
        JNZ REPEAT
        JMP AGAIN
```

Q.7 a. Explain the overview of 8259? Discuss various registers available in Intel 8259 –programmable interrupt controller.

Answer: Page Number 419 of Text Book

b. Describe the functionality of following pins available in DMA controller-8257

(i) Reset (ii) $\overline{IOW}$

(iii) HRQ (iv) HLDA

(v)TC (vi) $\overline{MR}$

(vii) ADSTB (viii) AEN

Answer:

Functions of pins in 8257DMA Controller:

i. Reset- Active high input pin connected to reset out pin of 8085When 8085 is reset then it sends logic 1 to 8257 to reset the control register becomes 00H,all four DMA channels are disabled.

ii. $\overline{IOW}$ -It's an active low pin that is activated by processor to write to an ARC,CR or the control register when 8257 is in slave mode.

iii. HRQ- stands for hold request. Active high output connected to HOLD input of 8085.whenever DRQ is active the corresponding DMA channel is enabled and HRQ is activated by 8257.to request processor for granting necessary control of the system bus.

iv. HLDA- Stands for HOLD acknowledge. Active high input pin which is connected to HLDA output of 8085.When HLDA becomes active it means that the processor has gone to HOLD state and 8257 is the master of the microcomputer system.

v. TC-Terminal Count- active high output pin activated when all LS 14 bits of CR become 0 for DMA channel being serviced.

vi. $\overline{MR}$ -It is active high input pin that is in tri-state when 8257 is in slave mode. When processor is in HOLD state 8257 drives this pin.

vii. ADSTB-Stands for address strobe- active high pin.8257 outputs 0 on this pin as long as it is in slave mode. When it becomes master it gives 1 only during first four clock cycles of DMA machine cycle.

AEN-Address enable- Active high output pin .8257 outputs 0 on this pin when 8085 is master of the system. When 8085 goes into HOLD state 8257 gives 1 on this pin indicating that it is mater now.

Q.8 a. Discuss the interpretation of the bits of the control port of 8253.

Answer:

Interpretation of Control port of 8253:

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

- SC1 and SC0 : 00 Counter 0 selected ;01 Counter 1 selected;10 Counter 2 selected and 11 –illegal
- M2,M1,M0 : 000 mode 0-interrupt on terminal count; 001- mode1-retriggerable monostable multi
  010- Mode 2-rate generator; 011-Mode 3 –square wave generator 100-Mode 4- software triggered strobe; 101-Mode 5- Hardware triggered strobe
  110 and 111- illegal.
- BCD- 1-Perform count down in decimal ;0- perform count down in hexadecimal
- RW1,RW0 : 00-Read on fly for READ operation illegal for WRITE operation
  : 01-Read/Write LS byte of counter
  : 10-Read/Write MS byte of counter
  : 11 Read /Write LS byte then Ms byte of counter.

b. Specify the mode word format required to initialize 8251in desired mode for following conditions:

(i) Asynchronous mode; Baud Rate x 1; 8 bit/character; even parity; one stop bit.

(ii) Synchronous mode; 5 character length, even parity; internal sync detection; Single sync character.

Answer:

Mode word format required to initialize 8251Communication interface:

(i) Asynchronous mode; baud rate factor x1; 8 bit character; odd parity; one stop bit-

D7	D6	D5	D4	D3	D2	D1	D0
S2	S1	EvP	EnP	L2	L1	B2	B1
Depends on sync/async		Parity	Parity enable	Character length		Buad rate factor	
0	1	0	1	1	1	0	1

ANSWER : **5DH**

(ii) Synchronous mode;5 character length, even parity; internal sync detection; single sync character

D7	D6	D5	D4	D3	D2	D1	D0
S2	S1	EvP	EnP	L2	L1	B2	B1
Depends on sync/async		Parity	Parity enable	Character length		Buad rate factor	
1	0	1	1	0	0	0	0

Answer: **B0H**

Q.9 a. Explain the functional pin diagram of 8051 with a neat diagram.
Answer: Page Number 548 of Text Book

b. Mention exactly what happens (which operation takes place) when following
8051 instruction is executed and identify its addressing mode:
(i) ORL A,50H
(ii) ADD A,20H
(iii) SUBB A,45H
(iv) ANL A @ Ri

Answer:

8051 instructions:Function and addressing modes:

(i) **ORL A,50H**-This instruction will bitwise logically OR the contents of the accumulator with data. Result will be stored in accumulator- Immediate addressing mode.

(ii) **ADD A,20H** –The instruction adds data to content of accumulator, It is direct addressing mode

(iii) **SUBB A,45H-** This instruction will subtract the contents of memory location whose direct address is specified from the contents of accumulator. Its direct addressing mode

(iv) **ANL A, @Ri –** this instruction will bitwise logically AND the contents of accumulator with contents of memory location pointed by Ri of selected register bank. Result will be stored in accumulator .Its register indirect addressing mode.

c. Mention the various types of instructions available for 8051, with examples.

Answer: Page Number 560 of Text Book

TEXT BOOK

The 8085 Microprocessor; Architecture, Programming and Interfacing, K. Udaya Kumar and B. S. Umashankar, Pearson Education, 2008