**Code: AE27**            **Subject: DIGITAL HARDWARE DES...**

# AMIETE – ET (OLD SCHEME)

| Time: 3 Hours | **OCTOBER 2012** | Max. Marks: 100 |
|---|---|---|

*PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.*

**NOTE: There are 9 Questions in all.**

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

**Q.1**    **Choose the correct or the best alternative in the following:**              **(2×10)**

a.   Which is not a property of VHDL

   **(A)**   Parallel language
   **(B)**   Strongly typed language
   **(C)**    Uses Implicit default sequential control flow
   **(D)**   Uses explicit time delays

b.   Component instantiation is use in _____ modeling

   **(A)** Structural              **(B)** Behavioral
   **(C)** Data flow               **(D)** High level model

c.   The signal assignment statement is denoted by the symbol

   **(A)** '= ='                   **(B)** '='
   **(C)** '=>'                    **(D)** '<='

d.   Pattern recognizer can be implemented using _____

   **(A)** Decoder                 **(B)** Counter
   **(C)** Mux/De-mux              **(D)** Shift register

e.   Operators belong to _____ of data subsystem.

   **(A)** Functional module       **(B)** Data paths
   **(C)** Storage module          **(D)** Conditional points

f.   _____ has no AND gates.

   **(A)** Coincident Decoder      **(B)** Tree Decoder
   **(C)** Priority encoder        **(D)** Binary encoder

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g.  PLA is a combinational module that provides _____

(A) NOT-AND-XNOR              (B) NOT-AND-OR
(C) NOT-AND-NOR               (D) NOT-AND-XOR

h.  In tabular representation of switching functions, an integer $j$ is associated with each n-tuple. For *n-tuple* j is defined as

(A) $j = \sum_{i=0}^{n-1} x_i 2^{i+1}$          (B) $j = \sum_{i=0}^{n} x_i 2^i$

(C) $j = \sum_{i=0}^{n-1} x_i 2^i$          (D) $j = \sum_{i=0}^{n-1} x_i 2^{i-1}$

i.  Microcontroller design can be represented using

(A) state machine              (B) activity chart
(C) flow chart                 (D) micro machine

j.  A data path is said to be _____ if it connects a unique source and destination.

(A) Indirected              (B) Directed
(C) Erected                 (D) Dedicated

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**Answer any FIVE Questions out of EIGHT Questions.**
**Each question carries 16 marks.**

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**Q.2**   a.  Explain data representation and coding in digital systems. Give an example for each.   **(6)**

b.  Design a BCD-to-Excess-3 code converter using basic gates.   **(5)**

c.  Explain the features of Computer Aided Design tools in digital systems.   **(5)**

**Q.3**   a.  Use Boolean algebra to prove the following:
$a'b' + ab + a'b = a' + b$   **(5)**

b.  Mention limitations of two-level networks in combinational systems.   **(5)**

c.  Write short notes for the following:
(i)  Serial Binary Adder.
(ii)  Threshold switching function.   **(6)**

**Q.4**   a.  Write a program in VHDL to implement the following ALU operations:
(i)  Add                    (ii)  Subtract
(iii) Multiply              (iv)  Divide   **(6)**

b.  Explain the behavioral and structural modeling in VHDL.                    **(5)**

c.  Explain delta delay and transport delay in VHDL.                           **(5)**

**Q.5**   a.  Explain the role of multiplexer as a Universal Combinational Module.    **(5)**

b.  Give the representation of n-bit register and mention its applications. Label
data and control signals in a *n-bit* register.                           **(6)**

c.  Compare PAL and GAL devices.                                               **(5)**

**Q.6**   a.  Explain hazards and race in asynchronous sequential machines. Give an
illustration.                                                             **(7)**

b.  Design a two input, two output sequence detector to detect a sequence 0101.  **(6)**

c.  Mention the features of flow table reduction in asynchronous sequential
machines.                                                                 **(3)**

**Q.7**   a.  Design data subsystem for to displaying values from 1 to 10. Draw the
relevant block diagram with data and control signals.                     **(7)**

b.  Compare the features of microprogrammed controller with respect to
controller implemented on a fixed network.                                **(5)**

c.  Give an example to illustrate horizontal and vertical encoding in control fields of
microinstruction.                                                         **(4)**

**Q.8**   a.  Determine the minimal state table that is equivalent to the following:    **(5)**

|            | *Input* |        |
| ---------- | ------- | ------ |
| *PS*       | *x = 0* | *x = 1* |
| *a*        | *f, 0*  | *b, 0* |
| *b*        | *d,0*   | *c ,0* |
| *c*        | *f, 0*  | *e, 0* |
| *d*        | *g,1*   | *a, 0* |
| *e*        | *d,0*   | *c, 0* |
| *f*        | *f, 1*  | *b, 1* |
| *g*        | *g,0*   | *h, 1* |
| *h*        | *g,1*   | *a, 0* |
|            | *NS, z* |        |

b.  Explain the working of asynchronous sequential machine and give its
representation.                                                           **(6)**

c.  Explain the role of functional decomposition in combinational systems.     **(5)**

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**Q.9** a. Write short notes from any **THREE** of the following:

   (i)   Microprogrammed Controller
   (ii)  Storage modules of a Data subsystem
   (iii) Process statement in VHDL
   (iv)  Programmable Sequential Arrays                          **(3×4 = 12)**

   b. Give an example to illustrate multiple output switching function and their
   minimization.                                                          **(4)**