ROLL NO. _____

Code: AE09 **Subject: ANALOG & DIGITAL ELEC S**

AMIETE – ET (OLD SCHEME)

Time: 3 Hours **OCTOBER 2012** **Max. Marks: 10**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. The common mode rejection ratio of an op-amp is
(A) much larger than unity **(B)** smaller than unity
(C) unity **(D)** None of these

b. An ideal amplifier has
(A) Noise figure of 0 dB **(B)** Noise figure of more than 0 dB
(C) Noise figure of unity **(D)** Noise figure of less than 1 dB

c. Output voltage of a comparator is
(A) Sine wave **(B)** Triangular wave
(C) Square wave **(D)** Sawtooth wave

d. An ideal current controlled voltage source has
(A) $R_i = \infty,\ R_o = \infty$ **(B)** $R_i = 0,\ R_o = \infty$
(C) $R_i = 0,\ R_o = 0$ **(D)** $R_i = \infty,\ R_o = 0$

e. As compared to TTL, ECL has
(A) Lower power dissipation **(B)** Lower propagation delay
(C) High propagation delay **(D)** High noise margin

f. The number of input and output in a full adder are
(A) 2 and 1 **(B)** 2 and 2
(C) 3 and 3 **(D)** 3 and 2

g. Which of the following counter results in least delay
(A) Ring counter **(B)** Ripple counter
(C) Synchronous counter **(D)** Asynchronous counter

h. Storage time of a transistor is the time taken for the collector current to fall t
(A) 90% from maximum value
(B) 10% from maximum value
(C) 10% to 90% from maximum value
(D) 50% from maximum value

i. Which memory requires periodic recharging
(A) All ROMS **(B)** All RAMS
(C) Static RAM **(D)** Dynamic RAM

j. In CCD
(A) A small charge is deposited for logical 1
(B) A small charge is deposited for both 1 & 0 logical
(C) A small charge is deposited for logical 0 and large charge for logical 1
(D) None of these

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Draw the circuit of a Widlar current source and explain its operations. **(8)**

b. When a voltage $V_1 = +40\mu V$ is applied to the non inverting input terminal and a voltage $V_2 = -40\mu V$ is applied to the inverting input terminal of an op-amp, an output voltage $V_0 = 100mV$ is obtained. But when $V_1 = V_2 = +40\mu V$, one obtain $V_0 = 0.4mV$. Calculate the voltage gain for the difference and common-mode signals and the common-mode rejection ratio. **(8)**

Q.3 a. What are switching capacitor filter? Mention their advantages. **(8)**

b. Explain the operation of first order low pass Butter-worth filter. **(8)**

Q.4 a. Determine the output voltage caused by each bit in a 6 bit ladder if the input level are 0=0V and 1=+16V. Determine the resolution and full scale output of this circuit. Also find out the voltage from the digital input of 101011. **(8)**

b. Show how a logarithmic amplifier can be built with an op-amp. **(8)**

Q.5 a. Explain how does Schottky barrier diode differ from a silicon junction diode. **(8)**

b. Describe following terms with respect to logic circuits:
(i) Noise margin (ii) Fan in – Fan out
(iii) Propagation delay (iv) Power delay product **(8)**

Q.6 a. Draw the circuit diagram of a TTL NAND gate and explain its operation. **(10)**

b. Compare the relative merits of TTL, ECL and CMOS logic family. **(6)**

Q.7 a. Minimize using kmap $f(A,B,C,D) = \sum m(0,2,3,5,7,12,15) + \sum d(1,4,8,11)$ a implement the simplified function using NAND gates only. **(8)**

b. Design a 1 bit comparator which can compare A=B, A>B, A<B. **(8)**

Q.8 a. Show the D flip flop and T flip flop implementation from J-K flip flop. **(8)**

b. What is a Shift Register? Explain Universal Shift register operation with an example. **(8)**

Q.9 Write short note on any **TWO:**

(i) Dynamic RAM Cells
(ii) CCDs
(iii) Bipolar Memory Cell

(8×2)