Subject: MICROPROCESSORS & MICROCO

ROLL NO.

Diplete – Et/cs (New Scheme)

Time: 3 Hours

Code: DE60/DC68

JUNE 2012

OCOA Max. Marks: 100

 (2×10)

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions, answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

Q.1 Choose the correct or the best alternative in the following:

- a. In Intel's 8085 microprocessor, the range of operating frequency is _____.
 - (A) 500 Hz to 3 MHz(C) 50 KHz to 3 MHz

(**B**) 500 KHz to 3 MHz (**D**) 5 KHz to 3 MHz

b. Intel's 8085 microprocessor has_____ address lines and can address a maximum of _____ memory.

(A) 8, 64 KBytes	(B) 16,8 KBytes
(C) 32, 64 KBytes	(D) 16, 64 KBytes

c. Intel's 8085 microprocessor has instruction size ranging from _____to ____.

(A) 0 to 4 bytes	(B) 0 to 3 bytes
(C) 1 to 3 bytes	(D) 1 to 6 bytes

d. In Intel's 8255, the specialty of Port-C is _____.

(A) BSR mode and two 4-bit ports(B) BSR mode and two 8-bit ports(C) BSR mode and Bidirectional I/O (D) None of the above

- e. In Intel's 8253, the following statement is FALSE.
 - (A) Operating frequency ranges from 0 Hz to 2 MHz
 - (B) The three timers T1, T2 and T3 are independently controlled
 - (C) 6 modes of operation including Mono-shot and square wave generation
 - (D) None of the above

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	Intel's 8259, the INT signal is generated based on the inputs available f	CUM
) ISR, IMR, IRR and Priority resolver) IMR and, IRR only) Priority resolver alone) ISR, IMR and Priority resolver, but not IRR	HIBOUINU.com
	ntel's 8051 MC can be interfaced with a maximum data memory ar code memory.	ıd
	(a) 64 Kbytes, 64 Kbytes (b) 16 Kbytes, 64 Kbytes (c) 64 Kbytes, 32 Kbytes (c) 8Kbytes, 64 Kbytes	
	Intel's 8051 MC status register, 'F0' bit is and 'Ov' bit is	
) not used, over flow flag) over flow flag, not used) general purpose flag, over flow flag) general purpose flag, not used	
	Intel's 8051 MC, size of SP register is and PC register is	
	a) 16 bits, 16 bits (B) 16 bits, 8bits b) 8bits, 16 bits (D) 8bits, 8bits	
	Intel's 8051 MC, the following statement is TRUE regarding the two mers.	
) T1 is an up-counter and T2 is a down-counter) Both T1 and T2 have4 modes of operation c) T1 is a down-counter and T2 is an up-counter c) T1 has 4 modes of operation and T2 has 3 modes of operation 	
	Answer any FIVE Questions out of EIGHT Questions. Each question carries 16 marks.	
Q.2	What are the salient features of the INTEL's-8085 microprocessor? Explain with a neat block diagram.	(10)
	 /hat are the functions of the following pins of INTEL's-8085?) READY i) SID and SOD ii) HOLD and HLDA 	(6)

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- 0.3 a. What are the addressing modes available in INTEL's-8085? Explain with example for each.
- StudentBounty.com b. What are the different instructions types available in INTEL's-8085? Explain with an example for each.

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(8)

- a. Correct the following instructions if necessary and indicate its addressing 0.4 mode. (8) (i) MOV B, B (ii) OUT 1234h (iii) LDAX, 1234h (iv) PUSH A
 - b. Using 8085 instructions, write an assembly language program to interchange the contents of two arrays of bytes starting from locations "x" and "y". Write necessary comments. (8)
 - **Q.5** a. When interrupted by an external interrupt what happens to the program execution in INTEL's-8085? Explain. (8)
 - b. What are the interrupt related instructions available in INTEL's-8085? Explain
- **Q.6** a. What are the modes of operation for INTEL's-8255? Explain. (8)
 - b. Interface a logic controller to MP-8085 and write an assembly language program to realize a full adder. Write necessary comments. (8)
- 0.7 a. Using a neat block diagram explain the internal architecture of INTEL's-8259. (8)
 - b. What is a DMA? Explain Burst mode and cycle stealing methods briefly. (8)
- 0.8 Using a neat block diagram explain the internal architecture of INTEL's-8253. a. (10)
 - b. What are the features of INTEL's 8251 USART? (6)
- **Q.9** a. What are the salient features of 8051 micro-controller? Explain with a neat block diagram. (8)
 - b. Write an assembly language program to interchange two blocks of data bytes using 8051 instructions. Write necessary comments for the same. (8)

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