ROLL NO. _____

Code: DE58 / DC58 **Subject: LOGIC DESIG**

DipIETE – ET/CS (NEW SCHEME)

Time: 3 Hours **JUNE 2012** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. If a digital system that uses N-bits can go through_____

(A) N-counts. **(B)** 2N-counts.
(C) 2^N-counts. **(D)** 2^N-1 counts.

b. Nibble means group of_____

(A) 8-bits. **(B)** 4-bits.
(C) 12-bits. **(D)** 16-bits.

c. The device used to store 4-bit of data is known as_____

(A) flip-flop. **(B)** MOD 4 counter.
(C) MOD 4 synchronous counter. **(D)** 4-bit shift register.

d. Representation of signed decimal number -9 in the 2's complement form is_____

(A) 01101 **(B)** 10111
(C) 11001 **(D)** 11100

e. Adder that adds two input bits is known as_____

(A) half adder. **(B)** full adder.
(C) series adder. **(D)** parallel adder.

f. If the input and output frequencies of a digital counter is 10 kHz and 2 kHz respectively. What is the modulus of the counter?

(A) MOD 10. **(B)** MOD 2.
(C) MOD 5. **(D)** MOD 20.

g. A 2K ROM has_____

(A) 8 address lines. **(B)** 10 address lines.
(C) 12 address lines. **(D)** 11 address lines.

h. A combinational circuit has_____

(A) only memory elements.
(B) only non memory elements.
(C) both memory and non memory elements.
(D) less memory elements.

i. Alphanumeric codes are_____

(A) Un-weighted codes. **(B)** 8-4-2-1 codes.
(C) Weighted codes. **(D)** None of the above.

j. The gate that is used in parity generation and correction is_____

(A) NAND **(B)** NOR
(C) EX-OR **(D)** NOT

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Describe the relative advantages of Parallel and Serial data transmission. **(6)**

b. Perform the following conversion:
(i) $(123)_{10}= (?)_8$
(ii) $(101011)_2=(?)_{16}$
(iii) $(7A9)_{16}=(?)_8$ **(6)**

c. Write a short note on parity bit. **(4)**

Q.3 a. State and prove DeMorgan's theorems. **(6)**

b. For the Boolean function $y = \overline{M + N} + \overline{P}Q$, construct the logic circuit using AND, OR and INVERTERs **(4)**

c. Simplify the following Boolean function using K-map
$f(A, B, C, D) = \sum m(3,4,5,6,7,12,13)$ **(6)**

Q.4 a. With neat circuit diagram explain the edge triggered JK-flip-flop. **(8)**

b. What is Potential Timing problem in flip-flop circuits? Explain it with the help of a Flip-Flop circuit. **(8)**

Q.5 a. Perform the subtraction of the following in the 2's complement system.
(i) 15-8
(ii) 1010-10110 **(4)**

b. Add 45 and 67 in BCD code. **(3)**

c. Design Full Adder Circuit using gates. **(9)**

Q.6 a. Design a mod-13 Asynchronous Counter. **(8)**

b. Design a counter that counts from 0011 to 0111 using IC 74190 synchronous decade counter. **(8)**

Q.7 a. Define a multiplexer and draw the circuit diagram of 4-input multiplexer. Show how this multiplexer can be used to realize 8-input multiplexer. **(10)**

b. Draw and explain BCD to 7 segment decoder. **(6)**

Q.8 a. Design a synchronous counter that has the sequence 000, 010, 101, 110 and repetition. The underired (unused) states 001, 011, 100 and 111 must always go to 000 on the next clock pulse. **(10)**

b. Draw the circuit diagram and Truth Table of 3-bit Johnson counter. **(6)**

Q.9 a. Explain the basic operating principles for Memory Systems. **(8)**

b. Draw the structure of a Dynamic RAM and explain its operation. **(8)**