

AMIETE – ET (NEW SCHEME)

Time: 3 Hours

JUNE 2012

Max. Marks: 160

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. Channel exists between source and drain without gate voltage is

- | | |
|--------------------------|------------------------|
| (A) Enhancement type MOS | (B) Depletion type MOS |
| (C) BiCMOS | (D) CMOS |

b. Limitation of MOS Technology is

- | | |
|-----------------------------|------------------------|
| (A) High power dissipation | (B) Compactness |
| (C) Load driving capability | (D) High Noise margin. |

c. Electron Transit time T_{sd} is inversely proportional to

- | | |
|--------------|--------------|
| (A) V_{gs} | (B) V_{ds} |
| (C) L | (D) E_{ds} |

d. The constant term K in I_{ds} expression is determined by

- | | |
|--|---|
| (A) $\frac{\epsilon_{ins} \epsilon_0 WL}{D}$ | (B) $\frac{\epsilon_{ins} \epsilon_0}{D}$ |
| (C) $\epsilon_{ins} \epsilon_0 \frac{W}{L}$ | (D) $\frac{\epsilon_{ins} \epsilon_0}{D} \mu$ |

e. Figure of merit ω_0 is directly proportional to

- | | |
|-------------------------------|---------------------------|
| (A) Width of channel | (B) Length of channel |
| (C) Mobility of electron/hole | (D) Electron Transit term |

Code: AE74**Subject: VLSI DESIGN**

f. Pull-up to pull-down ratio for an nMOS inverter driven by another nMOS inverter is

- (A) 6:1 (B) 8:1
(C) 16:1 (D) 4:1

g. Latch-up in CMOS can be reduced by

- (A) Increasing substrate doping level (B) Decreasing substrate doping level
(C) Increasing the value of R_s (D) Increasing the value of R_p

h. Minimum spacing between two diffusion layer is

- (A) 1λ (B) 2λ
(C) 3λ (D) 4λ

i. nMOS inverter with 4:1 Z_{pu} / Z_{pd} ratio has V_{DD} to G_{ND} ON resistance

- (A) 10K (B) 40K
(C) 50K (D) 90K

j. Total delay of cascaded CMOS inverter for N even is

- (A) $3.5 N\tau$ (B) $2.5 N\tau$
(C) $5 N\tau$ (D) $7 N\tau$

**Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.**

Q.2 a. With neat diagram explain Three modes of operation of nMOS enhancement mode Transistor (8)

b. With neat sketch explain the CMOS N-well Fabrication process. (8)

Q.3 a. Derive an expression for Pull-up to Pull-down ratio for an n-MOS inverter driven by another n-MOS inverter. (8)

b. Draw CMOS inverter circuit. Also compare CMOS & Bipolar transistor parameter. (8)

Q.4 a. Write circuit and Stick diagram for (8)
(i) 2 IP CMOS NOR gate
(ii) 2 IP EXOR gate using CMOS

b. Briefly explain λ based design rules for (8)
(i) Transistor
(ii) Wire

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- Q.5** a. Define sheet resistance and standard unit of capacitance (4)
- b. Calculate R_{on} and C_g of a n-MOS inverter in terms of R_s and C_g respectively.
Assume $\frac{Z_{pu}}{Z_{pd}} = 4:1$. (4)
- c. Write a short note on driving large capacitive loads. (8)
- Q.6** a. Obtain Scaling factor for (10)
(i) Gate capacitance (ii) Frequency
(iii) Power dissipation (iv) Current density
- b. Design 4:1 MUX using Transmission gate. (6)
- Q.7** a. Design 4×4 crossbar switch using MOS switch. (8)
- b. Implement adder element logic circuit using n-Switch based Multiplexer. (8)
- Q.8** a. Draw the structure of Six- transistor static CMOS memory-cell and explain its Read and Write operations. (10)
- b. Discuss about Ground rules for successful design of VLSI chip. (6)
- Q.9** a. Explain briefly various design styles used in VLSI design. (6)
- b. Define Controllability and observability. (4)
- c. Write Sequential logic circuit containing scan path for testing and explain its operation briefly. (6)