ROLL NO. _____

**Code: AE53/AC53/AT53 Subject: ELECTRONIC DEVICES & [illegible]TS**

## AMIETE – ET/CS/IT (NEW SCHEME)

**Time: 3 Hours** **JUNE 2012** **Max. Marks: 100**

***PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.***

**NOTE: There are 9 Questions in all.**

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions, answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

**Q.1 Choose the correct or the best alternative in the following: (2×10)**

a. In an RC phase shift oscillator circuit using an ideal voltage amplifier the frequency of oscillation is 1 KHz. If $C = 0.01\mu F$, then R is equal to _____

**(A)** 11.25K **(B)** 6.5K
**(C)** 15.92K **(D)** 20.45K

b. In a full wave rectifier supplied from a transformer with centre tapped secondary, the minimum reverse breakdown voltage that each diode should have, when the input to the transformer is $V_m \sin \omega t$, is _____.

**(A)** $2 V_m$ **(B)** $V_m$
**(C)** $V_m/2$ **(D)** $4 V_m$

c. In an NPN transistor whose $\beta$ is 49 and $I_{CO}$ is 2 μA, if $V_{CE}$ is equal to 4 V and $I_B = 0$, the collector current is equal to _____.

**(A)** 2 μA **(B)** 0.04 mA
**(C)** 0 **(D)** 0.1 mA

d. In a voltage divider biasing circuit for a transistor with $\beta = 49$, $R_E = 5\ K\Omega$ and $R_{TH} = 60\ K\Omega$, the bias stabilization factor $S(I_{CO})$ is equal to_____.

**(A)** 11.48 **(B)** 10.48
**(C)** 10.27 **(D)** 11

e. Three amplifiers of voltage gains 20 dB, 26 dB and 32 dB are cascaded to obtain an output voltage of 2 V. The input voltage needed is equal to_____.

**(A)** 0.25 mV **(B)** 0.25 V
**(C)** 0.25 μV **(D)** 2 V

f. If a transistor has $h_{ie} = 1.2\ K\Omega$, $h_{fe} = 50$, $h_{re} = 3\times10^{-4}$ and $h_{oe} = 40$ A/V its $h_{ib}$ = _____.

**(A)** 12 Ω **(B)** 23.5 Ω
**(C)** 36.5 Ω **(D)** 48 Ω

g. In crystal oscillator, a piezoelectric crystal is used to obtain high stability _____.

**(A)** frequency **(B)** amplitude
**(C)** bias voltage **(D)** wave shape

h. Maximum power transfer theorem states that the maximum power from a source is delivered to a load $R_L$, when its output resistance $R_O$ is equal to_____.

**(A)** $R_L/2$ **(B)** $2R_L$
**(C)** $R_L$ **(D)** 0

i. In a typical UJT oscillator circuit, if $R_T$ = 40 KΩ, $C_T$=0.12 μF and the UJT has η = 0.7, the frequency of oscillation is equal to_____.

**(A)** 33.2 Hz **(B)** 173 Hz
**(C)** 33.2 kHz **(D)** 173 kHz

j. Amplifier $A_1$ has its lower and upper cut-off frequencies as 50 Hz and 100 kHz respectively, while the second Amplifier $A_2$ has its lower and upper cut-off frequencies as 5 kHz and 1 MHz. If $A_1$ and $A_2$ are cascaded, the lower and upper cut-off frequencies of the cascaded amplifier are _____.

**(A)** 50 Hz and 1 MHz **(B)** 5 kHz and 100 kHz
**(C)** 5 kHz and 1 MHz **(D)** 50 Hz and 100 kHz

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**Answer any FIVE Questions out of EIGHT Questions.**
**Each question carries 16 marks.**

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**Q.2** a. For the RC circuit shown in Fig.1, derive the expression for the output voltage $V_o$ across the resistor R, if the input is $V_i u(t)$. **(8)**

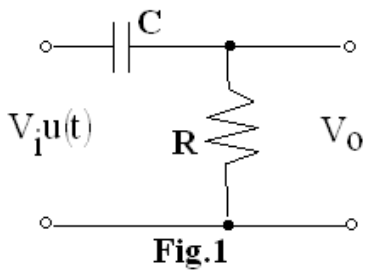

Fig.1

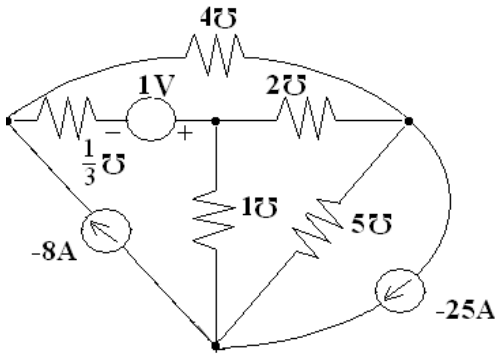

Fig.2

b. For the circuit shown in Fig.2, find the voltages across 2 mho and 4 mho conductances, using nodal analysis. **(8)**

**Q.3** a. Write short note on
(i) Tunnel Diode (ii) Zener Diode **(8)**

b. In the 6 V Zener regulator circuit of Fig.3, calculate the value of R, so that the circuit performs satisfactorily under all the given conditions. [ $I_z(\min) = 6$ mA, $P_d(\max)$ for the zener = 1164 mW] **(8)**

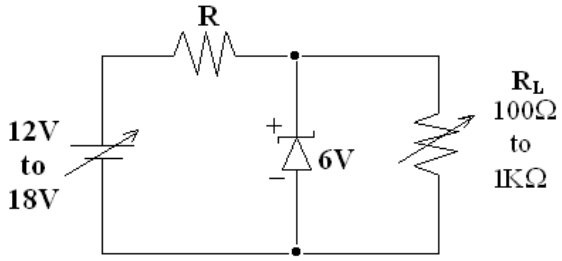


Fig.3

**Q.4** a. Draw the input and output characteristics of a transistor in common base configuration and explain how a transistor could be used as an amplifier. **(8)**

b. Explain the construction and operation of a JFET with suitable diagram, and draw its output characteristics. **(8)**

**Q.5** a. In the Darlington emitter follower circuit of Fig.4, determine the input impedance $R_{in}$, voltage gain $v_o/v_i$ and the output impedances $R_o$. **(9)**

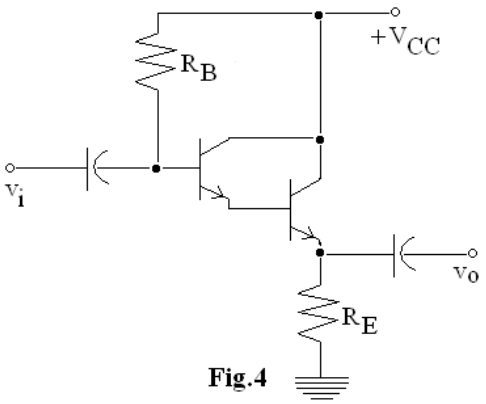


Fig.4

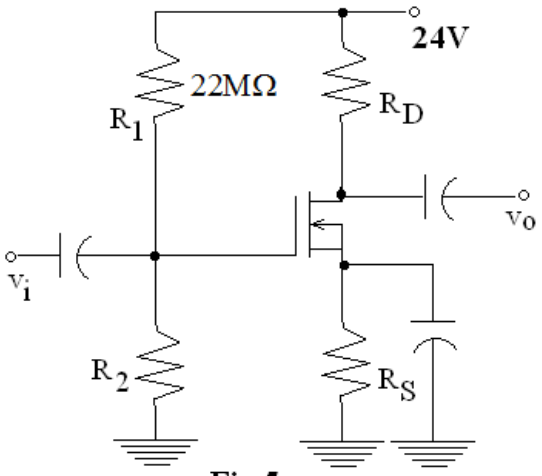


Fig.5

b. Design a potential divider biasing network for a DEMOSFET shown in Fig.5, with $I_{DSS}$ = 10 mA and $V_P$ = –4V, so as to place the operating point at $I_{DQ}$ = 2.5 mA. Assuming $R_D$ = 2.5 $R_S$, determine the voltage gain $v_o/v_i$ of the amplifier. **(7)**

**Q.6** a. A cascade of two identical N-channel JFETs, with $g_m$ = 1ms and $r_d$ = 40 kΩ, is shown in Fig.6. Write the ac equivalent circuit and then calculate the voltage gain of each stage and the overall voltage gain, $A_{v_o}$. If the two stages are interchanged, what will be the new overall voltage gain, $A_{v_o}$. **(8)**

b. In the RC coupled amplifier circuit of Fig.7, determine the lower cut-[illegible] frequency, $f_{L_{CE}}$ due to the bypass capacitor, $C_E$. **(8)**

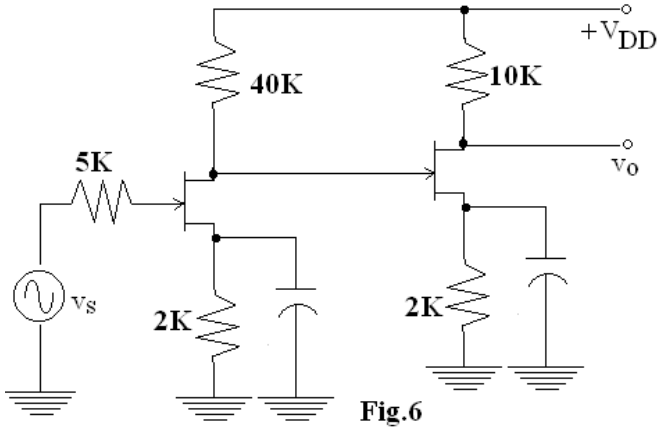


Fig.6

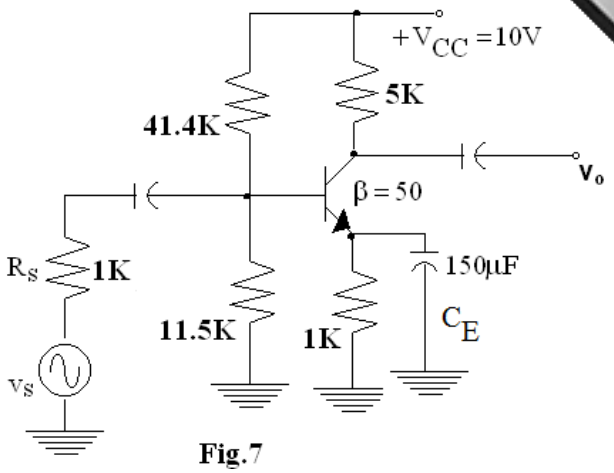


Fig.7

**Q.7** a. Prove that the maximum conversion efficiency of a class A power amplifier is 50%. **(8)**

b. A complementary symmetry class B output stage operated from a single supply voltage of +24 V, is to deliver power to a loudspeaker load of 4 Ω. If the input voltage is 10 sinωt, calculate the ac power output, dc power input, conversion efficiency and power dissipation in each of the transistors. **(8)**

**Q.8** a. State and explain Barkhausen criteria for sustained oscillations. Discuss the effect of loop gain |Aβ| on the amplitude of oscillations. **(8)**

b. Draw the circuit of a Wien's bridge oscillator using an ideal op amp. Obtain the expression for the frequency of oscillation. **(8)**

**Q.9** a. Write short notes on the semiconductor fabrication processes (i) Diffusion and (ii) Ion Implantation. **(10)**

b. Calculate the chip area needed for a 250 pF MOS capacitor, if the thickness of $SiO_2$ layer is 500 $\mathring{A}$ and its relative dielectric constant is 3.5. $(\epsilon_o = 54 \times 10^{-12}\ Fm^{-1})$. **(6)**