

NOTE: There are 9 Questions in all.

- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. Substrate in nMOS FET is

- (A) N type (B) P type
(C) PN type (D) None

b. In depletion mode FET devices channel is established when

- (A) $V_{gs} = V_{DD}$ (B) $V_{gs} > V_t$
(C) $V_{gs} = 0$ (D) $V_{gs} > V_{DD}$

c. Transit time τ_{sd} is

- (A) $\frac{\text{Valocity}}{\text{Channel length}}$ (B) $\frac{\text{Channel length}}{\text{Velocity}}$
(C) $\frac{\text{Charge}}{\text{Electric field}}$ (D) $\frac{\text{Channel length}}{\text{Electric field}}$

d. Pull-up to Pull-down ratio $\frac{Z_{pu}}{Z_{pd}}$ for nMOS inverter driven by another nMOS inverter is

- (A) 8:1 (B) 4:1
(C) 6:1 (D) 16:1

e. Implant in depletion type transistor is indicated by dotted square of dimension

- (A) $6\lambda \times 6\lambda$ (B) $8\lambda \times 8\lambda$
(C) $4\lambda \times 4\lambda$ (D) $16\lambda \times 16\lambda$

f. Total channel resistance of nMOS inverter when it is ON is

- (A) 20 k Ω (B) 30 k Ω
(C) 40 k Ω (D) 50 k Ω

g. Static power dissipation is low in _____ inverter.

- (A) PMOS (B) nMOS
(C) CMOS (D) nMOS & CMOS

h. Scaling factor for Gate Area is

- (A) $1/\beta^2$ (B) $1/\alpha^2$
(C) $1/\beta$ (D) $1/\alpha$

i. In nMOS pass Transistor _____ level output is degraded.

- (A) Tristate (B) High and low
(C) Low (D) High

j. D-algorithm is used to test _____ circuit

- (A) Combinational (B) Sequential
(C) Both (A) and (B) (D) Flip-Flops

**Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.**

Q.2 a. Write the cross-sectional view of nMOS enhancement and depletion mode Transistor indicating all the layers and terminals. (6)

b. With neat sketch explain the P-Well Fabrication process. (10)

Q.3 a. Derive the expression for I_{ds} starting from transit time. (8)

b. What are the different types of pull-ups are used in MOS circuit? Explain briefly with neat sketch. (8)

Q.4 a. Draw & explain the circuit diagram and stick diagram for logic function $\bar{f} = x + yz$ (8)

b. With neat diagram explain design rules for wires and contact? (8)

Q.5 a. Define sheet resistance and standard unit of capacitance. (4)

b. Derive the expression for total delay when N inverters are cascaded to drive large capacitive load (6)

c. Calculate the total capacitance for the Fig.1. (6)

Q.6 a. Derive the scaling factors for
(i) Gate capacitance
(ii) Operating frequency
(iii) Power dissipation (8)

b. Explain how transmission gate eliminates degradation of output levels.
Write the circuit of 4:1 MUX using Transmission gate. (8)

Q.7 a. Explain design methodology steps to design complex VLSI circuit. (6)

b. Design a 4 bit adder and obtain the expression for Sum, Carry & Half Sum. (10)

Q.8 a. Draw and explain the circuit and stick diagram of nMOS-pseudo static memory cell. (8)

b. Discuss the methods for optimisation of area, power dissipation and time of CMOS inverter. (8)

Q.9 a. Explain the method for detection of stuck at faults using sensitized path based testing technique. Determine the test vector for SA1 detection for the circuit shown in Fig.2. (8)

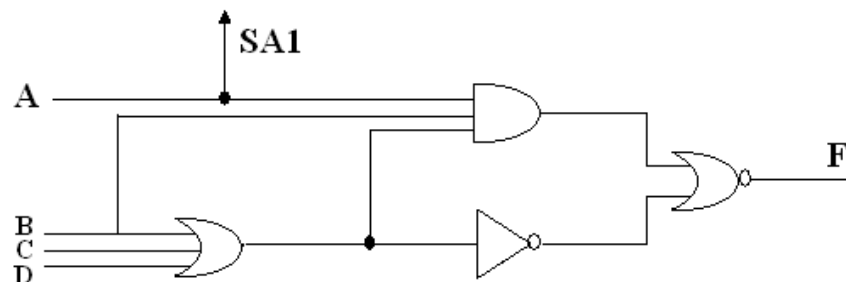


Fig.2

- b. Draw the circuit of BILBO and explain briefly. (8)