ROLL NO. _____

Code: AE68 **Subject: EMBEDDED SYSTEMS DES**

AMIETE – ET (NEW SCHEME)

Time: 3 Hours **DECEMBER 2011** **Max. Marks: 100**

NOTE: There are 9 Questions in all.

- **Please write your Roll No. at the space provided on each page immediately after receiving the Question Paper.**
- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. Microcontroller is an

(A) ASIC **(B)** ASIP
(C) Customized FPGA **(D)** All the above

b. Tasks must be able to communicate with one another to

(A) Coordinate their activities. **(B)** Share data
(C) Discover error conditions **(D)** Both **(A)** and **(B)**

c. The queues, mailboxes, and pipes are

(A) Same in all RTOS **(B)** Vary from one RTOS to another
(C) Only few variations **(D)** None of the above

d. The CACHE is usually designed using SRAM rather than DRAM because

(A) Cost
(B) Performance
(C) Appears on the same chip as a processor
(D) Both **(A)** and **(B)**

e. The difference between Synchronous and Enhanced Synchronous DRAM is

(A) Clocking **(B)** Bus Size
(C) Control Signals **(D)** None of the above

f. Real time system engineers avoid C memory allocation functions because

(A) Typically Slow **(B)** Execution Times are un-predictable
(C) Both **(A)** and **(B)** **(D)** None of the above

g. The Sensor networks are large-scale embedded systems that may contain

(A) Millions of nodes **(B)** Billions of nodes
(C) Thousands of nodes **(D)** both **(A)** and **(C)**

h. A node that transmits data among different types of networks is known as a

(A) Router **(B)** Switch
(C) Super Node **(D)** Hyper Node

i. In the write through technique, whenever we write to the cache, we also write to

(A) Main memory **(B)** I/O port
(C) Both **(A)** and **(B)** **(D)** None of the above

j. Components that are commonly used in embedded software

(A) The State Machine **(B)** The Circular Buffer
(C) The Queue **(D)** All the above

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. What is a design metric? List pair of design metrics that may compete with one another, providing an intuitive explanation of the reason behind the competition. **(8)**

b. List and define the three main IC technologies. What are the benefits of using each of the three different IC technologies? **(8)**

Q.3 a. Explain the programmer and Operating System considerations in ESD. **(8)**

b. What are ASIP's? Explain popular ASIP's used in ESD. **(8)**

Q.4 a. Explain how PWM works and show the interface structure controlling a DC motor with a PWM. **(8)**

b. Given an analog input signal whose voltage should range from 0 to 15 volts, and an 8-bit digital encoding, calculate the correct encoding for 5 volts. Then trace the successive-approximation approach to find the correct encoding. **(8)**

Q.5 a. Explain the difference between port-based I/O and bus-based I/O. **(6)**

b. Explain the four popular serial bus protocols. **(10)**

Q.6 a. Write a short note on RTOS semaphores **(8)**

b. Explain TASKS & TASKS STATES in RTOS. **(8)**

Q.7 a. What is cache mapping? Explain the direct mapping, fully associative mapping and set associative mapping techniques. **(8)**

b. Draw and explain the Basic DRAM architecture. **(8)**

Q.8 a. Explain the standard features of events in RTOSs context. **(8)**

b. In RTOS environments, what are the rules Interrupt routines must follow that do not apply to task code? **(8)**

Q.9 a. List the advantages of task structure in an ESD. **(8)**

b. Discuss how to encapsulate Semaphores and Queues. **(8)**