Subject: LINEAR ICs & DIGITAL ED

**ROLL NO.** 

# AMIETE – ET/CS/IT (NEW SCHEME)

**Time: 3 Hours** 

# **DECEMBER 2011**

AL ED Max. Marks: 100

 $(2 \times 10)$ 

NOTE: There are 9 Questions in all.

- Please write your Roll No. at the space provided on each page immediately after receiving the Question Paper.
- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions, selecting at least TWO questions from each part, each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

#### Q.1 Choose the correct or the best alternative in the following:

a. The bandwidth of an ideal Op-Amp is

( <b>A</b> ) 0	<b>(B)</b> 1MΩ
( <b>C</b> ) ∞	<b>(D)</b> 80KΩ

b. If the change in voltage is  $\Delta V = 2.4 V$  and rise time 4µs then slew rate of the Op-Amp is

(A) $0.4 V/\mu s$	<b>(B)</b> $0.5 \mathrm{V/\mu s}$
(C) $0.1 V/\mu s$	( <b>D</b> ) $0.6 V/\mu s$

c. The output voltage of an Op-Amp integrator is

(A) $V_0(t) = -R_1C_f \int V_i(t)dt$	<b>(B)</b> $V_0(t) = -R_1 \int V_i(t) dt$
(C) $V_0(t) = -\frac{1}{R_1 C_f} \int V_i(t) dt$	<b>(D)</b> $V_{O}(t) = \int V_{i}(t) dt$

d. The output frequency of a triangular wave generator is given by

(A) 
$$f_0 = \frac{R_1 R_3}{4R_2 C_1}$$
  
(B)  $f_0 = \frac{R_3}{4R_1 C_1 R_2}$   
(C)  $f_0 = \frac{1}{4R_1 R_2 R_3 C_1}$   
(D)  $f_0 = \frac{R_2}{4R_1 R_3 C_1}$ 

AE54/AC54/AT54/ DEC \_ 2011

Subject: LINEAR ICs & DIGITAL ED

**ROLL NO.** 

studentBounts.com e. The equivalent weight of the LSB in a 4 bit variable resistive divider DAC is

(A) 
$$\frac{1}{4}$$
 (B)  $\frac{1}{16}$   
(C)  $\frac{1}{15}$  (D)  $\frac{1}{32}$ 

- f. An XOR gate gives a high output
  - (A) if there are odd number of 1's in input.
  - (B) if there are odd number of 0's in input.
  - (C) if there are even number of 1's in input.
  - (**D**) if there are even number of 0's in input.
- g. For checking the parity of a digital word, it is preferable to use

(A) AND gates	( <b>B</b> ) NAND gates
(C) EXOR gates	<b>(D)</b> NOR gates

h. The maximum number of binary states that a counter can have if it uses 8 FlipFlops is

(A) 8	<b>(B)</b> 16
( <b>C</b> ) 64	<b>(D)</b> 256

i. To obtain 10 KHz square wave from 1 MHz clock, ÷by counter to be used is

(A) $\div$ by 10 counter	<b>(B)</b> $\div$ by 100 counter
(C) $\div$ by 1000 counter	$(\mathbf{D}) \div by 1 counter$

j. What will be the output voltage of a 6 bit binary ladder DAC with input 101001 if V(0) = 0 and V(1) = 10 V

( <b>A</b> ) 6.41V	<b>(B)</b> 0.0156V
( <b>C</b> ) 6.4V	<b>(D)</b> 4.1V

#### PART (A) Answer At least TWO questions. Each question carries 16 marks.

- a. Derive the output expression for a differential amplifier using Op-Amp. Using Q.2 the same, derive the expression for CMRR of the differential amplifier. (4+4)
  - b. Explain the method of frequency compensation using dominant pole compensation method. (8)

AE54/AC54/AT54/DEC = 2011

### Subject: LINEAR ICs & DIGITAL ED

**ROLL NO.** 

- StudentBounty.com 0.3 a. A square wave of frequencies 100 Hz, 10 KHz and 1MHz are applied as input to an Op-Amp voltage follower. The Op-Amp has a slew rate of  $1V/\mu s$ . Show the output waveforms for these 3 cases & explain.
  - b. Explain the operation of a precision full wave rectifier with waveforms.
- **Q.4** a. In an Op-Amp Schmitt trigger circuit  $R_2 = 110K\Omega$ ,  $R_1 = 60K\Omega$ ,  $V_{ref} = 2V$  $V_i = 1V pp$  sinewave saturation voltage =  $\pm 15V$ . Determine the threshold voltages V<sub>LT</sub> & V<sub>UT</sub>. (8)
  - b. Draw a sample and hold circuit. Explain its operation and indicate its uses. (8)
- a. (i)Draw the diagram and explain the operation of a fixed regulator used as **Q.5** adjustable regulator. (ii)Using the above circuit with IC 7805. design for  $V_0 = 7.5V$ ,  $I_0 = 4.2mA$ ,  $V_R = 5V$ ,  $I_{R1} = 25mA$ . (4+4)
  - b. (i) Explain the operation of R-2R ladder DAC. (ii) Calculate the output voltage for  $10000000_2$  for R-2R ladder DAC  $R_F = R = 5K\Omega$  for a reference voltage of 5V. (4+4)

## PART (B) Answer At least TWO questions. Each question carries 16 marks.

- **Q.6** a. Perform the following:
  - (i) Add 120 with -55 in 2's complement method.
  - (ii) Subtract -68 from -15 in 2's complement.
  - (iii)  $(24.6)_{10} = ()_2$
  - (iv)  $(0.640625)_{10} = ()_8$ (v)  $(0.582)_{\rm H} = ()_{10}$ (vi)  $(574)_8 = ()_2$ (8)
  - b. Perform the following BCD addition: (i) 175 + 326(ii) 589 + 199 (8)
- a. Simplify the given Boolean expression using Boolean theorems and implement **Q.7** using basic gates.

(i) 
$$AB + \overline{AC} + A\overline{BC}(AB + C)$$
  
(ii)  $XY + XYZ + XY\overline{Z} + \overline{X}YZ$  (6)

AE54/AC54/AT54/DEC = 2011

AMIETE - ET/CS/IT (NEW SCHEME)



# Subject: LINEAR ICs & DIGITAL ED

**ROLL NO.** 

b. Reduce the following function using K map technique

(i) 
$$f(A, B, C, D) = \sum m(0,1,4,8,9,10)$$

StudentBounty.com (ii) Draw the gate level diagram to 4:1 MUX. Draw the truth table and the output expression.

- a. What is an encoder? Draw and explain the truth table of an octal to binary **Q.8** encoder. (8)
  - b. Explain clocked SR FlipFlop with the help of truth table and diagram. Convert the same into and clocked D FlipFlop and explain its working. (8)

#### Q.9 a. Write short notes on:-

(i)	hnson counter or Twisted ring counter.	(6)
(i)	hnson counter or Twisted ring counter.	(

- (ii) 3 bit synchronous binary counter. (6)
- b. (i) A counter has 14 stable states 0000 through 1101. If the input frequency is 50 KHz, what will be its output frequency. (2)

(ii) The propagation delay time  $t_{pd}$  for each flip flop is 50ns. Determine the maximum operating frequency for mod 32 ripple counter. (2)