ROLL NO. _____

Code: AC07 / AT07 Subject: COMPUTER ARCHITECTUR

AMIETE – CS/IT (OLD SCHEME)

Time: 3 Hours **DECEMBER 2011** Max. Marks: 100

NOTE: There are 9 Questions in all.

- **Please write your Roll No. at the space provided on each page immediately after receiving the Question Paper.**
- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2 ×10)**

a. The product of sums form for the Boolean function $F(A,B,C,D)=\sum(0,1,2,5,8,9,10)$ is

(A) $(A'+B')(C'+D')(B'+D)$ **(B)** $(A'+B)(C'+D')(B+D)$
(C) $(A+B')(C+D')(B'+D)$ **(D)** $(A'+B')(C'+D')(B+D)$

b. In which representation, –14 is represented as 11110001?

(A) Signed Magnitude
(B) signed 1's complement
(C) Signed 2's complement
(D) –14 cannot be represented as 11110001

c. Which of the following instruction is described by PC ← AR

(A) Load **(B)** Store
(C) Branch unconditional **(D)** Branch and save return address

d. What happens when the RET instruction is executed at the end of subroutine?

(A) the information where the stack is initialized is transferred to the stack pointer
(B) the memory address of the RET instruction is transferred to the program counter
(C) two data bytes stored in the top two locations of the stack are transferred to the program counter
(D) two data bytes stored in the top two locations of the stack are transferred to the stack pointer

e. What type of operation(s) is/are performed by a microprogram sequencer operation?

(A) read **(B)** write
(C) read and write **(D)** read and execute

f. Which is true for a typical RISC architecture?

(A) Instruction taking multiple clock cycles
(B) Have few registers
(C) Hardware control unit
(D) Micro programmed control unit

g. Which of the following address modes calculate the effective address as (address part of the instruction) + (content of CPU register)

(A) Direct Address Mode **(B)** Indirect Address mode.
(C) Relative address Mode. **(D)** Indexed address Mode.

h. What is a trap?

(A) External interrupt **(B)** Internal Interrupt.
(C) Software Interrupt **(D)** Error

i. A bus organized CPU has 16 registers with 32 bits in each, an ALU and a destination decoder. How many inputs and outputs are there in the decoder?

(A) 16 - to - 32 line decoder **(B)** 4 – to - 8 line decoder
(C) 8 - to - 16 line decoder **(D)** 4 – to -16 line decoder

j. Which of the following is used to handle branch instructions during pipeline conflicts?

(A) Prefetch target instruction **(B)** branch prediction
(C) delayed execution of instruction **(D)** both **(A)** and **(B)**

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Discuss the concept of stored program architecture. How it is different from Von Neumann architecture? Comment on the architecture of presently used processors. **(8)**

b. List the truth table of a three variable exclusive-OR function: $X=A \oplus B \oplus C$ **(3)**

c. Convert the BCD number 360 in to binary, octal and EX–3. **(5)**

Q.3 a. The following transfer statements specify a memory. Explain the memory operation in each case.
(i) R2← M[AR]
(ii) M[AR]←R3
(iii) R5← M[R5] **(6)**

b. List any 4 arithmetic micro operations and describe what functions are performed by them. **(4)**

c. With a diagram, explain how binary adder subtractor works. **(6)**

Q.4 a. Convert the following arithmetic expression from infix to reverse polish notation
(i) A*B+C*D+E*F
(ii) A*B+A*(B*D + C*E)
(iii) A+B*[C*D+E*(F+G)] **(6)**

b. Explain Interrupt cycle with a flowchart. **(10)**

Q.5 a. Explain the need of address sequencing. Describe with block diagram of a control memory and the associated hardware needed for selection of the next microinstruction. **(12)**

b. Perform the arithmetic operations given below with binary numbers and with negative numbers in signed 2's compliment representation. Use 7 bits to accommodate each number together with its sign. In each case determine if there is an overflow.
(i) (+35)+(+40) (ii) (–35)+(–40) **(4)**

Q.6 a. What are the various addressing modes? Explain with suitable examples. **(8)**

b. Design a 8 bit bus system to read data from any of the four 8 bit registers A, B, C and D. Use appropriate number of selection lines and draw the function table. Show the block diagram making use of multiplexers. **(8)**

Q.7 a. With neat flow chart, explain addition & subtraction of two signed binary numbers. **(8)**

b. Show the step by step multiplication process using Booth's algorithm when (+15) and (+13) are multiplied. The multiplicand is +15. **(8)**

Q.8 a. Explain the three types of mapping procedures used in the organization of cache memory. **(10)**

b. A computer uses RAM chips of 1024 × 1 capacity.
(i) How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes.
(ii) How many chips are needed to provide a memory capacity of 16K bytes? Show the connection diagram for the same. **(6)**

Q.9 a. How priority is decided in a multiple interrupt system? Give the hardware description of priority encoder. **(8)**

b. Discuss different modes of DMA data transfer. **(8)**