	DiplETE – ET (NEW	SCHEME) – Code: DE	(IB)	
Time	: 3 Hours	DG ELECTRONICS	56 Max. Marks: 100	
 Q¹ th Th of Or q¹ 	E: There are 9 Questions in all. uestion 1 is compulsory and carries a space provided for it in the answe ne answer sheet for the Q.1 will be f the commencement of the examina ut of the remaining EIGHT Que uestion carries 16 marks. ny required data not explicitly given	er book supplied and nowhere else collected by the invigilator after h tion. estions answer any FIVE Ques	e written in e. half an hour tions. Each	
Q.1	Choose the correct or the best alternative in the following: (2×10)			
	a. The most commonly used transistor circuit configuration is			
	(A) common base(C) common collector	(B) common emitter(D) none of these		
	b. The FET is characterised by			
	(A) voltage gain(C) power gain	(B) current gain.(D) none of these		
	c. When no signal is applied, the approximate collector efficiency of a class A power amplifier is			
	 (A) 10 % (C) 25 % 	 (B) 50 % (D) 0 %. 		
	d. The input impedance of an ideal	op-amp is		
	(A) finite(C) infinite	(B) zero(D) unity		
	e. The slew rate is expressed as			
	(A) 2 π f Vm / 10 ⁶ (C) Vm 10 ⁶ / 2 π f	(B) 2 π f 10 ⁶ / Vm (D) 2 π f / Vm 10 ⁶		
	(•)			
	f. The instrumentation amplifier h	aving an important feature of		

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g. In a multivibrator, we have	feedback	
(A) 100% positive	(B) both positive and negative	
(C) negative	(D) none of these	
h. In the diffused resistor method, the terms of surface dimensions L, W	feedback (B) both positive and negative (D) none of these e sheet resistance Rs can be expressed in and diffused resistor R as	0
(A) RL/W	(B) RW/L	
(C) W/RL	(D) RWL	
i. In the common mode configuratio	on, gain is	
(A) very high	(B) always infinite	
(C) always unity	(D) very low	
j. IC 723 General purpose regulator	has following limitations	
(A) no short circuit protection	(B) output voltage is fixed	

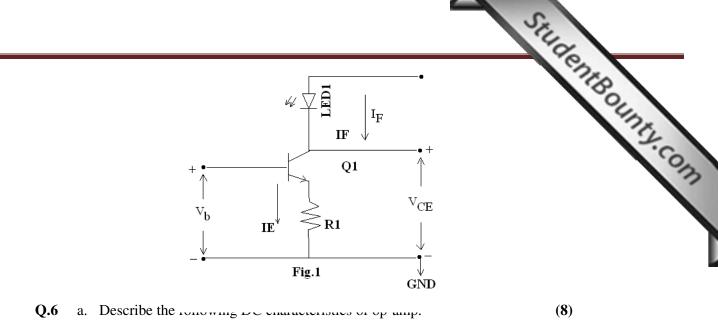
Answer any FIVE Questions out of EIGHT Questions. Each question carries 16 marks.

- Q.2 a. List the basic processes used in the silicon planar technology, and describe the oxidation process in detail. (8)
 b. Discuss the various ways for fabricating PNP transistor. (8)
 Q.3 a. Draw an h-parameter equivalent circuit for the CB unbypassed base bias configuration and briefly explain the component of the model. (8)
 b. A CE amplifier having the following h parameters h_{ie} = 1100Ω, h_{oe} = 25µS, h_{fe} = 50 and h_{re} = 2.5×10⁻⁴, if load and source resistances are 1 KΩ. Find
- Q.4 a. Draw the transfer characteristics of a FET and show that the gate source voltage increases with decrease in drain current. (8)
 - b. A JFET has a drain current of 5mA, I_{DSS} of 10 mA and gate source cut off Voltage $V_{GS(off)}$ = -6V, find the values of (i) V_{GS} and (ii) V_P (8)
- Q.5 a. Draw the circuit diagram of transformer-coupled class A amplifier and drive an expression for relation between reflected load and the secondary load. (8)
 - b. The LED in the circuit shown in Fig.1 is to pass a 20mA current. The circuit voltages are Vcc = 15V, $V_{BE} = 0.7V$, $V_F = 1.9 V$ and $V_B = 5V$. Determine a suitable resistance value for R_1 and calculate V_{CE} for Q_1 . (8)

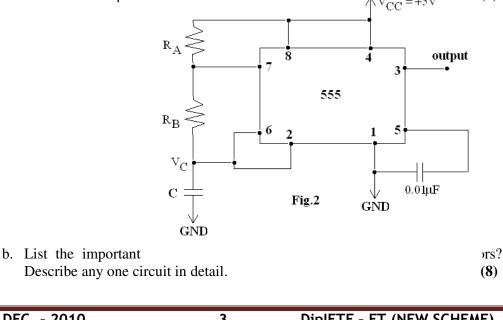
current and voltage gain.

(8)

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- (i) Input offset voltage
- (ii) Input offset current
- (iii) Input bias current
- (iv) Thermal drift
- b. Describe the operation of voltage follower using op-amp. Why it is also called as non-inverting buffer amplifier. (8)
- Q.7 a. Draw the circuit of op-amp integrator and drive an expression for the output voltage. (8)
 - b. A non inverting summing amplifier having three resistances at non inverting terminal are $R_1 = R_2 = R_3 = 1K\Omega$, the feedback resistance is of $2K\Omega$. The input sources connected at the non-inverting terminals are of $V_a = 3V$, $V_b = 4V$ and $V_c = -1V$, find the output voltage (V_o) . (8)
- **Q.8** a. Describe the operation of astable multivibrator using IC555 as shown in Fig. 2 and find the frequency of oscillation and duty cycle if $R_A = 6.8 \text{ K}\Omega$, $R_B = 3.3 \text{ K}\Omega$ and $C = 0.1 \mu \text{F}$. (8)



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- StudentBounts.com Q.9 a. Draw the connection diagram of three pin adjustable voltage regulator (D 317). Find the value of input set resistor R_1 and output set resistor R_2 . The output voltage Vo=5V, output current Io=1.0A, adjustment pin current $I_Q = 100 \mu A$ and the voltage between output and reference terminal is $V_R = 1.25$ V, $I_{R1} = 5mA$.
 - b. Draw the functional diagram of ADC and list out the names and applications of commonly used ADCs. (8)

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