Code: DE09 **Subject: DIGITAL ELECTRONICS**
Time: 3 Hours **Max. Marks: 100**

DECEMBER 2010

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after half an hour of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. The decimal equivalent of the fractional binary number 0.1011 is _____

(A) 0.6875 **(B)** 0.9375
(C) 0.625 **(D)** 0.0625

b. If the output of a 2 input gate is 1 if and only if its input are equal , it is true for _____

(A) AND Gate **(B)** XOR Gate
(C) OR Gate **(D)** XNOR Gate

c. The main advantage of ECL over TTL or CMOS is _____

(A) ECL is less expensive.
(B) ECL consume less power.
(C) ECL is available in a greater variety of circuit type.
(D) ECL is faster.

d. The input to a full adder are A = 1, B = 1 , $C_{in} = 0$, the outputs are _____

(A) SUM = 1, Count = 1. **(B)** SUM = 1, Count = 0.
(C) SUM = 0, Count =1. **(D)** SUM = 0, Count = 0.

e. A feature that distinguishes the JK flip-flop from the SR flip-flop is the _____

(A) Toggle condition. **(B)** Present input.
(C) Type of clock. **(D)** Clear input.

f. To serially shift a byte of data into a shift register, there must be _____

(A) One clock pulse. **(B)** One load pulse.
(C) Eight clock pulse. **(D)** One clock pulse for each 1 in the data.

g. A memory with 256 addresses has _____

(A) 256 address lines. **(B)** 6 address lines.
(C) 1 address line. **(D)** 8 address lines.

h. The accuracy of a D/A converter is a measure of _____

(A) The difference between the actual output and expected output voltage.
(B) Percentage of full scale or maximum output voltage.
(C) **(A)** and **(B)** both.
(D) neither **(A)** nor **(B)**.

i. The most popular A/D converter is the _____

(A) Successive Approximation Converter.
(B) Counting Type Converter.
(C) Parallel Comparator Converter.
(D) Dual Slope Converter.

j. The 2's complement of the number 11001000 is _____.

(A) 00110111 **(B)** 00110001
(C) 01001000 **(D)** 00111000

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Convert the binary number 101101 into gray number. **(6)**

b. Convert the BCD code 10000110 into decimal and hexadecimal number. **(4)**

c. Add the BCD number 0010 0011 and 0001 0111 and convert the result into hexadecimal number. **(6)**

Q.3 a. Using a Karnaugh map, convert the following standard SOP expression into a minimum SOP expression.

$$Y = \overline{A}\,\overline{B}\,\overline{C}\,D + \overline{A}\,\overline{B}\,C\,D + \overline{A}\,\overline{B}\,C\,\overline{D} + \overline{A}\,B\,\overline{C}\,\overline{D} + \overline{A}\,B\,\overline{C}\,D + A\,B\,\overline{C}\,D + A\,\overline{B}\,\overline{C}\,D + A\,\overline{B}\,C\,D + A\,\overline{B}\,C\,\overline{D}.$$

(8)

b. Simplify the expression AB+ A(B+C)+B(B+C). **(8)**

Q.4 a. Compare the following characteristics of DTL, TTL, ECL and CMOS logic families.
(i) Basic Gate (ii) Fanout (iii) Noise immunity (iv) Power dissipation
(v) Propagation delay. **(8)**

b. What is wired logic? Draw the wired AND connection of DTL gates a explain its importance. **(8)**

Q.5 a. Describe the basic operation of Multiplexer and explain its role in combinational logic circuit designs. **(8)**

b. Draw the logic symbol and associated truth table of 1 line to 4 line DEMUX and implement its logic circuit. **(8)**

Q.6 a. Design a logic circuit which can work as BCD to Decimal decoder. Explain the functioning of the circuit with the help of Truth Table. **(8)**

b. Realize the Full Adder circuit with the help of NAND-NAND gates. Draw neat logic circuit diagram for Sum and Carry separately. **(8)**

Q.7 a. Convert the operation of RS flip-flop into D Flip-Flop. **(4)**

b. What is Race-around problem? How can you rectify it? **(4)**

c. Design a decade counter using J-K Flip-Flops. **(8)**

Q.8 a. Explain the operation of Static MOS RAM cell with the help of suitable diagram. **(8)**

b. Differentiate the following type of memories
(i) RAM vs ROM
(ii) SRAM vs DRAM
(iii) EPROM vs EEPROM
(iv) CACHE vs MAIN MEMORY **(8)**

Q.9 a. Explain the circuit operation of Successive Approximation A/D converter. **(8)**

b. Draw the block Diagram of Analog to Digital converter using Voltage to Frequency conversion and explain its operation in brief. **(8)**