

**Subject: COMPUTER ORGANIZATION**

Time: 3 Hours

Max. Marks: 100

**DECEMBER 2010****NOTE: There are 9 Questions in all.**

- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after half an hour of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

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**Q.1 Choose the correct or the best alternative in the following: (2×10)**

a. The individual bits in a status register called

- (A) Word (B) byte  
(C) flags (D) bits

b. The binary code of instruction on a microcomputer is called

- (A) Op code (B) mnemonic  
(C) byte (D) operand

c. Name the sequence of binary codes stored in the control unit

- (A) A program (B) An instruction  
(C) An opcode (D) Micro program

d. The data bytes operated in the ALU are

- (A) operands (B) digits  
(C) opcodes (D) mnemonics

e. If  $(211)_x = (152)_8$  then the value of base x is

- (A) 6 (B) 5  
(C) 7 (D) 9

f. The logic expression for overflow in the addition of 2's complement integers is

- (A)  $C_{n-1}$  or  $C_n$  (B)  $C_{n-1}$  and  $C_n$   
(C)  $C_{n-1} \oplus C_n$  (D)  $C_n \oplus C_{n-1}$

g. 16 bytes are pulled from stack having top of stack address 00CD. What will be the new top of stack address?

- (A) 00BD (B) 00AD  
(C) 00DD (D) 10CD

- h. In 4 bit CLA, The addition process requires only
- (A) 4 gates (B) 3 gate delay  
(C) 1 XOR gate delay (D) 2 gate delay
- i. Registers R1 & R2 of a computer contain the decimal values 1200 & 4600.  
Find the effective address of the memory operand for subtract (R1) -, R5
- (A) 5830 (B) 4599  
(C) 4699 (D) 1200
- j. RWM is
- (A) volatile memory (B) non volatile memory  
(C) programmable (D) non programmable

**Answer any FIVE Questions out of EIGHT Questions.  
Each question carries 16 marks.**

- Q.2** a. Explain different functional units of a digital computer. (4)
- b. What is a bus? Explain single bus structure in an architecture. (4)
- c. List the steps needed to execute the following instructions:  
Add Loc A, R0  
Add R1, R2, R3 (8)
- Q.3** a. What is an addressing mode? Explain any 3 addressing mode with example. (2+2×3)
- b. Represent the decimal values -5, -14, -10, -19, 51 and -43 as signed 7 bit numbers in (i) 2's complement format (ii) signed magnitude format. (4+4)
- Q.4** a. Consider the following possibilities for saving the return address of a subroutine (i) in a processor register (ii) in a memory location associated with the call so that a different location is used when the SR is called from different places. Which of these supports subroutine nesting and which supports subroutine recursion? (4+4)
- b. Explain interrupt hardware for multiple interrupts with a single INTR line. (8)
- Q.5** a. Devices A, B, C are connected to the bus of a computer. I/O transfer for 3 devices use interrupt control.
- (i) Interrupt nesting for devices A & B is not allowed, bus interrupt request from C may be accepted. While A or B is being serviced.  
Suggest different ways in which this can be accomplished if (i) The computer has one IRQ line (ii) 2 IRQ lines INTR1 & INTR2 with INTR1 having higher priority than INTR2. (4+4)

- b. Explain bus arbitration using daisy chain (8)
- Q.6** a. Explain with a diagram, the operation of a static CMOS RAM cell for read and write operations. (8)
- b. In an SDRAM,  $\overline{\text{RAS}}$  line is asserted and the test word of data is transferred five clock cycles later. Assume 32 bits of data are transferred in parallel & 133 MHz clock is used & the burst length is 8. Calculate the time it takes to transfer  
 (i) 32 bytes of data (ii) 64 bytes of data  
 Calculate the latency in each case. (4+4)
- Q.7** a. Show that the logic expression  $C_n \oplus C_{n-1}$  is a correct indicator of overflow in the addition of 2's complement integers by using a truth table. (8)
- b. A half adder is a combinational logic circuit having x & y inputs and two outputs s & c (sum & carry) (i) design a half adder as a 2 level AND OR circuit (ii) Implement a full adder using 2 half adders. (4)
- c. Compare the longest logic delay path through the network (4)
- Q.8** a. Multiply each pairs of signed 2's complement numbers using Booth Algorithm  
 $A = 001111$                        $B = 001111$   
 (Multiplicand)                      (multiplier) (8)
- b. Give the basic features of IEEE FLOATING point number standard. (8)
- Q.9** a. Explain the control sequences for the execution of the instruction Add(R3), R1 (8)
- b. Explain the control unit organisation of a hardwired control. (8)