Subject: VLSI DESIGN

Time: 3 Hours **DECEMBER 2010** **Max. Marks: 100**

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after half an hour of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. MOS transistor with implant channel is called as_____.

(A) bipolar **(B)** enhancement
(C) BiCMOS **(D)** depletion

b. Substrate in nMOS is _____.

(A) N type **(B)** P type
(C) polysilicon **(D)** metal

c. Switching speed of MOS transistor is inversely proportional to _____of the channel.

(A) square of length **(B)** length
(C) square root of length **(D)** three times of length

d. Zpd/Zpu for an nMOS inverter driven by another nMOS inverter is _____.

(A) 1/6 **(B)** 1/16
(C) 1/8 **(D)** 1/4

e. latch up in CMOS circuit exists in _____.

(A) P-well only **(B)** n-well only
(C) P-well and n-well **(D)** twin tup

f. Feature size of MOS transistor is _____.

(A) $2\lambda \times 2\lambda$ **(B)** $\lambda \times \lambda$
(C) $4\lambda \times 4\lambda$ **(D)** $\frac{\lambda}{2} \times \frac{\lambda}{2}$

g. Standard unit capacitance value C_g for $5\mu m$ MOS transistor is _____.

(A) 0.0005 pF **(B)** 0.04 pF
(C) 0.01 pF **(D)** 0.02 pF

h. Overall delay *fd* for nMOS cascaded inverter driven by large capacitive load is _____.

(A) $3.5\ eN\tau$ **(B)** $4.5\ eN\tau$
(C) $1.5\ eN\tau$ **(D)** $2.5\ eN\tau$

i. Gate Area Ag is scaled by _____.

(A) $1/\alpha$ **(B)** $1/\beta$
(C) $1/\alpha^2$ **(D)** $1/\beta^2$

j. In constant field scaling model _____.

(A) $\alpha = \frac{1}{\beta}$ **(B)** $\beta = 1$
(C) $\beta = \alpha$ **(D)** $\alpha = 1$

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. With neat diagram explain the working of enhancement mode nMOS transistor. **(8)**

b. Design the inverter using CMOS logic. Explain its characteristics also. **(8)**

Q.3 a. Derive an expression for I_{ds} in non saturated and saturated region. **(10)**

b. What is body effect? Explain briefly how threshold voltage Vt will be affected by body effect. **(6)**

Q.4 a. Obtain pull up to pull down ratio for a nMOS inverter driven through one or more pass transistor. **(10)**

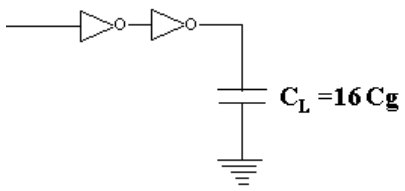
b. Explain the working of MOSFET. **(6)**

Q.5 a. Write λ based design rules for wires and transistor. **(8)**

b. Define sheet resistance and standard capacitance for a feature size transistor. **(8)**

Q.6 a. Derive an expression for total delay for N-cascaded inverters driving a large capacitive load. **(8)**

b. Two nMOS inverters are cascaded to drive a capacitive load $C_L = 16C_g$ a
shown in Fig.1. Calculate pair delay in terms of τ. **(8)**



Inverter 1	Inverter 2
$Lpu_1 = 16\ \lambda$	$Lpu_2 = 2\lambda$
$Wpu_1 = 2\ \lambda$	$Wpu_2 = 2\ \lambda$
$Lpd_1 = 2\ \lambda$	$Lpd_2 = 2\ \lambda$
$Wpd_1 = 2\ \lambda$	$Wpd_2 = 8\ \lambda$

Fig. 1

Q.7 a. Obtain scaling factor for the following:
(i) Parasitic capacitance (ii) Channel resistance (iii) Gate delay
(iv) Saturation current **(8)**

b. Design a two-line to four-line decoder circuit to the mask layout level and determine its boundary box. **(8)**

Q.8 a. Design two input NOR gate using CMOS. **(6)**

b. Write an example of an inverter showing that the power dissipation decreases at the expense of area. **(10)**

Q.9 a. Write a note on design styles in VLSI. **(6)**

b. Obtain test-vector for the Fig.2, using sensitised path based testing. **(10)**

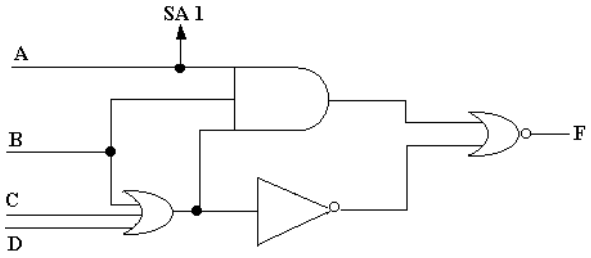


Fig.2