Subject: EMBEDDED SYSTEMS DESIGN

Time: 3 Hours **Max. Marks: 100**

DECEMBER 2010

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after half an hour of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. Which of the following is incorrect common design metrics?

(A) Size, Performance, flexibility **(B)** Maintainability, correctness, safety
(C) NRE cost, unit cost, power **(D)** Rigid, linearity, sturdy

b. A sequential circuit is a digital circuit whose outputs are a function of

(A) Present as well as previous input values
(B) Present values
(C) Previous values
(D) None of the above choices

c. Emulator supports

(A) Debugging the program while it executes on development processor
(B) Debugging the program while it executes on target processor
(C) Programmers to evaluate and correct their programs
(D) Programmers to convert HLL to MLL

d. Baud rate is defined as

(A) Number of signals changes per second
(B) Number of bits per second
(C) Number of signals changes per minute
(D) Number of bits per minute

e. Storage permanence is defined as

(A) Storage capacity
(B) Ability of memory to hold its stored data
(C) Size of the memory
(D) None of the above

f. PCI bus is used for

(A) Interconnecting chips
(B) Connecting expansion boards

(C) Connecting processor memory subsystems
(D) All the above

g. Which one of the following is not a semaphore variant?

(A) Counting semaphore **(B)** Resource semaphore
(C) Mutex semaphore **(D)** Dormant semaphore

h. Events are one-bit flags

(A) With which tasks signal one another
(B) With which tasks are executed
(C) With which tasks are terminated
(D) None of the above

i. A hard real-time system is one

(A) Where both logical and timely correctness is important
(B) Where logical correctness is important
(C) Where timely correctness is important
(D) None of the above

j. The phases of instruction execution are

(A) F,D,E,W **(B)** F,E,W,D
(C) W,F,D,E **(D)** E,F,D,W
Where F = fetch, D = decode, E = execute, W = write

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain design metrics used for embedded systems. **(10)**

b. Briefly explain the following:

(i) combinational & sequential circuit
(ii) single purpose processor and general purpose processor **(6)**

Q.3 a. With example explain how program & data memory fetches can be overlapped in a Harvard architecture. **(6)**

b. Explain the following:-
(i) Device programmers (ii) Linker
(iii) Cross compiler (iv) System call
(v) Emulators **(10)**

Q.4 a. Given a timer with a terminal count and a clock frequency of 10MHz. Calculate the following:-
(i) its Range & Resolution
(ii) the Terminal count values needed to measure 3ms intervals
(iii) If a prescalar is added, what is the minimum division needed to measure an interval of 100ms

(iv) Instead of a prescalar a second 16-bit up counter is cascaded, what ... range and resolution of this design. (...

b. With example, explain watch-dog timers and reaction timer. **(8)**

Q.5 a. What is cache mapping? Explain the direct mapping, fully associative mapping and set associative mapping techniques. **(8)**

b. Given the following three cache designs, find the one with the best performance by calculating the average cost of access. Show all calculations

(i) 4Kbyte, 8-way set associative cache with a 6% miss rate; cache hit costs one cycle, cache miss costs 12 cycles.
(ii) 8Kbyte, 4-way set associative cache with a 4% miss rate; cache hit costs two cycles, cache miss costs 12 cycles.
(iii) 16Kbyte, 2-way set associative cache with a 2% miss rate; cache hit costs three cycles, cache miss costs 12 cycles. **(8)**

Q.6 a. Explain in brief serial, parallel and wireless communication mediums. Write two common applications for each. **(9)**

b. Explain how to extend the number of ports on a 4-port 8051 to 8 by using extended parallel I/O. Using block diagram for 8051 and the extended parallel I/O device, draw and label all interconnections and I/O ports. Clearly indicate the names and width of all connections. **(7)**

Q.7 a. Explain the following:-

(i) How does the scheduler know when a task has become blocked or unblocked?
(ii) What happens if all the tasks are blocked?
(iii) What if two tasks with the same priority are ready?
(iv) If one task is running and another higher priority tasks unblocks, does the tasks that is running, get stopped and moved to the ready state right away. **(8)**

b. What is semaphore? Discuss the advantages of multiple semaphore. Also give the semaphore problems. **(8)**

Q.8 a. Explain with C program how to pass date from one task to another task by putting the data into a buffer and then writing a pointer to the buffer onto the queue. **(10)**

b. Explain standard features of events. **(6)**

Q.9 a. Explain with example and C program, to write short interrupt routines. **(10)**

b. Explain some few techniques to save memory space. **(6)**