Subject: LINEAR ICs & DIGITAL ELECTRONICS

Time: 3 Hours **Max. Marks: 100**

DECEMBER 2010

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions, selecting at least TWO questions from each part, each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. An op amp is ideal in all respects except that it has finite gain of 10^4. If this op amp is used as a voltage follower, the gain of the voltage follower is equal to _____.

(A) 0.99 **(B)** 0.999
(C) 0.9999 **(D)** 1.0

b. An op amp has a CMRR of 86dB. If its differential gain is 109dB, the common mode gain is equal to _____.

(A) 7.07 **(B)** 10
(C) 14.14 **(D)** 20

c. The input to a voltage follower using an op amp is a sine wave of 20 V peak to peak amplitude and 2 kHz frequency. The minimum slew rate required for the op amp, so that the output is not distorted is _____.

(A) 0.125V/μs **(B)** 1.25V/μs
(C) 0.125V/ms **(D)** 1.25 V/ms

d. The output Vo in the circuit of Fig.1 is equal to_____.

(A) +3 V **(B)** -3 V
(C) +19 V **(D)** -19 V

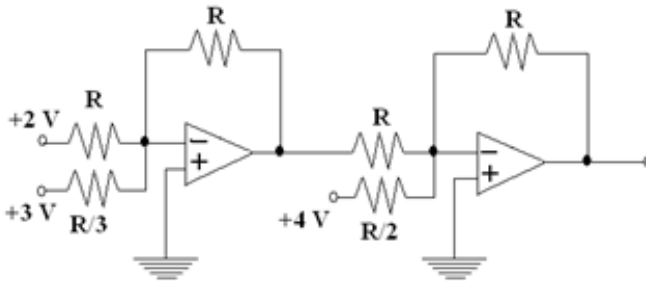

Fig.1

e. In the Schmitt trigger circuit of Fig.2 'hysteresis' is equal to_____.

(A) 2 V
(B) 5 V
(C) 7 V
(D) 3 V

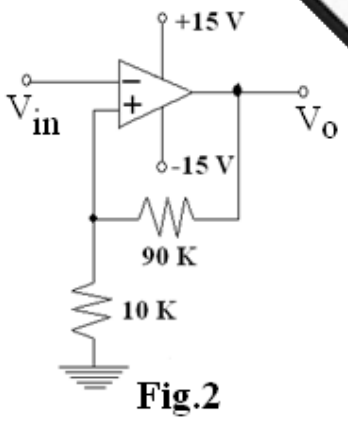

Fig.2

f. The decimal equivalent of the hexadecimal number FACE is equal to_____.

(A) 61440
(B) 64206
(C) 64440
(D) 66206

g. The output of a 2-input EXCLUSIVE-NOR gate is ONE, when both the inputs are _____.

(A) one
(B) zero
(C) equal
(D) different

h. The minimum number of NAND gates required to realize an EXCLUSIVE-OR function (using only NAND gates) is_____.

(A) 3
(B) 4
(C) 5
(D) 6

i. The minimum number of JK flip-flops required to build a synchronous decade counter is _____.

(A) 3
(B) 4
(C) 5
(D) 6

j. The main advantage of successive approximation type A/D converter is_____.

(A) Low Cost
(B) High Conversion Time
(C) Constant Conversion Time
(D) Low Conversion Time

PART (A)
Answer At least TWO questions. Each question carries 16 marks.

Q.2 a. Classify IC's on the basis of application, device used & chip complexity. **(4)**

b. An op amp has an input impedance of 1MΩ, output impedance of 1KΩ a gain of 10^4. When this op amp is used as an inverting amplifier as shown Fig.3, determine the voltage gain and the output impedance of the amplifier. **(8)**

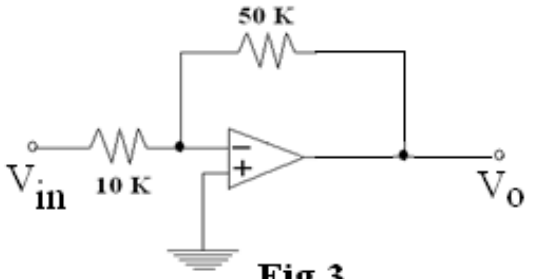

Fig.3

c. Design an inverting amplifier having a gain of 34 dB and input impedance of 10 KΩ, using an ideal operational amplifier. **(4)**

Q.3 a. In the difference amplifier of circuit of Fig.4, obtain the condition required, so that the common mode gain is equal to zero. **(8)**

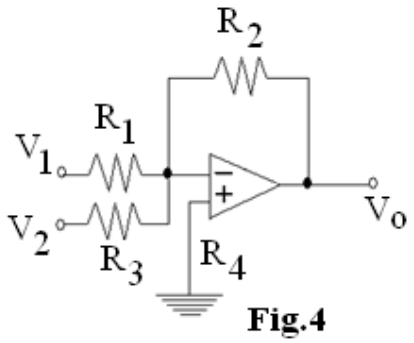

Fig.4

b. Draw the circuit of an instrumentation amplifier using three ideal op amps and design the values of the different resistors so that the differential gain is 40dB and common mode gain is equal to zero. **(8)**

Q.4 a. Draw the circuit of a differentiator using an ideal op amp, and prove that it works as a differentiator. **(5)**

b. What modifications are required to make the circuit in 4(a) a practical differentiator circuit. **(3)**

c. Design a Schmitt trigger using an ideal op amp operating with +12V and -12V, to have UTP (upper trigger point) and LTP (lower trigger point) as +4V and +1V respectively. Also draw the output waveform if the input is a triangular waveform varying from –6V and +6V. **(8)**

Q.5 a. Draw the block diagram of a voltage comparator type A/D converter, and explain it's functioning. What is its main advantage? **(8)**

b. Draw the circuit of an Astable Multivibrator using 555 timer IC, and design the values for the different components in the circuit so that the output is HIGH for100 μs and LOW for 300 μs during each cycle. **(8)**

PART (B)
Answer At least TWO questions. Each question carries 16 marks.

Q.6 Perform the following conversions:

(i) $(456.75)_{10} = (\ )_2$ (ii) $(101101.101)_2 = (\ )_{10}$
(iii) $(352.25)_{10} = (\ )_8$ (iv) $(327.46)_8 = (\ )_{10}$
(v) $(2040.125)_{10} = (\ )_{16}$ (vi) $(567.75)_8 = (\ )_{16}$
(vii) $(DEFA.CE)_{16} = (\ )_8$ (viii) $(765.575)_8 = (\ )_2$ **(2×8)**

Q.7 a. State and prove De Morgan's theorems. **(5)**

b. Draw the logic circuit to implement the AND function using only NOR gates. **(5)**

c. Obtain the logic expression for the output X of the circuit in Fig.5, and simplify using De Morgan's theorems. **(6)**

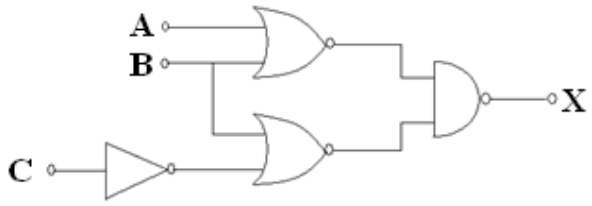

Fig.5

Q.8 a. Implement the half-adder by using 4:1 MUX and realize it using only NAND gates. **(6)**

b. Draw the truth table for 'SUM and 'CARRY OUT' of a FULL ADDER. From the truth table, obtain logic expressions for them. From these expressions, realize the FULL ADDER using logic gates. **(10)**

Q.9 a. Draw the circuit of a latch using two NAND gates and explain its operation. **(4)**

b. Draw the internal circuit of an edge triggered JK flip-flop and explain its functioning using necessary waveforms. **(6)**

c. Draw the circuit of a MOD-50 ripple counter to reduce 50 Hz to 1Hz, using JK flip-flops and explain its operation with its state transition diagram. **(6)**