

Subject: ELECTRONIC DEVICES AND CIRCUITS

Time: 3 Hours

Max. Marks: 100

DECEMBER 2010

NOTE: There are 9 Questions in all.

- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after half an hour of the commencement of the examination.
- Out of the remaining EIGHT Questions, answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. The dual of given network in Fig.1 is

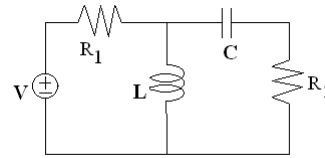


Fig.1

- (A) (B)
- (C) (D)

b. The value of load resistance R_L for maximum power transfer in the given circuit (Fig.2) is

- (A) 3Ω (B) 1Ω
 (C) 0Ω (D) cannot be determined

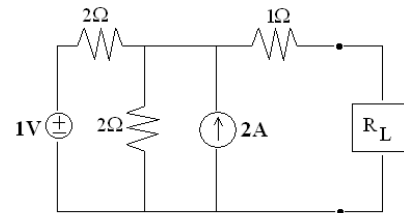


Fig.2

c. The V-I characteristic curve of circuit shown in Fig.3 is

- (A) (B) (C) (D)

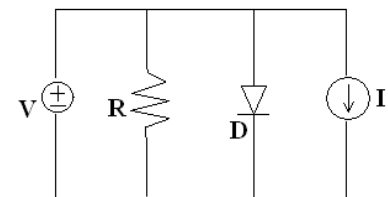


Fig.3

d. If V_m is the peak AC voltage of one-half of transformer secondary then P_{AV} of full wave rectifier with centre-tapped transformer is

- (A) $\frac{V_m}{2}$ (B) V_m
 (C) $2V_m$ (D) 1.11

e. The amplification factor (μ) of JFET is equal to

- (A) $\frac{g_m}{r_d}$ (B) $g_m r_d$
 (C) $\sqrt{g_m r_d}$ (D) $\sqrt{\frac{r_d}{g_m}}$

f. The maximum efficiency of class B push pull power amplifier is

- (A) $\frac{\pi}{2}$ (B) $\frac{\pi}{\sqrt{2}}$
 (C) $\frac{\pi}{2\sqrt{2}}$ (D) $\frac{\pi}{4}$

g. In negative feedback amplifier, identify false statements

- (A) BW increases (B) gain increases
 (C) noise reduces (D) stability improves

h. In multistage amplifier,

- (A) Gain increases and BW increases
 (B) Gain decreases and BW increases
 (C) Gain decreases and BW decreases
 (D) Gain increases and BW decreases

i. Emitter follower has

- (A) high input impedance and high output impedance
 (B) high input impedance and low output impedance
 (C) low input impedance and high output impedance
 (D) low input impedance and low output impedance

j. In Wein bridge oscillator, frequency of oscillation is

- (A) $2\pi RC$ (B) $\frac{1}{2\pi RC}$
 (C) $\frac{1}{2\pi RC\sqrt{6}}$ (D) $\frac{1}{2\pi\sqrt{LC}}$

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. State and explain the Thevenin's Theorem. Also explain how we get Norton's equivalent from Thevenin's equivalent of a circuit. (4)

b. Determine the V and I in the given Circuit (Fig.4) (4)

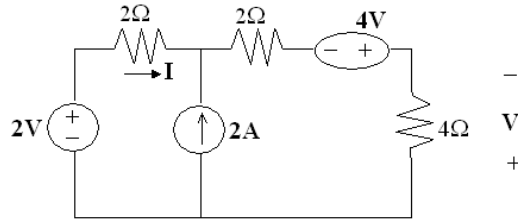


Fig.4

c. State Miller's (8)

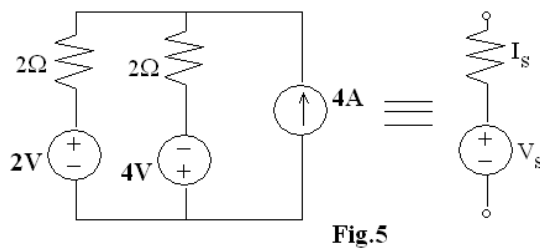


Fig.5

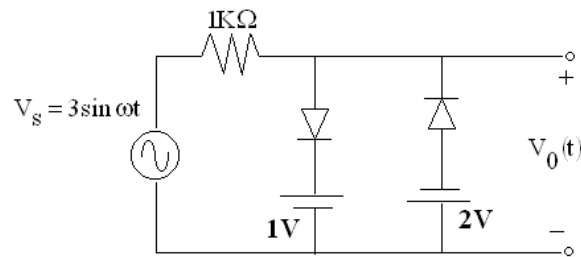


Fig.6

Q.3 a. Sketch $v_0(t)$ as shown in Fig.6 a

b. Using ideal diode, design a clamper circuit to perform the function indicated in the Fig.7. (6)

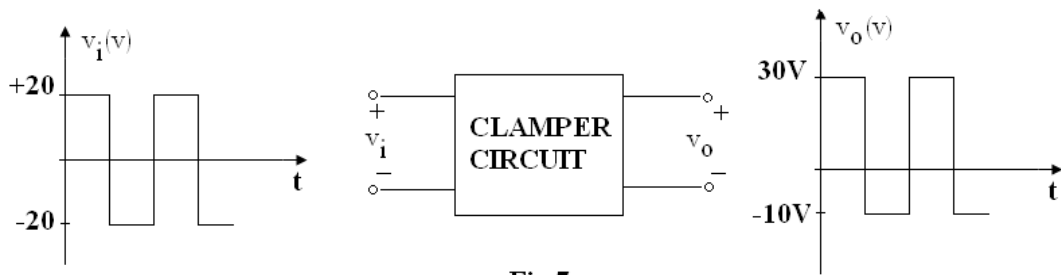


Fig.7

(i) $R_L = 100K\Omega$

(ii) $R_L = 10K\Omega$

(iii) $R_L = 1K\Omega$

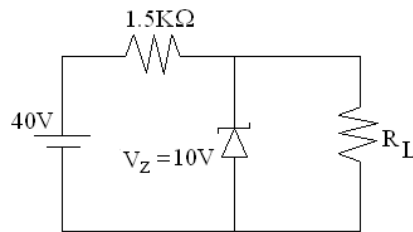


Fig.8

Q.4 a. (i) Draw AC equivalent circuit diagram.

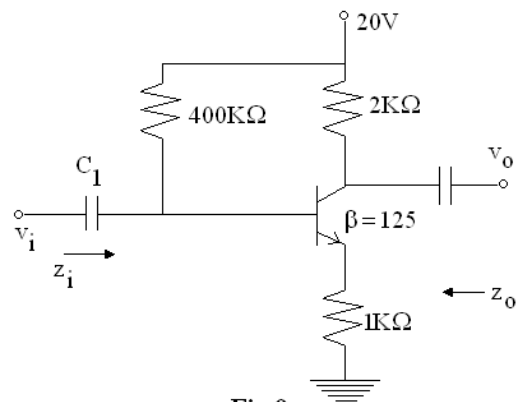


Fig.9

(ii) Calculate A_V, A_I, Z_i and Z_0 .

b. Explain the need of biasing in Transistor circuit and describe self biasing technique. (8)

Q.5 a. What is Power Amplifier? Compare Class A, Class B, Class AB and Class C Power Amplifiers. (8)

b. For the Amplifier circuit shown in Fig.10.
 $V_{CC} = 15V, \beta = 40, I_{CQ} = 5mA, V_{CEQ} = 7.5V$

(i) Estimate the value of R_L

(ii) Specify I_{BQ}

(iii) For a swing in i_C from 0mA to 10mA.

Find AC power output and efficiency.

What is the corresponding swing in i_B .

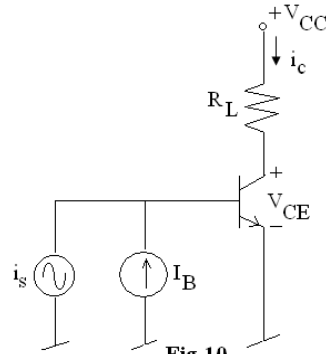


Fig.10

(8)

Q.6 a. Explain Barkhausen criterion for sustained oscillation. In the given block diagram (Fig.11), determine the value of C for system to be oscillatory. (8)

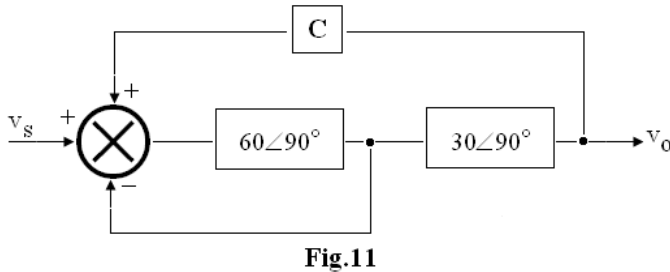


Fig.11

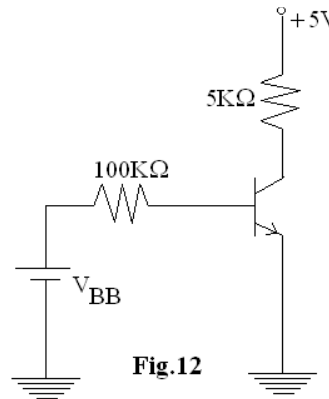


Fig.12

b. Explain Wein's bridge oscillator. Deduce the condition for sustained oscillation. (8)

Q.7 a. Explain the frequency response curve of single stage RC coupled amplifier. Compare it with two stage RC coupled amplifier. (5)

b. Write short note on Darlington Amplifier. Also discuss its merits and demerits. (5)

c. Explain multistage amplifier and its different cascade connections. (6)

Q.8 a. The JFET to be operated at an operating point defined by
 $I_D = 3mA, V_{DS} = 12V, V_{GS} = -3V, V_{DD} = 36V$
 Design an approximate biasing circuit. Assume $V_{GG} = 12V, R_G = 12M\Omega$. (8)

b. For the Transistor in Fig.12 find the range of V_{BB} for Transistor to be in
 (i) Cut-off Region. (ii) Active Region. (8)
 Given $\beta = 100, V_{BE}(Cut-in) = 0.5V, V_{BE}(Sat) = 0.8V, V_{CE}(Sat) = 0.2V$.

Q.9 a. What is buried layer? What purpose does it serve? What is the type of doping of the buried layer of npn transistor IC? (8)

b. Write short note on Integrated Resistors and Integrated Capacitors. (8)