AMIETE – ET (OLD SCHEME)

Code: AE27 **Subject: DIGITAL HARDWARE DESIGN**
Time: 3 Hours **Max. Marks: 100**

DECEMBER 2010

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after half an hour of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2x10)

a. An AND gate has 7 inputs. How many input rows are there in its truth table?

(A) 64 **(B)** 32
(C) 16 **(D)** 128

b. In a modern digital computer, a subtractor is normally not used because

(A) subtractor are very expensive
(B) the design of a subtractor is very complex
(C) the adder is geared for doing subtraction also
(D) most of the programs do not require subtraction

c. Flip Flop outputs are always

(A) complement of each other **(B)** independent of each other
(C) the same **(D)** same as inputs

d. In PLA

(A) Only AND arrays are programmable
(B) Both AND arrays and OR arrays are programmable
(C) Only OR arrays are programmable
(D) AND arrays are programmable and OR arrays are fixed

e. Rise and Fall delay values could be passed into entity using

(A) generics **(B)** functions
(C) procedures **(D)** drivers

f. The dynamic race hazard problem occurs in

(A) Combinational circuits only
(B) Both combinational and sequential circuits
(C) None of combinational and sequential circuits
(D) None of the above

g. A combinational logic circuit that is used when it is desired to send data from two or more source through a single transmission line known as

(A) decoder **(B)** encoder
(C) multiplexer **(D)** demultiplexer

h. The m-bit parallel adder consists of

(A) (m+1) full adders **(B)** m/2 full adders
(C) (m-1) full adders **(D)** m full adders

i. A demultiplexer is also known as

(A) data selector **(B)** data distributor
(C) multiplexer **(D)** encoder

j. 2 KB of memory means, its capacity is

(A) 2000 × 8 bits **(B)** 2000 × 10 bits
(C) 2048 × 8 bits **(D)** 2024 × 8 bits

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Write a note on CAD tools. **(7)**

b. State De Morgan's law and prove it using truth table **(3)**

c. Prove the Boolean identity **(3)**
$XY'Z + XYZ + X'Y'Z = XZ + Y'Z$

d. Construct the truth table for Boolean expression given below. **(3)**
$y = x_1 x_2 + x_2 x_3$

Q.3 a. Realize the logic function $A' + B' + C$ using NAND gates only. **(4)**

b. Simplify the expression $Y = \left((AB)' + A' + AB\right)'$ **(4)**

c. Simplify the Boolean expression using K maps. **(4)**
$Y = \prod M\ (0,1,3,5,6,7,10,14,15)$

d. Construct full adder with two half adders and OR gate. **(4)**

Q.4 a. Draw the circuit of UP/DOWN counter. **(4)**

b. Explain briefly different types of registers. **(4)**

c. Implement the following function with a 8x1 multiplexer.
Y (A, B, C, D) = ∑ (0, 1, 2, 5, 9, 11, 13, 15)

d. Distinguish between combinational and sequential circuits. **(4)**

Q.5 a. Compare Moore and Mealy machines. **(6)**

b. Write a VHDL code for FSM that can detect 1011 sequence. **(5)**

c. write note on assert and report statement in VHDL. **(5)**

Q.6 a. Write a short note on FPGA. **(4)**

b. Differentiate between: **(4)**
(i) Next statement and exit statement
(ii) Wait statement and process statement

c. Write a VHDL code for T Flip Flop using behavioral approach. **(4)**

d. Write VHDL code for binary to gray code converter using data flow style of modeling. **(4)**

Q.7 a. Construct a Moore machine which is equivalent to the Mealy machine given in table. **(6)**

Mealy Machine

	Next State			
Present State	input a = 0		input a = 1	
	state	output	state	Output
→ q1	q3	0	q2	0
q2	q1	1	q4	0
q3	q2	1	q1	1
q4	q4	1	q3	0

b. Write VHDL code for BCD to seven segment decoder. **(5)**

c. Write a short note on functions and procedures in VHDL. **(5)**

Q.8 a. Write short notes on the following: **(4×4=16)**
(i) PAL
(ii) Structural Style of modeling
(iii) Race Around Condition
(iv) VHDL classes and objects

Q.9 a. Write a note on ASM charts and ASM blocks **(8)**

b. Define micro instruction format. **(8)**