AMIETE - ET (OLD SCHEME)

Code: AE21 **Time: 3 Hours** Subject: DIGITAL COMMUNICAT

Max. Marks:

DECEMBER 2010

NOTE: There are 9 Questions in all.

- StudentBounty.com • Ouestion 1 is compulsory and carries 20 marks. Answer to 0.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the O.1 will be collected by the invigilator after half an hour of the commencement of the examination.
- Out of the remaining EIGHT Questions, answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

Q.1 Choose the correct or the best alternative in the following: (2×10)

- a. Signal to Quantization noise ratio in n-bit PCM system depend on
 - (A) Sampling frequency employed
 - (B) Independent of the value of n
 - (C) Increases with increasing value of n
 - (D) Decreases with increasing value of n
- b. Which system has maximum probability of error

| (A) PSK | (B) ASK |
|---------|----------------|
| (C) FSK | (D) BPSK |

c. When number of quantization level is 64 in PCM, the number of pulses in a code group will be

| (A) | 2 | (B) | 4 |
|-----|---|-------------|----|
| (C) | 6 | (D) | 16 |

d. If S/N ratio of signal is 15 and bandwidth is 5 kHz, the channel capacity is

| (A) 10 Kbits/s | (B) 20 Kbits/s |
|----------------|-----------------------|
| (C) 30 Kbits/s | (D) 40 Kbits/s |

e. Cyclic codes are subclass of

| (A) | Convolution codes | (B) Linear Block codes |
|-----|-------------------|---------------------------------|
| (C) | BCH codes | (D) Reed Solomon Codes |

f. The no of 1s in the length of PN sequence for a 4 stage shift register is

| (A) 5 | (B) 6 |
|----------------|--------------|
| (C) 7 | (D) 8 |

g. Slope overload in delta modulation can be avoided using

| (A) $\Delta/T_s \ge M'(t)$ | $(\mathbf{B}) \ \Delta/\mathrm{T}_{\mathrm{s}} \leq \mathrm{M}'(\mathrm{t})$ |
|----------------------------|--|
| (C) $\Delta/T_s = M'(t)$ | (D) None |

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h. The probability of error in ASK system

| (A) $\frac{1}{2} \operatorname{erfc}[\mathrm{E}_{\mathrm{s}}/4\eta]^{1/2}$ | (B) $\frac{1}{2} \operatorname{erfc}[\mathrm{E}_{\mathrm{s}}/\eta]^{1/2}$ |
|---|--|
| (C) $\frac{1}{2} \operatorname{erfc}[0.6 \mathrm{E}_{\mathrm{s}}/\eta]^{1/2}$ | (D) $\frac{1}{2} \operatorname{erfc}[E_s/2\eta]^{1/2}$ |

StudentBounty.com i. A DS spread spectrum has a 2.4576 Mcps code clock rate and 19.2 Kbps information rate. What is processing gain:

| (A) 64 | (B) 128 |
|------------------|----------------|
| (C) 256 | (D) 512 |

j. The rate efficiency of (6,3) block code in % is

| (A) 25 | (B) 50 |
|-----------------|----------------|
| (C) 75 | (D) 100 |

Answer any FIVE Questions out of EIGHT Questions. Each question carries 16 marks.

| Q.2 | a. | Explain how ISI can be reduced by pulse . Compare the performance degradation of communication filter due to noise interference and ISI. | (8) |
|-----|----|--|-----|
| | b. | Compare FH – SS with DS – SS technique. | (8) |
| Q.3 | a. | | (8) |
| | b. | Represent the data bits 101001 by the bipolar NRZ waveform. Sketch the following digital modulation scheme for these waveform (i) ASK (ii) FSK (iii) PSK | (8) |
| Q.4 | a. | A Systematic block code (6, 3) has a generator matrix as follows: $G = \begin{bmatrix} 100:110\\010:011\\001:111 \end{bmatrix}$ Find all its code vectors of this code. | (8) |
| | b. | Explain convolution codes. Design an encoder for convolution code using 3 shift register and taking 4 bit length of input data stream. | (8) |
| Q.5 | a. | $H = \begin{bmatrix} 101100\\ 110010\\ 011001 \end{bmatrix}$ (i) Determine the generator matrix (ii) Find the code word that begin 101 | (8) |
| | | | (0) |

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b. Draw the state diagram, and Trell's diagram for K = 3, code rate =

generated by $g_1(X) = X^2 + X$ $g_2(X) = X + 1$ $g_3(X) = X^2 + X + 1$

- StudentBounty.com a. Explain spread spectrum modulation. What is Pseudorandom Noise 0.6 sequence? Write at least 6 properties for PN sequences. (8)
 - b. A Pseudorandom Noise sequence is generated using a four stage linear feedback shift register. A modulo 2 adder is used between output of fourth and third shift register. A feedback path is from adder to input of first shift register. The chip rate is 10^7 chips per second, calculate:

(8)

- **0.7** a. Show that the impulse response of a matched filter h(t) matched to a signal s(t) is h(t) = Ks(T-t). Where T is the symbol duration and k is the proportionately constant. (8)
 - b. Determine the probability of error P_e in frequency shift keying (FSK) (8)
- **Q.8** a. Draw the block diagram of delta modulation system and explain its working. (8)
 - b. A decimal number N was transmitted using seven bit even parity Hamming code. After transmission, it was received as 1101101. Is there any error introduced during transmission? What is the value of N? (8)
- Q.9 a. Derive an expression for output signal to quantization noise ratio in a commercial PCM system. (8)
 - b. A certain 8 bit uniform quantization PCM system can accommodate a signal ranging from -1V to +1V. The RMS value of the signal is 0.5 V. Calculate the signal to quantization noise ratio and express it in dB. (8)

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