Code: AE05 **DECEMBER 2010** **Subject: BASIC ELECTR**
Time: 3 Hours **Max. Marks:**

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after half an hour of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. Hall effect can be used_____.

(A) to find type of semiconductor (whether P-type or N-Type)
(B) to find carrier concentration
(C) to measure conductivity
(D) all of the above

b. In an RC coupled amplifier, the gain decreases in the frequency response due to the _____.

(A) coupling capacitor at low frequency and bypass capacitor at high frequency
(B) coupling capacitor at high frequency and bypass capacitor at low frequency
(C) coupling junction capacitance at low frequency and coupling capacitor at high frequency
(D) device junction capacitor at high frequency and coupling capacitor at low frequency

c. An N-channel JFET has Pinch-off voltage, $V_P = -4V$. Given that $V_{GS} = -1V$, then the minimum V_{DS} for the device to operate in the Pinch-off region will be _____.

(A) + 1V **(B)** + 3V
(C) + 4V **(D)** + 5V

d. Class AB operation is often used in Power amplifiers in order to _____.

(A) get maximum efficiency **(B)** Remove even harmonics
(C) overcome crossover distortion **(D)** reduce collector dissipation

e. An amplifier has an open-loop gain of 1000, lower 3 dB cut-off frequency of 100 Hz and upper 3 dB cut-off frequency of 1 MHz. If a negative feedback of 60 dB is provided to this amplifier, then the lower 3 dB and upper 3 dB cut-off frequencies with feedback will be respectively _____.

(A) 33 Hz and 1 MHz **(B)** 50 Hz and 1 MHz
(C) 50 Hz and 2 MHz **(D)** 33 Hz and 2 MHz

f. The Barkhausen criterion for sustained oscillations is given by _____

(A) $A\beta = 1$ **(B)** $|A\beta| \geq 1$

(C) $|A\beta| < 1$ **(D)** $\angle A\beta = 180^\circ$

g. The purpose of phase-log compensation is to _____.

(A) make the op-amp stable at very high values of gain
(B) make the op-amp stable at very low values of gain
(C) reduce the unity gain frequency
(D) increase the bandwidth

h. The output time period of a transistorised monostable multivibrator using base resistor R_b and coupling capacitor C_b for the output transistor is given by _____.

(A) R_bC_b **(B)** $0.69\ R_bC_b$
(C) $2\ R_bC_b$ **(D)** $1.38\ R_bC_b$

i. If the load resistance of a capacitor filtered full-wave rectifier is reduced, the ripple voltage _____.

(A) increases **(B)** decreases
(C) is not affected **(D)** has a different frequency

j. The digital circuit as shown in Fig. 1 works as

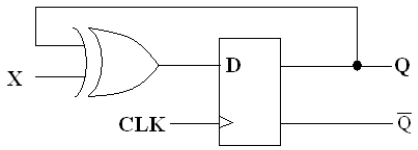

Fig. 1

(A) JK flip-flop **(B)** Clocked R-S flip-flop
(C) T flip-flop **(D)** Ring counter

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Sketch a family of Common-Base output characteristics for a transistor and indicate the active, cut-off and saturation regions. Explain the shapes of the curves qualitatively. **(8)**

b. A Zener diode as shown in Fig. 2 has V_Z = 12 V, determine the minimum and maximum Zener currents as well as the output voltage, when (i) the Zener diode is considered to be ideal one (ii) the Zener resistance of the Zener diode is 7 Ω. Comment on the results of the output voltage. **(8)**

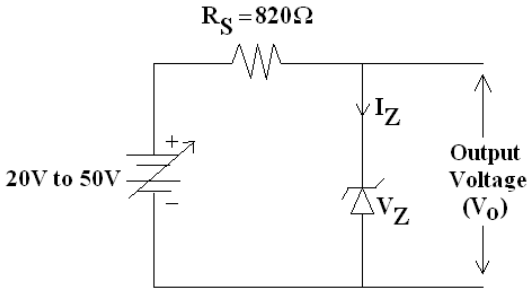

Fig. 2

Q.3 a. Draw the Hybrid-Π model for a transistor in Common Emitter configuration at high frequencies and explain the different parameters involved in the circuit. **(8)**

b. Draw the small-signal T-equivalent circuit of cascode amplifier and derive an expression for its voltage gain. Determine the voltage gain (A_V) of the cascoded amplifier. If $r_e' = 6.73\Omega$ and $R_C = 1.8k\Omega$. **(8)**

Q.4 a. Draw the small signal AC equivalent circuit of source follower at high frequencies and derive an expression for the input admittance and output admittance. What are the applications of source follower? **(9)**

b. A class B Push-pull power amplifier is supplied with V_{CC} =50 V. The signal swings the collector voltage down to V_{min} =5 V, and the total dissipation (P_d) in both transistors is 40 W. Find
(i) the DC power input (ii) the AC power output (iii) conversion efficiency. **(7)**

Q.5 a. What type of feedback is used in emitter follower? Draw the circuit of an emitter follower and show that the output voltage follows the input voltage. **(6)**

b. The gain of an amplifier is 100 and its bandwidth is 10 kHz. If 10% of negative feedback is applied in the basic amplifier, determine:
(i) the gain with negative feedback (ii) the bandwidth with negative feedback. **(4)**

c. Draw the circuit diagram of Hartley Oscillator using BJT and briefly explain how the oscillations are maintained in this oscillator. **(6)**

Q.6 a. Define slew rate and explain its importance in op-amp. **(5)**

b. Draw the circuit of an op-amp integrator and derive an expression for its output voltage. Also draw the output waveform for square wave input waveform. **(7)**

c. Find the output voltage V_o for the op-amp circuit as shown in Fig. 3. **(4)**

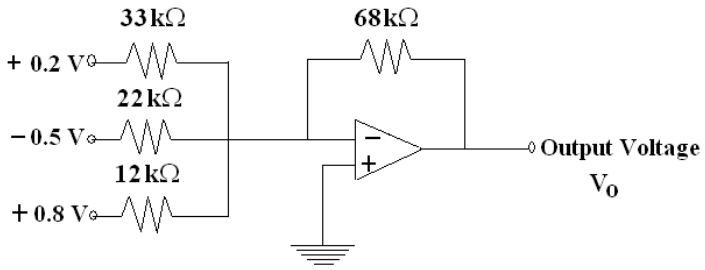

Fig. 3

Q.7 a. Draw the circuit of an astable multivibrator using op-amp and describe its operation with the help of output waveform. **(7)**

b. Design a Schmitt Trigger with V_{UT} = 5 V and V_{LT} = – 5 V. What is the hysteresis voltage? Assume $V_{sat} = \pm$ 10 V **(4)**

c. Draw the block diagram for IC555 Timer and explain briefly, the components used. **(5)**

Q.8 a. Draw the circuit of Transistor Shunt Voltage Regulator and explain its operation. What are its limitations? **(7)**

b. Draw the circuit of Full-wave Bridge Rectifier and explain its operation with the help of input and output waveforms. What is P.I.V. for this rectifier? **(9)**

Q.9 a. State and prove de-Morgan's theorems. **(5)**

b. Minimize the four-variable logic function
$f(A,B,C,D) = \sum m(0,1,2,3,5,7,8,9,11,14)$ using Karnaugh Map. **(6)**

c. What is a half-adder? Draw the logic diagram of a half-adder and explain its operation with the help of truth table. **(5)**