StudentBounty.com AMIETE - CS/IT (NEW SCHEME) Code: AC58/AT5 _

Subject: COMPUTER ORGANIZATION

Time: 3 Hours

DECEMBER 2010

NOTE: There are 9 Questions in all.

- Ouestion 1 is compulsory and carries 20 marks. Answer to 0.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after half an hour of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

Q.1 Choose the correct or the best alternative in the following:

 (2×10)

Max. Marks: 100

a. The basic performance equation for a computer is

(A) $T = \frac{N \times S}{R}$	$(\mathbf{B}) \ \mathrm{T} = \frac{\mathrm{N} \times \mathrm{R}}{\mathrm{S}}$
(C) $T = \frac{S \times R}{N}$	$(\mathbf{D}) \ \mathbf{N} = \frac{\mathbf{S} \times \mathbf{R}}{\mathbf{T}}$

b. The maximum positive and negative numbers which can be represented in 2's complement form using n bits are

$(\mathbf{A}) + (2^{n-1} - 1), -(2^{n-1} - 1)$	$(B) + (2^{n-1} - 1), -2^{n-1}$
(C) 2^{n-1} , -2^{n-1}	(D) 2^{n-1} , -(2^{n-1} + 1)

c. Registers R1 and R2 of a computer contain the decimal values 1200 and 4600 respectively. What is the effective address of the memory operand for the following instructions (i) Load 20(R1), R5 (ii) Subtract R1, R5

(A) 1220 and 5830	(B) 5830 and 4599
(C) 1200 and 4599	(D) 1220 and 1200

d. Negative numbers cannot be represented in

(A) Signed magnitude form	(B) 1's complement form
(C) 2's complement form	(D) 8-4-2-1 code

e. A k-bit field can specify any one of

(A) 3^{κ} registers	(B) 2^{κ} registers
(C) K^2 registers	(D) K ³ registers

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- f. SPEC rating=
 - (A) (Running time of reference computer)/(Running time of computer under test)
- StudentBounts.com (B) (Running time of computer under test)/ (Running time of reference computer)
 - (C) (Running time of reference computer)/(Running time of reference computer under test)
 - (D) None of the above

g. X(PC) denotes which type of addressing mode ?

(A) Index	(B) Indirect
(C) Relative	(D) none of these

h. In Assembly language programming, minimum number of operands required for an instruction is/are

(A) Zero.	(B) One.
(C) Two.	(D) Both (B) & (C).

After fetching the instruction from the memory, the binary code of the i. instruction goes to

(A) Program counter.	(B) Instruction registers.
(C) Accumulator.	(D) Instruction pointer.

- j. What is the content of Stack Pointer (SP)?
 - (A) Address of the current instruction
 - (B) Address of the next instruction
 - (C) Address of the top element of the stack
 - **(D)** Size of the stack.

Answer any FIVE Questions out of EIGHT Questions. Each question carries 16 marks.

Q.2	a.	Explain with neat diagram, steps taken by processor to execute followin instructions:-	g
		LOAD LOC A, R1 ADD R1, R0 (0	6)
		ADD KI, KO	0)

- b. Explain four different types of instruction a processor performs. Give an example for each. (6)
- c. Explain two ways to measure the performance of a processor (4)
- a. Describe the addressing scheme of the following assembly instructions:-**Q.3**

(i) MOVE LOC,R2	(ii) ADD (R1),R0	
(iii) ADD (R1,R2),R3	(iv) Branch > 0 $-8(PC)$	
(v) MOVE (R1),-(R2)	(vi) ADD #\$5D,R1	(12)

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	b.	Write an assembly program to find DOT product of two vectors using A Increment addressing mode Let two devices A and B have ID number 5 and 6 respectively request use bus. Explain the working of bus selection. Draw the timing diagram of handshake control of data transfer during an	
Q.4	a.	Let two devices A and B have ID number 5 and 6 respectively request use bus. Explain the working of bus selection.	ing to (5)
	b.	Draw the timing diagram of handshake control of data transfer during an and output operations.	(7)
	c.	Explain the working of direct memory access.	(4)
Q.5	a.	Differentiate parallel and serial port. Draw the diagram for interconnec keyboard to a processor and label various signals.	ting a (7)
	b.	Differentiate SCSI and PCI Bus. Write a short note on USB bus.	(6)
	c.	Draw the block diagram of serial interface.	(3)
Q.6	a.	Explain the diagram for the organization of $2M \times 32$ Memory modules us 512×8 memory chips. Explain the operation of data transfer from mem that use clock to processor.	0
	b.	Explain any three semiconductor RAM memories.	(6)
	c.	Explain performance issues considered in memory system.	(4)
Q.7	a.	Explain how to build 16 bit carry look ahead (adder) from 4 bit adders	(8)
	b.	Explain Address translation in virtual memory. Write short notes secondary storage.	on (8)
Q.8	a.	Multiply each of the following pair of binary number. In each of the ca assume A is the multiplicand and B is the multiplier A = 010111 and $B = 110110$ using Booth's algorithm	ase,
		A = 01101 and $B = 11010$ using bit pair recoding	(8)
	b.	Perform division operation on the following pair of binary numbers, in e case assume Q is dividend and M is divisor (i) $M = 11$ and $Q = 1000$, perform division using restore division method (ii) $M = 11$ and $Q = 1000$, perform division using non restoring division method	l
Q.9	a.	Explain hardwired control and microprogram control. Give their respect applications.	tive (8)
	b.	Explain the format of microinstruction.	(4)
	c.	Draw the block diagram of microinstruction sequencing.	(4)

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