## AMIETE - CS (OLD SCHEME)

Code: AC23 Subject: MICROPROCESSOR BASED SYSTEM DA Time: 3 Hours

## **DECEMBER 2010**

**NOTE:** There are 9 Questions in all.

- Student Bounts, com • Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after half an hour of the commencement of the examination.
- Out of the remaining EIGHT Questions, answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

## Q.1 Choose the correct or the best alternative in the following:

 $(2\times10)$ 

Max. Marks:

- a. Signal voltage ranges for a logic high and for a logic low in RS-232C standard are
  - (A) Low = 0 volts to 1.8 volts, high = 2.0 volts to 5 volts
  - **(B)** Low =-15 volts to -3 volts, high = +3 volts to +15 volts
  - (C) Low = +3 volts to +15 volts, high = -3 volts to -15 volts
  - **(D)** Low = 2 volts to 5.0 volts, high = 0 volts to 1.8 volts
- b. What will be the contents of register AL after the following has been executed

MOV BL, 8C

MOV AL, 7E

ADD AL, BL

- (A) 0A and carry flag is set
- **(B)** 0A and carry flag is reset
- (C) 6A and carry flag is set
- (D) 6A and carry flag is reset
- c. Which of the following statement is true?
  - (A) The group of machine cycle is called a state.
  - **(B)** A machine cycle consists of one or more instruction cycle.
  - (C) An instruction cycle is made up of machine cycles and a machine cycle is made up of number of states.
  - **(D)** None of the above
- d. A buffer is used to
  - (A) increase the output current
- **(B)** increase the output voltage
- **(C)** decrease the output current
- (**D**) none of the above
- The PCI bus is the important bus found in all the new Pentium systems because
  - (A) It has plug and play characteristics
  - **(B)** It has ability to function with a 64 bit data bus
  - (C) Any Microprocessor can be interfaced to it with PCI controller or bridge
  - **(D)** All of the above

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|     |    |  | 25  | E.                 |
|-----|----|--|---|--------------------|
|     | f. | Which pins are general purpose I/O pins during mode-2 operation of the 82C55?  (A) PAO – PA7 (B) PBO-PB7 (C) PC3-PC7 (D) PC0-PC2  If the crystal oscillator is operating at 15 MHz, the PCLK output of 8284 is (A) 2.5 MHz (B) 5 MHz |   |                    |
|     |    | (A) PA0 – PA7<br>(C) PC3-PC7   | ( <b>B</b> ) PB0-PB7<br>( <b>D</b> ) PC0-PC2                                      |                    |
|     | g. | . If the crystal oscillator is operating at 15 MHz, the PCLK output of 8284 is   |   |                    |
|     |    | (A) 2.5 MHz<br>(C) 7.5 MHz   | ( <b>B</b> ) 5 MHz<br>( <b>D</b> ) 10 MHz   |                    |
|     | h. | Which type of JMP instruction assembles if the distance is 0020 h bytes  |   |                    |
|     |    | <ul><li>(A) near</li><li>(C) short</li></ul>   | <ul><li>(B) far</li><li>(D) none of the above</li></ul>                           |                    |
|     | i. | Suppose that , if BX=0301, after execution of MOV AL, [BX + 1346H] the AL will have  |   |                    |
|     |    | <ul><li>(A) The content of 1647</li><li>(C) The content of 1346 + 0301</li></ul>   | ( <b>B</b> ) The content of 0301 + 1346 ( <b>D</b> ) The content of 1346          |                    |
|     | j. | When the 82C55 is reset, its I/O ports are all initializes as  |   |                    |
|     |    | <ul><li>(A) Output port using mode 0</li><li>(C) Output port using mode 1</li></ul>  | <ul><li>(B) Input port using mode 1</li><li>(D) Input port using mode 0</li></ul> |                    |
|     |    | Answer any FIVE Questions of Each question ca  |   |                    |
| Q.2 | a. | Explain DOS function call and BIOS function call with one ex each.   |   | of<br>( <b>8</b> ) |
|     | b. | What was Special about the 8087?   | ,   | (3)                |
|     | c. | Draw the block diagram of a microprocessor based computer system showing the address, data and control bus structure   |   | m<br>(5)           |
| Q.3 | a. | Explain the salient features of Pentium in brief.  |   | (6)                |
|     | b. | Discuss the following assembler d  | irectives with example.   | (10)               |
|     |    | (i) DWORD<br>(ii) OFFSET<br>(iii) SEGMENT<br>(iv) MACRO<br>(v) ASSUME  |   |                    |
| Q.4 | a. | Design the chip select and decoding logic to interface 8086 with eight 2764 (8 KB) EPROM at memory location 10000 H – 1 FFFFH and eight 4016 (2 KB) SRAM at memory locations 20000 H – 23 FFFH.                                      |   |                    |

Student Bounty.com stored in the memory location started at 3000 H. 0.5 a. Explain data addressing modes (with examples) available microprocessors. b. What are the contents of data bus and the states of Ao and BHE when the following instructions are executed in 8086. (i) CPU writes a byte 11H at memory locations 1000: 0002H. (ii) CPU writes a word 2211H at memory location 1000: 0003H. **Q.6** a. Show how a typical DMA controller can be interfaced to an 8086/8085 based maximum mode system. **(8)** b. Differentiate between synchronous and asynchronous types of serial communication. **(4)** c. What do you mean by A/D conversion? Explain Successive approximation A/D technique. **(4)** a. Explain the operation of 8279. Explain the following terms:  $\mathbf{Q.7}$ **(8)** (i) N key Roll over. (ii) Key board debounce. (iii) FIFO RAM. b. Given [BX] = 637D [S1] = 2A9B and displacement = C237. Determine the effective address resulting from these registers and the following addressing mode (i) Immediate (ii) Register using BX (iii) Direct (iv) Based Index Relative **(8) Q.8** a. Why are the 8086 memory and 80386 memory set up as 2 Byte and 4 Byte banks respectively. **(8)** b. Compare real mode memory addressing and protected mode memory addressing used in 8086. **(8)** 0.9 a. Discuss the features of EISA bus. **(6)** b. Discuss the following terms: (10)(i) Branch prediction logic in Pentium (ii) Cache structure in Pentium

b. Write a Program in assembly language to find the largest of n num

(iv) Super scalar architecture (v) Real time operating system.

(iii) Threaded system