Rewarding Learning

General Certificate of Secondary Education
2013

Technology and Design

Unit 2:
Systems and Control

Element 1: Electronic and Microelectronic Control Systems

[GTD21]

FRIDAY 7 JUNE, AFTERNOON

MARK SCHEME

General Marking Instructions

Introduction
Mark schemes are intended to ensure that the GCSE examinations are marked consistently and fairly. The mark schemes provide markers with an indication of the nature and range of candidates' responses. The mark schemes should be read in conjunction with these general marking instructions.

Assessment objectives
Below are the assessment objectives for GCSE Technology and Design.

Students must:
- recall, select and communicate their knowledge and understanding of technology and design in a range of contexts (AO1);
- apply skills, knowledge and understanding, in a variety of contexts and in designing and making products (AO2); and
- analyse and evaluate products, including their design and production (AO3).

Flexibility in marking
Mark schemes are not intended to be totally prescriptive. No mark scheme can cover all the responses which candidates may produce. In the event of an unanticipated answer, examiners are expected to use their professional judgement to assess the validity of answers. If an answer is particularly problematic, then examiners should seek the guidance of the Supervising Examiner.

Positive Marking
Examiners are encouraged to be positive in their marking, giving appropriate credit for what candidates know, understand and can do rather than penalising candidates for errors or omissions. Examiners should make use of the whole of the available mark range for any particular question and be prepared to award full marks for a response which is as good as might reasonably be expected of a 16-year-old GCSE candidate

Awarding zero marks
Marks should only be awarded for valid responses and no marks should be awarded for an answer which is completely incorrect or inappropriate.

Types of mark schemes
Mark schemes for tasks or questions which require candidates to respond in extended written form are marked on the basis of levels of response which take account of the quality of written communication.

Other questions which require only short answers are marked on a point for point basis with marks awarded for each valid piece of information provided.

Levels of response
Tasks and questions requiring candidates to respond in extended writing are marked in terms of levels of response. In deciding which level of response to award, examiners should look for the "best-fit" bearing in mind that weakness in one area may be compensated for by strength in another. In deciding which mark within a particular level to award to any response, examiners are expected to use their professional judgement. The following guidance is provided to assist examiners.

- ***Threshold Performance*:** Response which just merits inclusion in the level and should be awarded a mark at or near the bottom of the range.

- ***Intermediate Performance*:** Response which clearly merits inclusion in the level and should be awarded a mark at or near the middle of the range.

- ***High Performance*:** Response which fully satisfies the level description and should be awarded a mark at or near the top of the range.

Marking calculations
In marking answers involving calculations, examiners should apply the "own figure rule" so that candidates are not penalised more than once for a computational error.

Quality of written communication
Quality of written communication is taken into account in assessing candidates' responses to all tasks and questions that require them to respond in written form. These tasks and questions are marked on the basis of levels of response. The description for each level of response includes reference to the quality of written communication.

For conciseness, quality of written communication is distinguished within levels of response as follows:

Level 1: Quality of written communication is limited.
Level 2: Quality of written communication is satisfactory.
Level 3: Quality of written communication is very good.

In interpreting these level descriptions, examiners should refer to the more detailed guidance provided below:

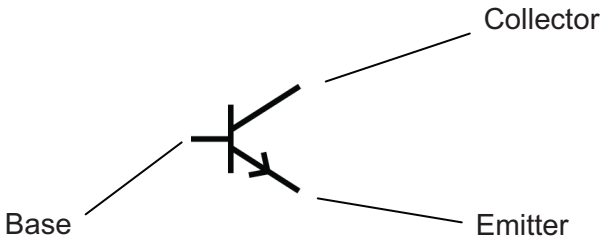
Level 1 (Limited): The level of accuracy of presentation, spelling, punctuation and grammar is limited. The candidate makes a limited selection and use of an appropriate form and style of writing. The organisation of material may lack clarity and coherence. There is little use of specialist vocabulary.

Level 2 (Satisfactory): The level of accuracy of presentation, spelling, punctuation and grammar is satisfactory. The candidate makes a satisfactory selection and use of an appropriate form and style of writing supported with appropriate use of diagrams as required. Relevant material is organised with some clarity and coherence. There is some use of specialist vocabulary.

Level 3 (Very Good): The level of accuracy of presentation, spelling, punctuation and grammar is very good. The candidate successfully selects and uses the most appropriate form and style of writing, supported with precise and accurate use of diagrams where appropriate. Organisation of relevant material is very good. There is very good use of appropriate specialist vocabulary.

AVAILABLE MARKS

1 (a) (i)



Arrow on correct leg
Neat drawing [2]

(ii) Correct labelling of Base, Collector and Emitter. [3]

(iii) When a voltage of ≈ 0.7 V is applied at its base.
Voltage value
Applied at base [2]

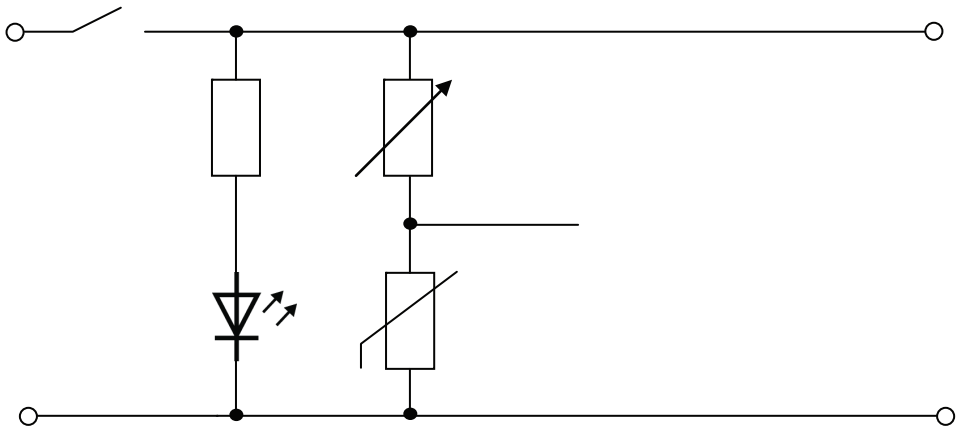
(b) (i) Potential Divider Circuit or Temperature sensing circuit [1]

(ii) Component A: Variable Resistor [1]
Component B: Thermistor [1]

(iii) Single pole, single throw [1]

(iv) Reference to:
When the SPST switch is closed circuit is switched on/power to circuit
Variable resistor allows the sensitivity of circuit to be set
Assume negative temperature coefficient thermistor
In cold conditions the thermistor resistance increases/vice versa
When this happens current will flow to point x to provide output [4]

(c) (i) Resistor
LED (Arrow directions and orientation)
Connections [4]

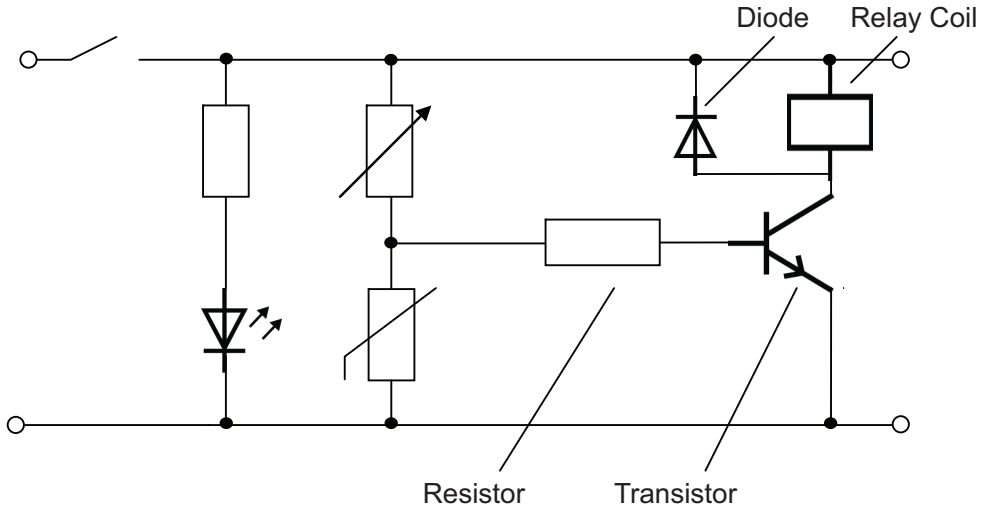


(ii) SPST switch closes, power on
Current flow from 9V line to 0V line
Resistor protects the LED from too high current
LED switched on [4]

(iii) Serves as a circuit on indicator/warning [1]

(iv) V = 9 – 2 = 7V
R = 7/6
R = 1.167kΩ or 1167Ω [1] for value, [1] for units [4]

(d) **(i)** Relay Coil drawn correctly, labelled and in correct location
Transistor switch drawn correctly and in correct location
Resistor drawn correctly and in correct location
Diode drawn correctly and in correct location [1] Orientation [1]
Diode connections to circuit 9V rail and bottom of relay coil
Transistor, resistor and relay connections all correct [7]



(ii) Resistor
To protect the transistor from too high a base current
Diode
To protect the relay coil from back EMF [4]

(iii) To switch on a motor or to switch on a higher voltage circuit [1]

40

2 **(a)** Possible method . . .

Breadboard, Computer Software, Proprietary kit, Copper strip . . . [1]

(b) Example: screen modelling, no handling of parts, simulation, improved efficiency. [2]

(c) Main differences:

Digital components are either on or off
Analogue components give a constant signal that varies in strength/ weakness [2]

(d)

Component	Digital/Analogue
7 Segment Display	Digital
Toggle Switch	Digital
LDR	Analogue
Reed Switch	Digital

[4]

(e)

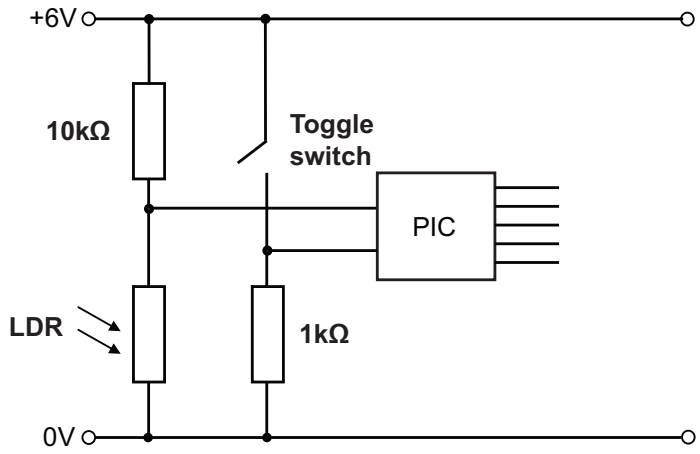


Fig. 3

[4]

AVAILABLE MARKS

(f) (i)

LIGHTS		BIT PATTERN
Red and Yellow LEDs on		0 0 0 1 1
Wait 2 sec		
Green and Blue LEDs on		0 1 1 1 1
Wait 4 sec		
All LEDs off		0 0 0 0 0
Wait 2 sec		
All LEDs on		0 1 1 1 1
Wait 10 sec		
All LEDs off		0 0 0 0 0
END		

Fig. 4

[9]

AVAILABLE MARKS

(ii)

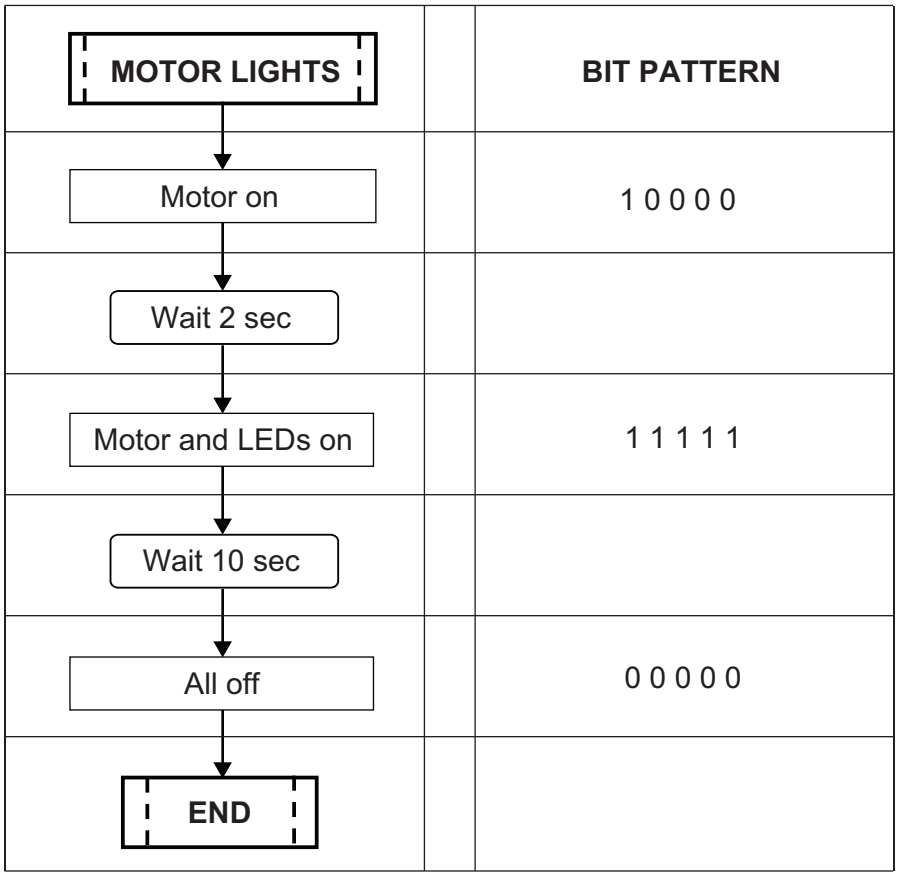


Fig. 5

[6]

AVAILABLE MARKS

(iii)

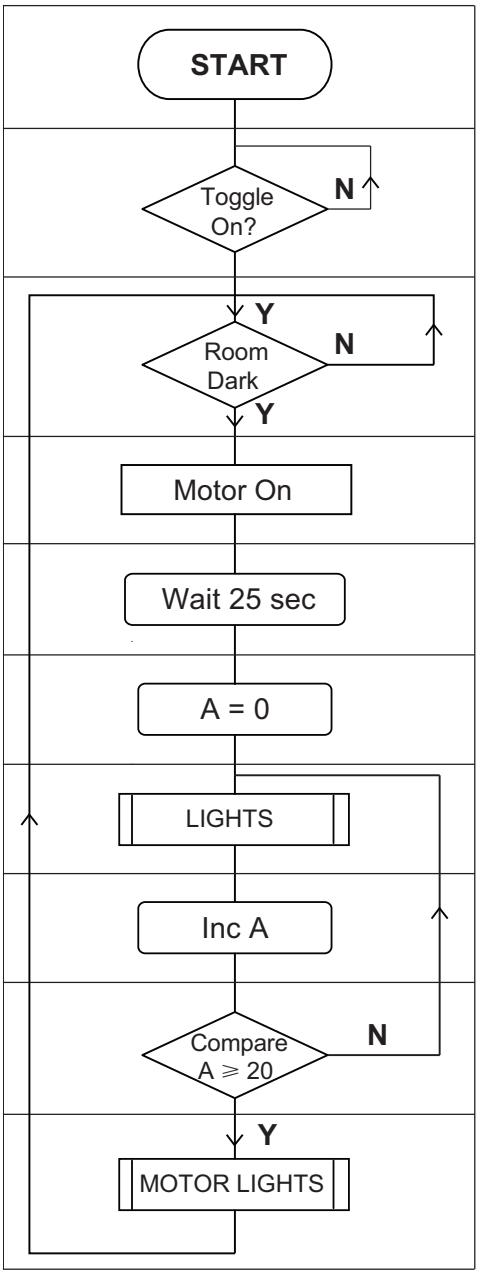


Fig. 6 [12] 40

Total **80**

AVAILABLE MARKS