Candidate Name	Centre Number	Candidate Number
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WJEC CBAC

GCSE

294/02

ELECTRONICS

MODULE TEST E2

HIGHER TIER

P.M. FRIDAY, 6 June 2008

45 minutes

For Examiner's use only

Total Mark	

ADDITIONAL MATERIALS

In addition to this examination paper you may need a calculator.

INSTRUCTIONS TO CANDIDATES

Write your name, centre number and candidate number in the spaces at the top of this page.

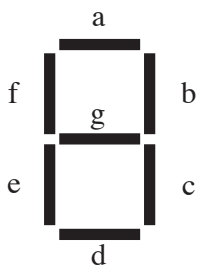
Answer **all** the questions in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.

Answer **all** questions

1. The diagram shows the arrangement of the LEDs in a seven-segment display.



Complete the following table.

Segments							Number Displayed
a	**b**	**c**	**d**	**e**	**f**	**g**	
1	1	1					**7**
1	1	1	1	0	0	1	

[2]

2. *(a)* Complete the truth tables for the following logic gates:

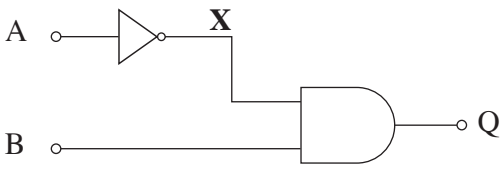
(i) a **NOT** gate [1]

Input	Output
0	
1	

(ii) an **AND** gate [1]

Inputs		Output
0	0	
0	1	
1	0	
1	1	

(b) Complete the following truth table for this system. [2]

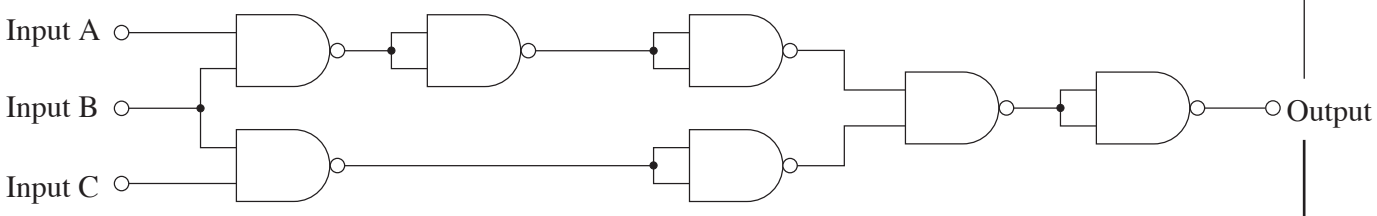


Input A	Input B	X	Q
0	0		
0	1		
1	0		
1	1		

(c) (i) Complete the diagram to show how a NAND gate can be made to behave as a NOT gate. [1]

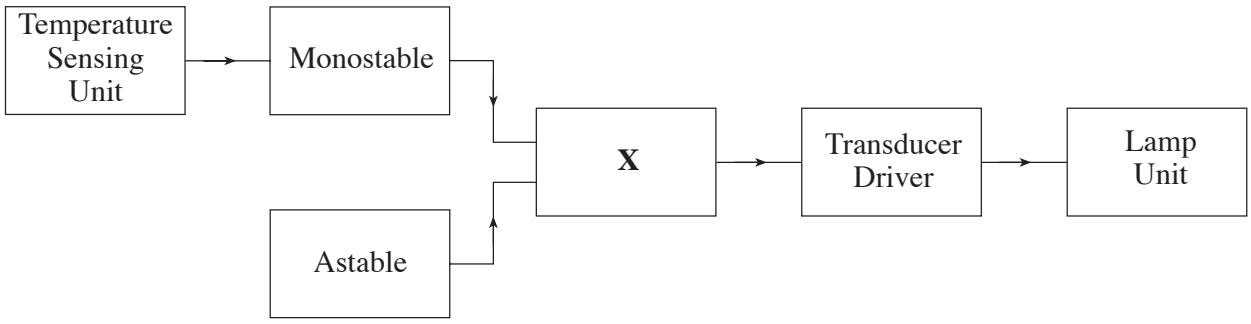
(ii) Draw a diagram to show the NAND gate equivalent of an AND gate [1]

(iii) Here is a logic system built using only NAND gates.



Cross out all redundant gates [1]

3. Here is the block diagram for a freezer alarm.



The lamp does not light when the freezer is cold enough.
The lamp flashes on and off repeatedly when the freezer is too hot.
The monostable outputs a logic 1 signal for 30 s when the freezer gets too hot.

(a) What type of logic gate is required in block **X**? [1]

Answer .....

(b) What is the job of the astable in this system?

Choose one of the following answers:

A. It makes the Lamp Unit pulse on and off over and over again.

B. It outputs a steady logic 1 signal when the freezer gets too hot.

C. It keeps the Lamp Unit switched on for 30s and then switches it off automatically.

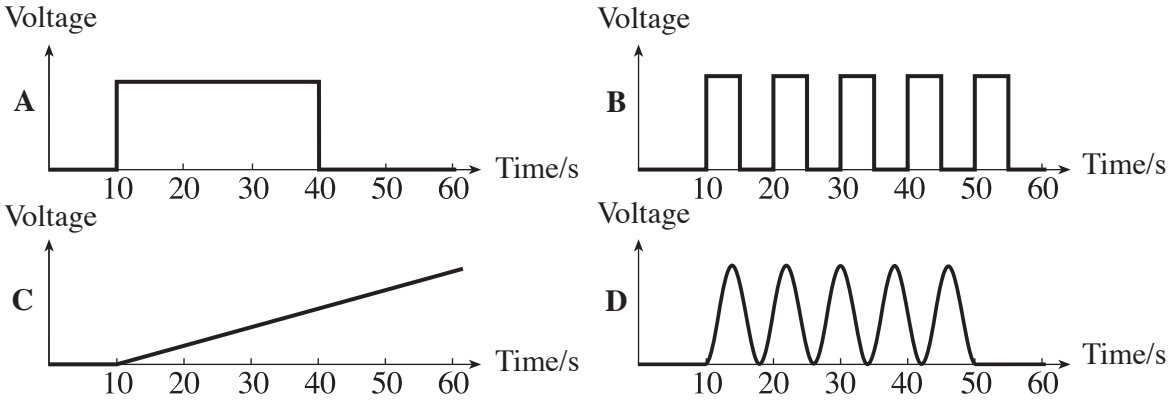
D. It buffers the output of the monostable, providing enough current to light the lamp.

[1]

Answer .....

(c) The temperature in the freezer rises and triggers the monostable.

Which of the following shows the output signal from the monostable?



[1]

Answer .....

(d) The monostable time delay can be found from the formula

T = 1.1 RC (where T is in seconds, R is in MΩ and C is in μF)

This can be re-arranged into the form:

$$\mathbf{R = \frac{T}{1.1C}}$$

The monostable circuit uses a 470 μF capacitor.

Calculate the value of resistance needed to produce a time delay of 30 s. [2]

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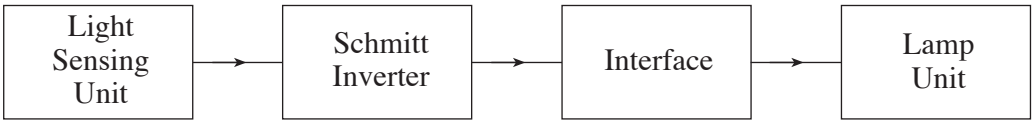
4. The block diagram shows the design of a security light, which turns on automatically when it gets dark.



(a) The Light Sensing Unit gives out a logic 0 signal in the dark.

(i) The Schmitt Inverter inverts the signal from the Light Sensing Unit.

Explain what this sentence means. [1]

.....

.....

(ii) What is the other use of the Schmitt Inverter in this system? [1]

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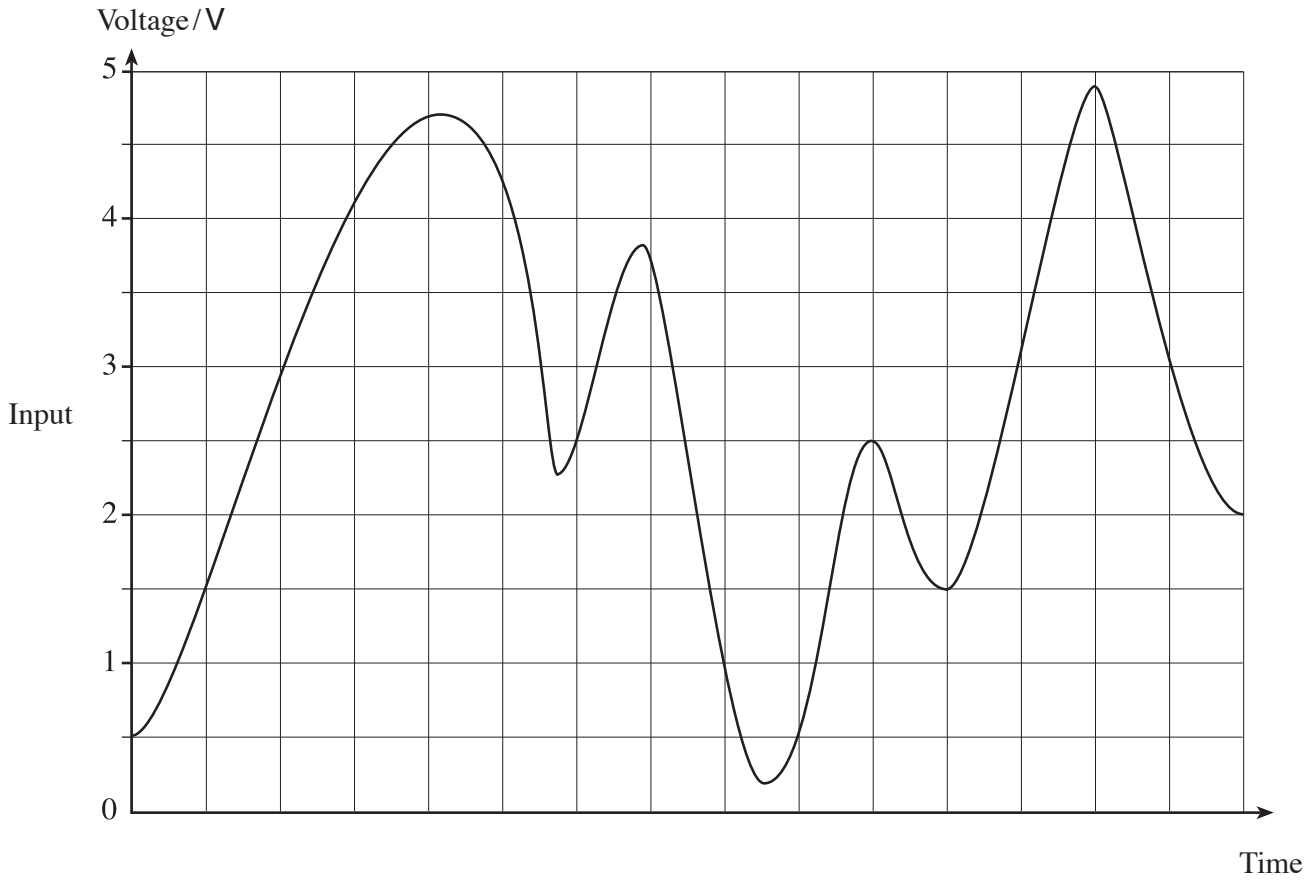
(b) Here is part of a data sheet for a Schmitt Inverter:

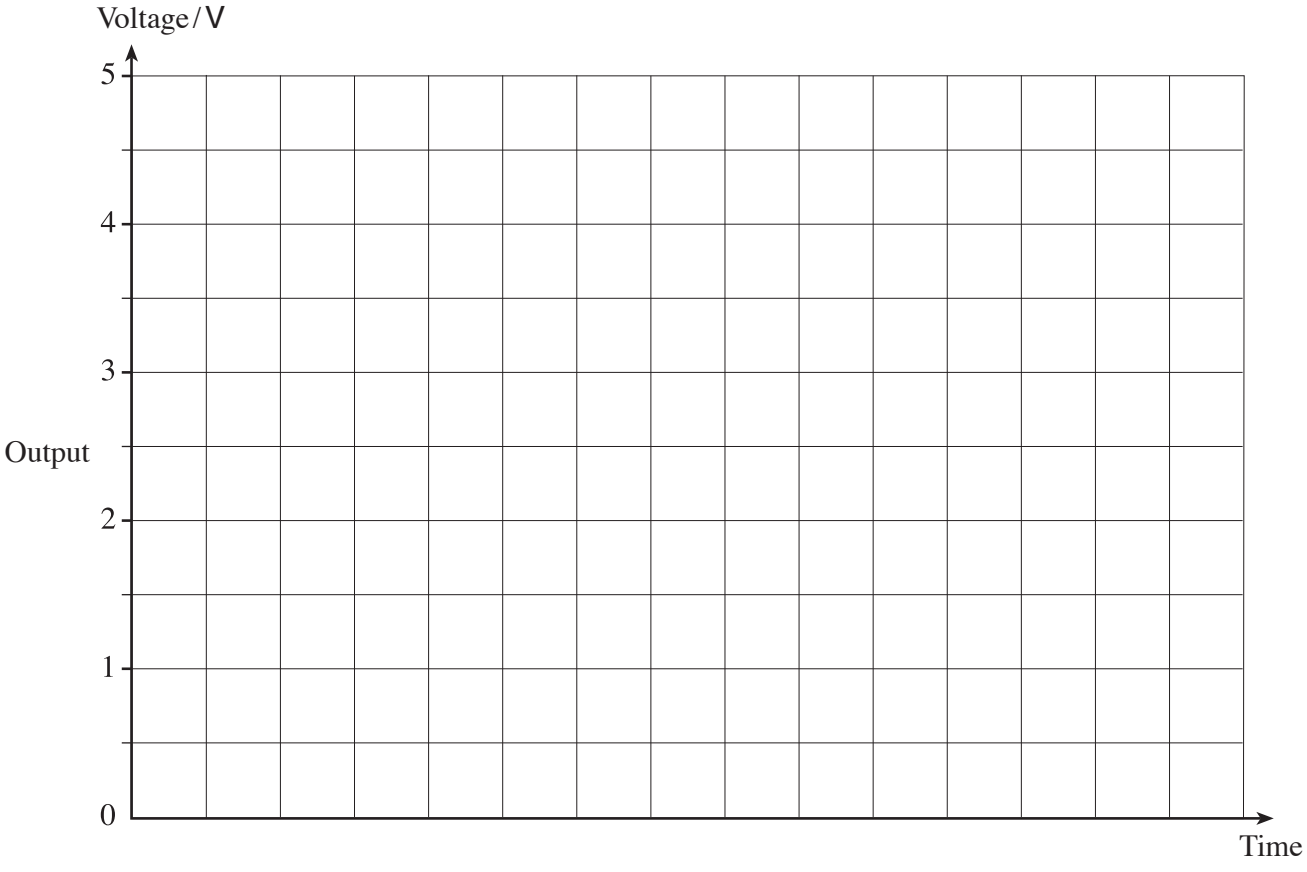
When connected to 5 V supply:

- Logic 0 = 0 V
- Logic 1 = 5 V
- The output changes from logic 1 to logic 0 when a **rising** input voltage reaches 3 V
- The output changes from logic 0 to logic 1 when a **falling** input voltage reaches 1 V

The input signal for the Schmitt Inverter is shown below.

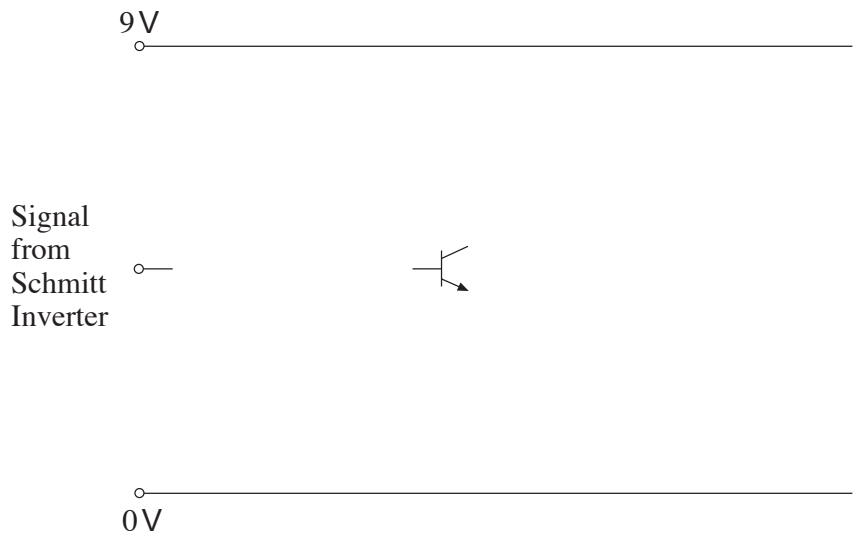
Use the axes provided to draw the resulting output signal produced by the Schmitt Inverter. [4]





Examiner only

(c) (i) Complete the circuit diagram to show how a transistor switch can be used to interface the Schmitt Inverter to the bulb. [3]



(ii) A thyristor is often used as an interface device. Why is it **not** suitable in this system? [1]

.....

.....

5. An electronic system has two input sensors **A** and **B**, and three outputs **P**, **Q** and **R**. The truth table showing how the input sensors control the outputs is shown below.

B	A	P	Q	R
0	0	1	1	1
0	1	1	1	0
1	0	0	1	0
1	1	0	0	0

(a) Which of the following expressions correctly describes the **P** output? [1]

A **NOT A** **B** **NOT B**

Answer .....

(b) Which of the following expressions correctly describes the **Q** output? [1]

A AND B **A OR B** **A NAND B** **A NOR B**

Answer .....

(c) Complete the following diagram to show how the **R** output can be obtained using a single logic gate. [1]

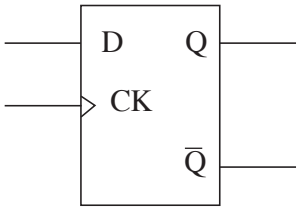
(d) **Another** electronic system uses a memory IC rather than logic gates to control output devices from input sensors.

The memory IC has 4 address pins and 8 data pins.

(i) How many outputs can be connected to the memory IC? ..... [1]

(ii) How many memory locations are there on the memory IC? ..... [1]

6. *(a)* The D-type flip-flop can be used for data transfer, under the control of the clock. The D-type flip-flop is rising-edge triggered.

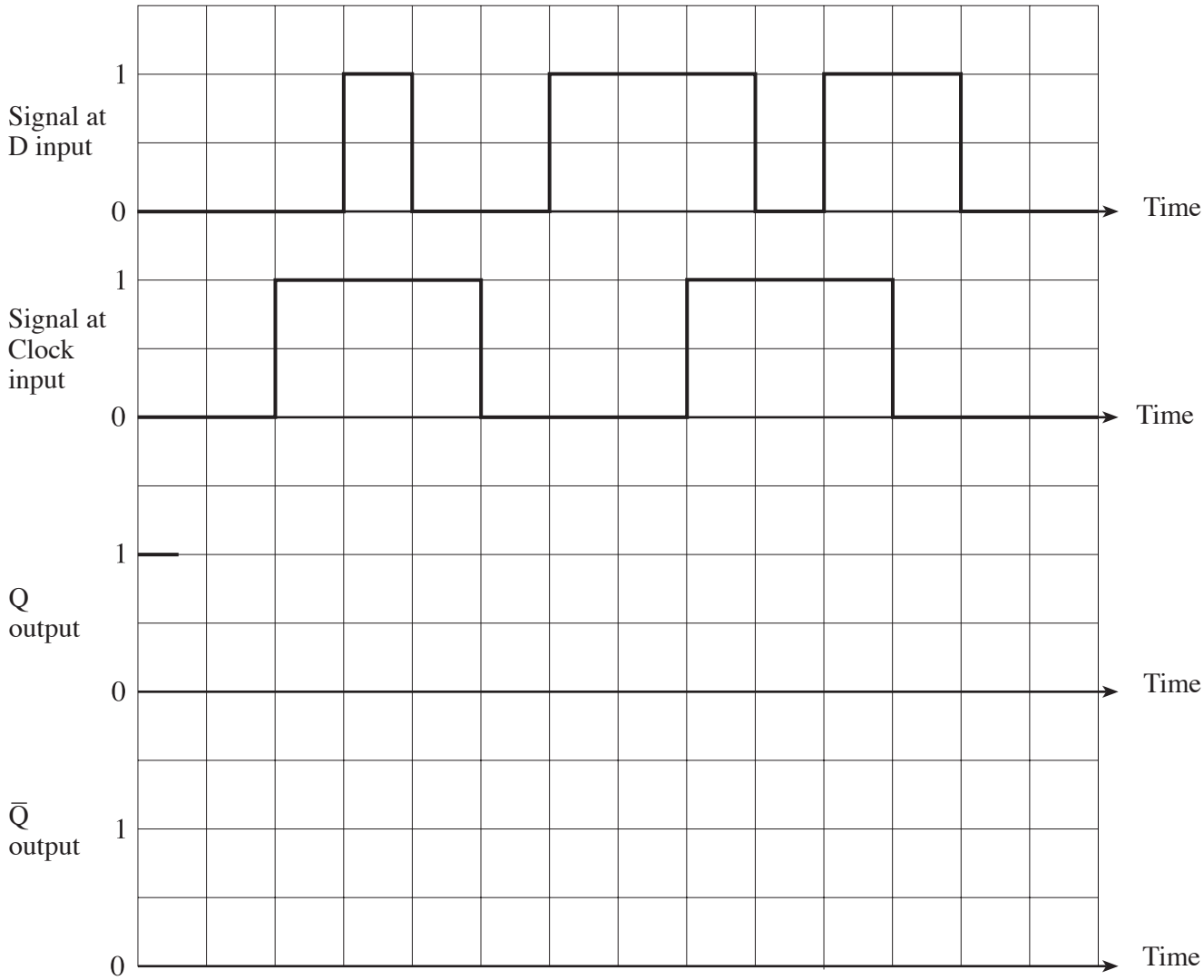


The signal shown in the first graph is sent into the D input.

The second graph shows the pulses sent into the clock input.

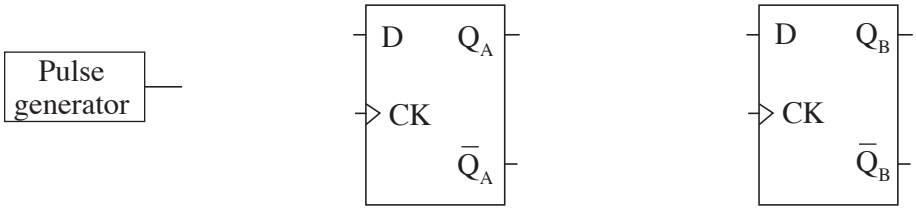
Use the axes provided to draw the signals at the Q and $\overline{Q}$ outputs.

The Q output is initially at logic 1. [3]



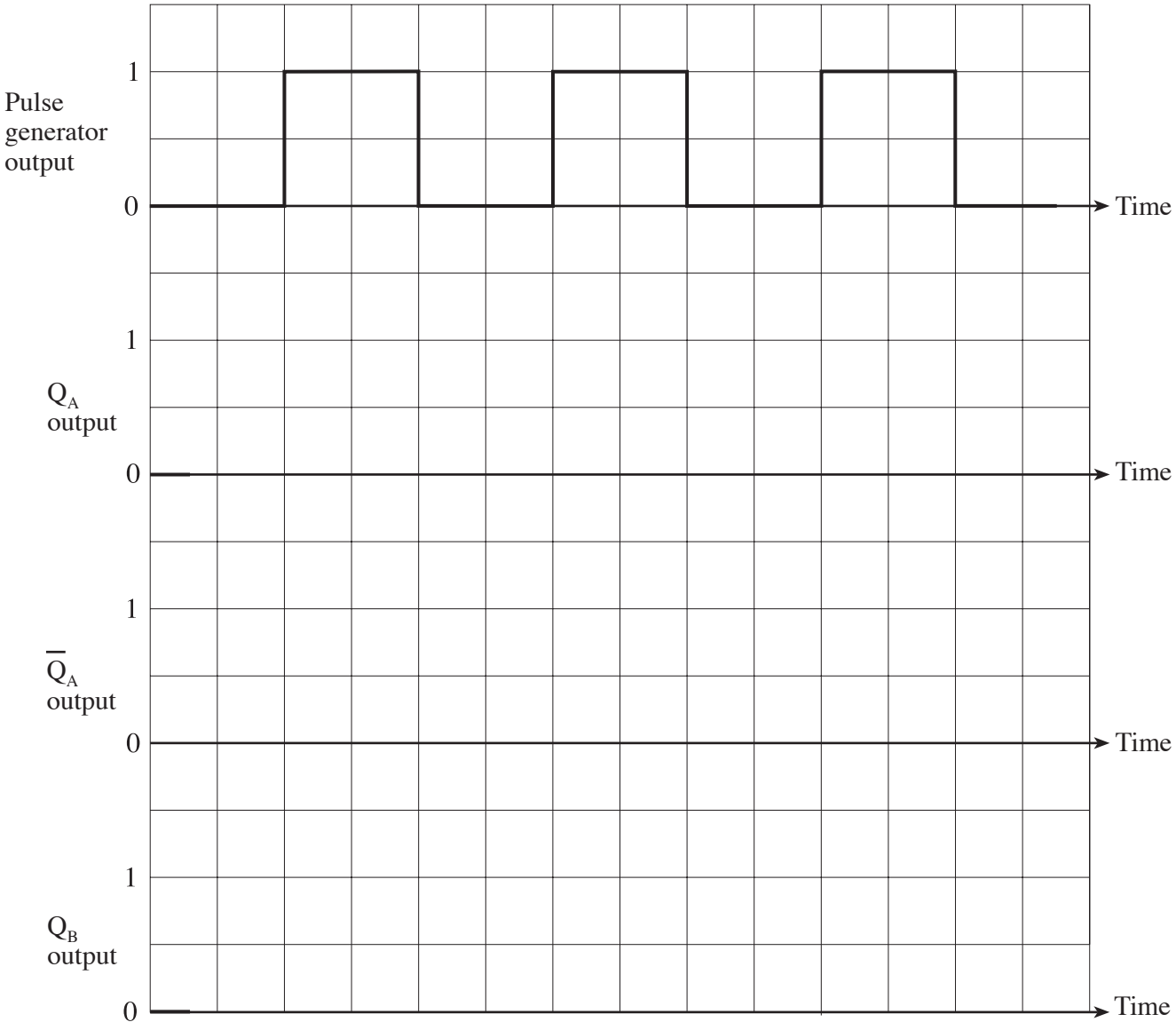
(b) A binary counter can be built from a series of D-type flip-flops, or can be obtained as a dedicated counter IC.

(i) The following diagram shows a pulse generator and two **rising-edge** triggered D-type flip-flops



Draw on the diagram the connections required to make a 2-bit up-counter, connected to the pulse generator. [3]

(ii) The graph shows clock pulses applied to the 2-bit up-counter.
Use the axes provided to draw the signals which would appear at the outputs of the two flip-flops. [3]
Initially the Q_A output and the Q_B output are both at logic 0.



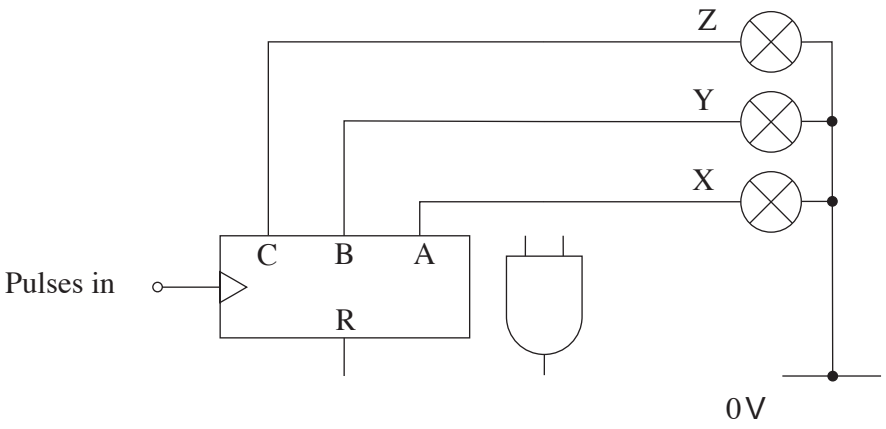
(c) The next diagram shows a counter IC, used to control a lighting sequence.

The sequence is given in the table.

Pulse number	Lamp State		
	Z	**Y**	**X**
0	Off	Off	Off
1	Off	Off	On
2	Off	On	Off
3	Off	On	On
4	On	Off	Off
5	On	Off	On
6	Off	Off	Off
7	Off	Off	On
Sequence continues			

A lamp is switched on when the corresponding counter output is logic 1.

A partly completed circuit diagram is shown below.



Complete the circuit diagram by adding suitable connections from the counter to the AND gate. [2]