GCSE MARKING SCHEME

SUMMER 2016

ELECTRONICS E1
4161/01

INTRODUCTION

This marking scheme was used by WJEC for the 2016 examination. It was finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conference was held shortly after the paper was taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conference was to ensure that the marking scheme was interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conference, teachers may have different views on certain matters of detail or interpretation.

WJEC regrets that it cannot enter into any discussion or correspondence about this marking scheme.

GCSE ELECTRONICS - E1

SUMMER 2016 MARK SCHEME

1. (a) 7 V

(b) 5 mA

(c) 2 V

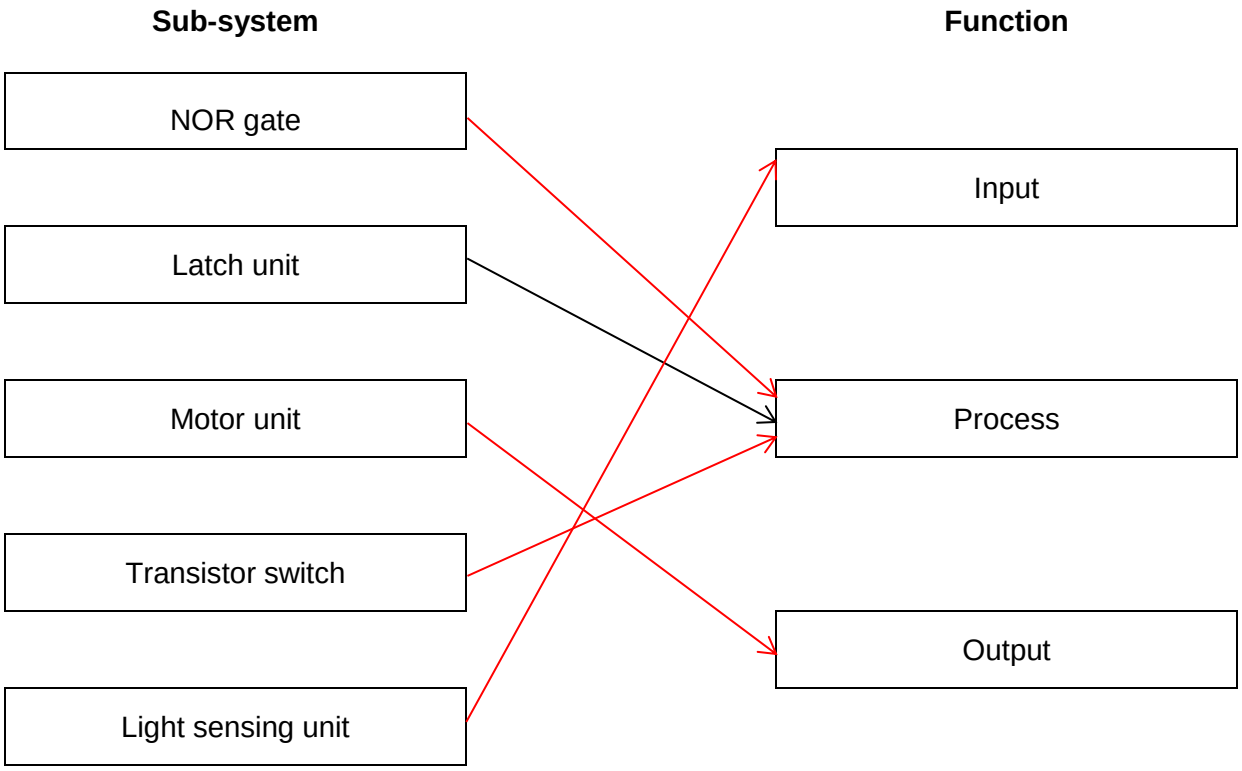
(d) 8 mA

[4]

2. (a) Diode
Variable resistor
Thyristor

[3]

(b)



[4]
{-1 for each additional line drawn.}

3. (a) 4

[1]

(b) OR gate

[1]

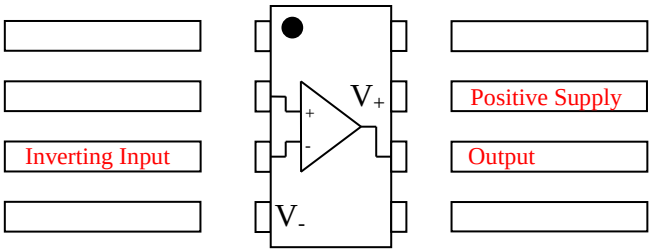
(c) 11

[1]

4. NAND gate NOT gate AND gate

[3]

5. The following diagram shows the pinout of a comparator IC.



[3]

6. Red Violet Yellow

[3]

7. (a) (i)

☑ $P = 9 \times 0.4$

[1]

(ii) 3.6 W

[1]

(b) B & D

[1]

8. (a) LDR

[1]

(b) 9 V

[1]

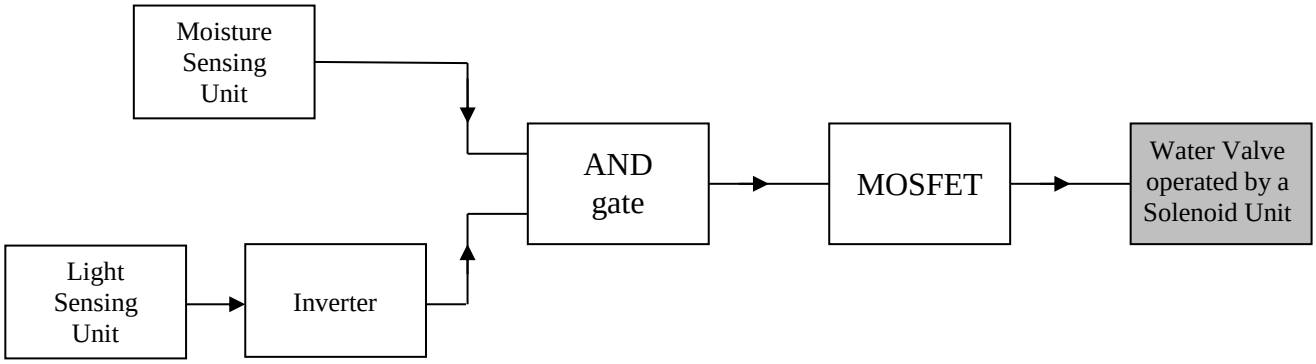
(c) (i) ☑ V_{OUT} would increase

[1]

(ii) Resistance of LDR decreases, so voltage across resistor will increase

[1]

9.



[5]

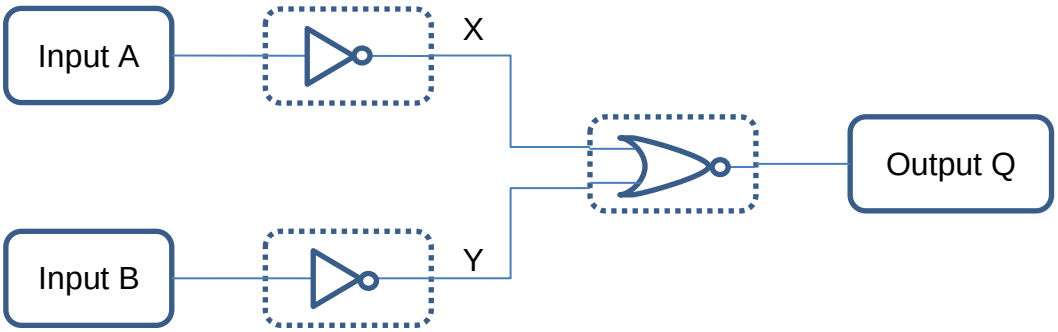
10. (a) NAND gate

[1]

(b) OR gate

[1]

11. (a)

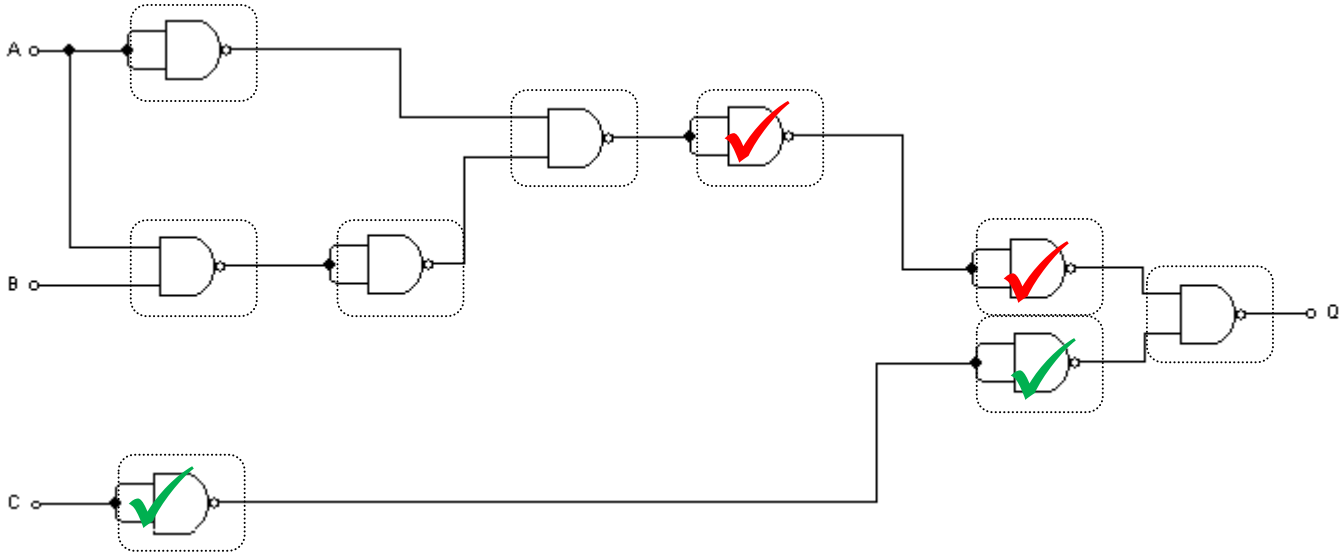


{2 × NOT gates = 1 mark, NOR Gate – 1 mark}
[2]

(b) AND gate

[1]

12.



[2]
{-1 for extra gates deleted}

13. 2.1 kΩ

41 kΩ

1.44 kΩ

[3]

14. (a) $Q = \overline{A}.\overline{B}$

[1]

(b) $Q = \overline{A}.B + A.\overline{B}$

[1]

15.

Standard Gate	NAND Equivalent Circuit
	Diagram A
	Diagram D
	Diagram C

[3]

16. (a) Resistor in P
Switch in Q Both required for 1 mark

[1]

(b) Pull Down Resistor / It pulls the input B to 0 V (logic 0) when the switch S_2 is open.

[1]

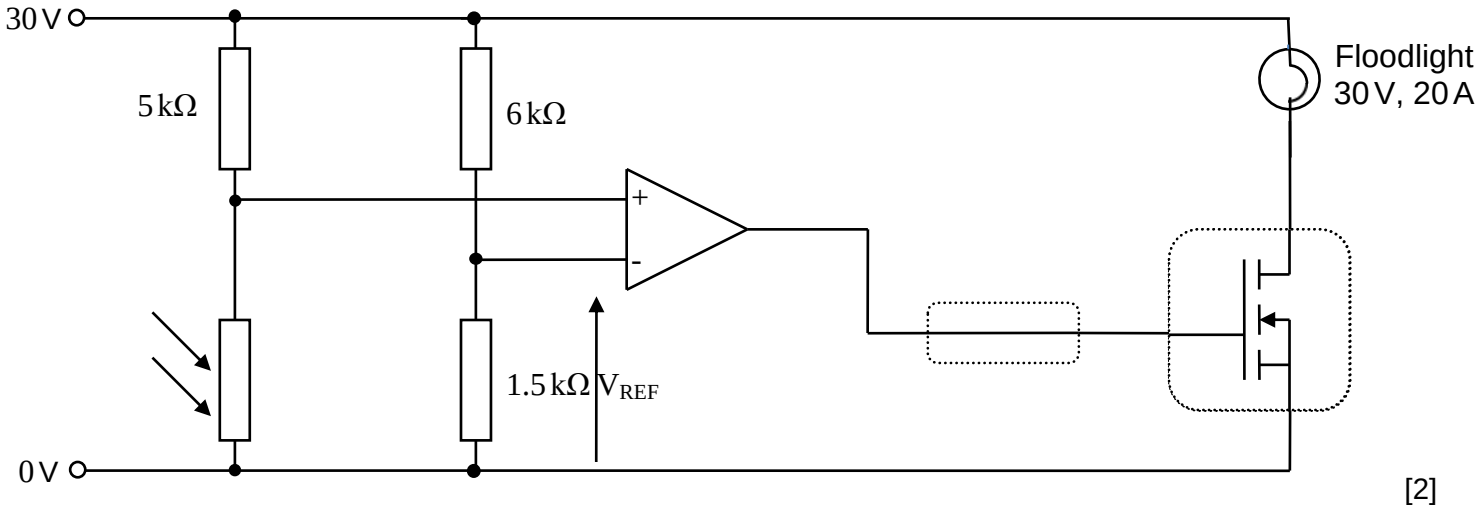
17. (a) $V_{REF} = \frac{1.5}{6+1.5} \times 30$

[1]

(b) $V_{REF} = 6\,V$

[1]

(c)



[2]

18. (a) 10 V

[1]

(b) $R = \frac{10}{16}$

[1]

(c) $R = 0.625\ k\Omega$

[1]

(d) $680\,\Omega$

[1]