



GCSE

4162/01

ELECTRONICS

UNIT E2 – Paper replacement test

P.M. TUESDAY, 21 June 2016

1 hour plus your additional time allowance

Surname _____

Other Names _____

Centre Number _____

Candidate Number 0 _____

For Examiner's use only		
Question	Maximum Mark	Mark Awarded
1.	4	
2.	3	
3.	2	
4.	4	
5.	3	
6.	2	
7.	3	
8.	3	
9.	2	
10.	3	
11.	3	
12.	3	
13.	5	
14.	5	
15.	2	
16.	2	
17.	2	
18.	3	
19.	6	
Total	60	

ADDITIONAL MATERIALS

In addition to this paper you may require a calculator and a ruler and separate insert.

INSTRUCTIONS TO CANDIDATES

Use black ink, black ball-point pen or your usual method.

Write your name, centre number and candidate number in the spaces provided on the front cover.

Answer ALL questions in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.

Answer ALL questions.

1(a) The boxes on the left give the names of two sub-systems.

The boxes on the right give descriptions of three applications.

Draw a line to link each sub-system to its correct application. [2]

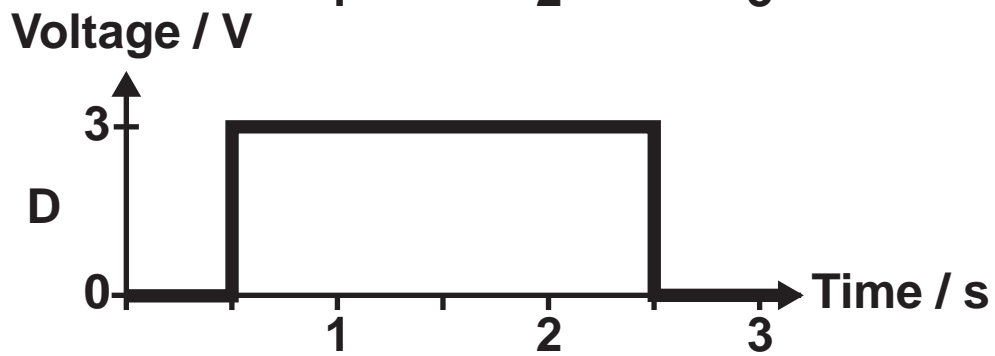
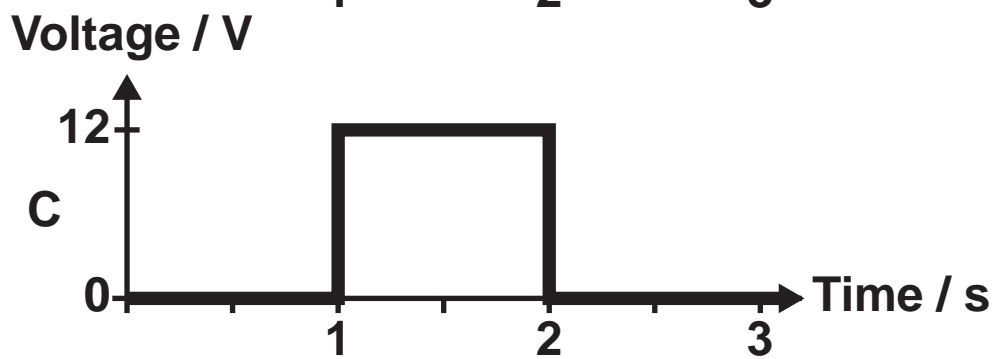
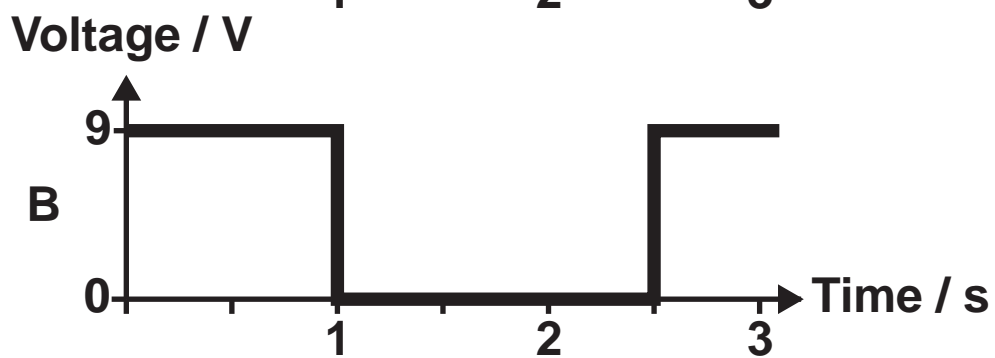
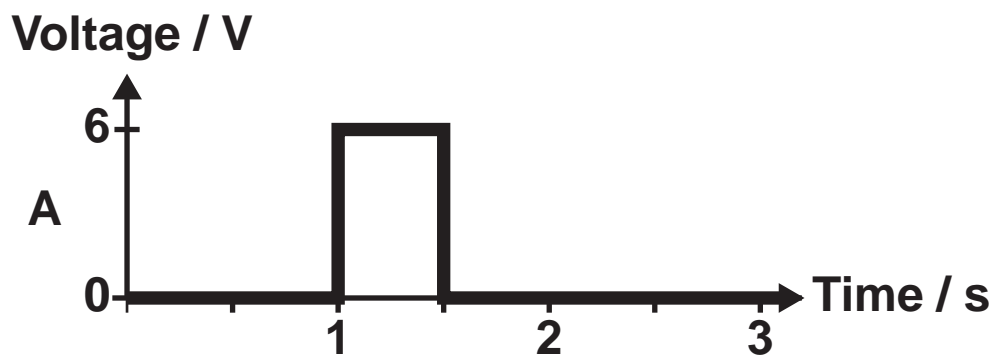
Monostable

When a burglar alarm is switched on a warning LED flashes on and off, repeatedly.

A street light comes on when it gets dark and turns off when it gets light.

Astable

The buzzer in a shop comes on for 10 seconds when someone steps on a pad in the doorway and then goes off automatically.



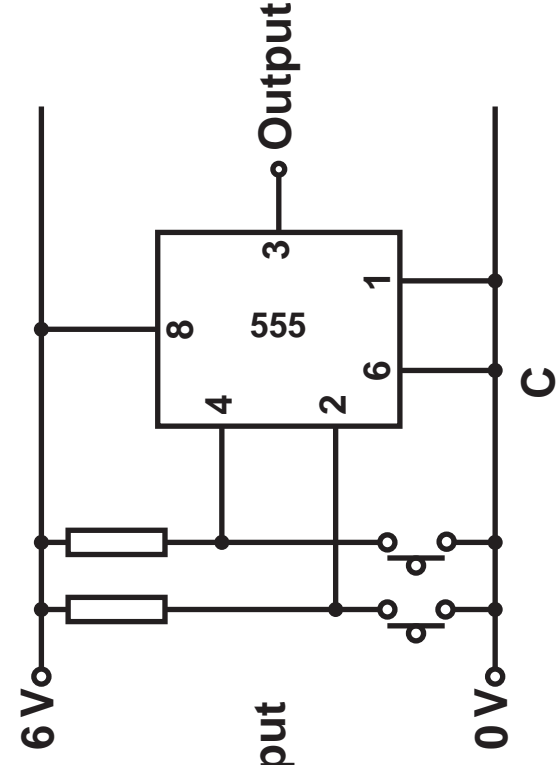
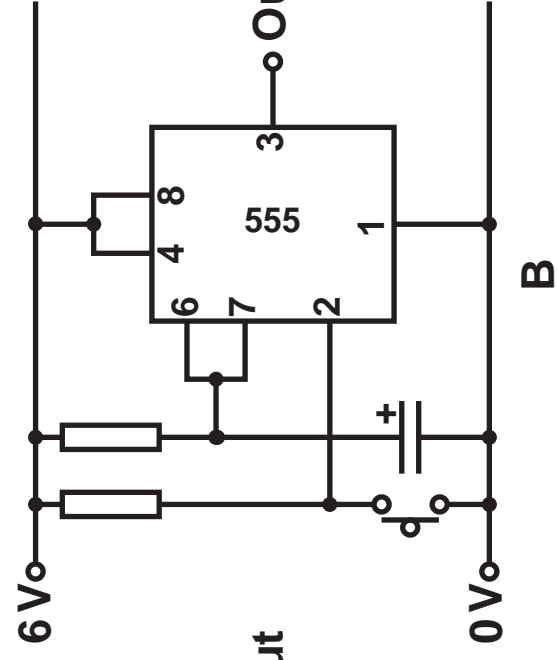
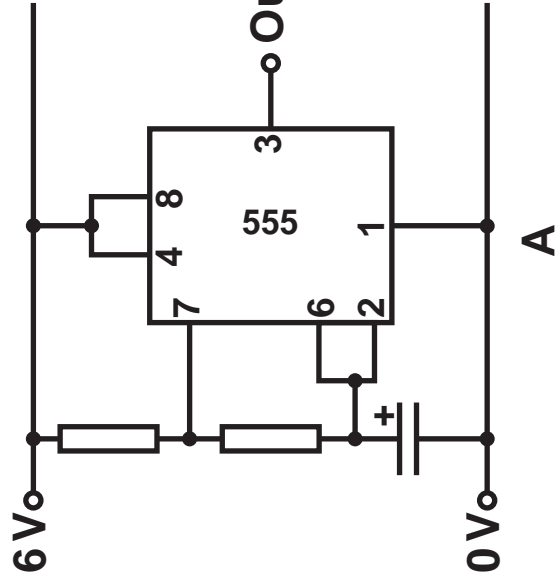
1(b) Shown opposite are four signals generated by monostable circuits.

(i) Which signal has the longest period?
(Tick (✓) the correct answer.) [1]

A	<input type="checkbox"/>
B	<input type="checkbox"/>
C	<input type="checkbox"/>
D	<input type="checkbox"/>

(ii) Which signal has the largest amplitude?
(Tick (✓) the correct answer.) [1]

A	<input type="checkbox"/>
B	<input type="checkbox"/>
C	<input type="checkbox"/>
D	<input type="checkbox"/>



2(a) One of the circuits shown opposite is an astable circuit, one a latch and one a monostable.

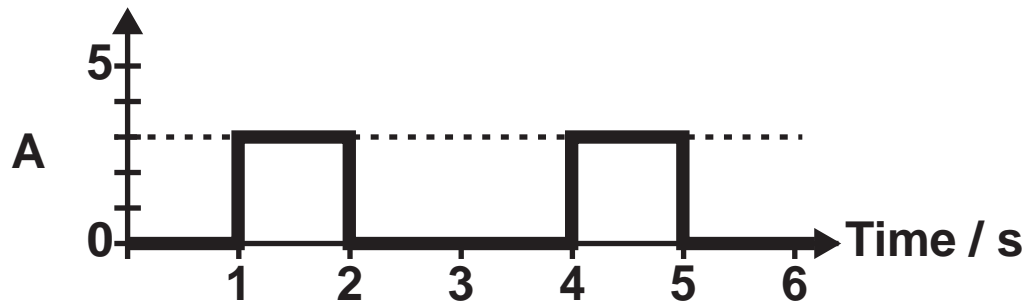
Which one is an astable circuit?
(Tick (✓) the correct answer.) [1]

A

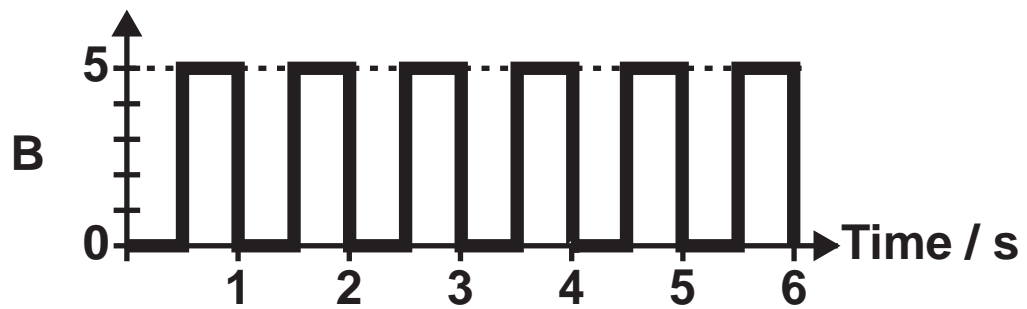
B

C

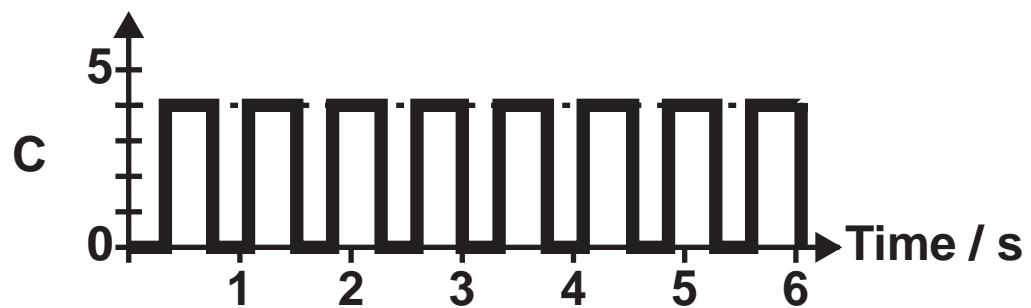
Voltage / V



Voltage / V



Voltage / V



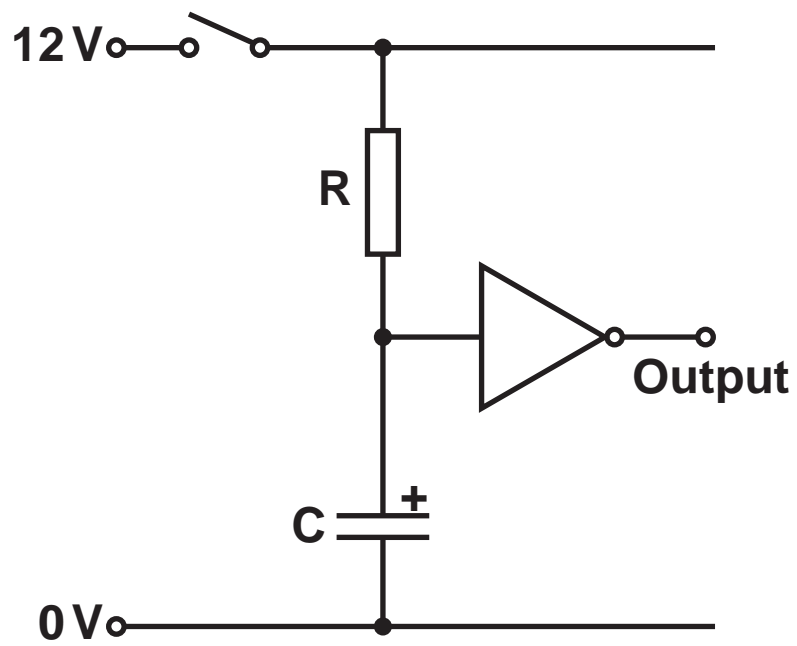
2(b) Shown opposite are three astable signals.

- (i) Which has the highest frequency?
(Tick (✓) the correct answer.) [1]

A	<input type="checkbox"/>
B	<input type="checkbox"/>
C	<input type="checkbox"/>

- (ii) What is the amplitude of signal A in volts?
(Tick (✓) the correct answer.) [1]

1	<input type="checkbox"/>
2	<input type="checkbox"/>
3	<input type="checkbox"/>
4	<input type="checkbox"/>



3. The circuit diagram shown opposite shows a time delay circuit. When the switch is closed, the output stays at a high voltage for a while and then drops to a lower value.

(a) Which one of the following sets of resistor/capacitor values keeps the output high for the longest time? (Tick (✓) the correct answer.)

[1]

SET	RESISTOR	CAPACITOR
A	10 k Ω	220 μ F
B	100 k Ω	220 μ F
C	10 k Ω	22 μ F
D	100 k Ω	22 μ F

<input type="checkbox"/>
<input type="checkbox"/>
<input type="checkbox"/>
<input type="checkbox"/>

3(b) Which one of the following statements gives the BEST explanation for the purpose of the NOT gate in this circuit? (Tick (✓) the correct answer.) [1]

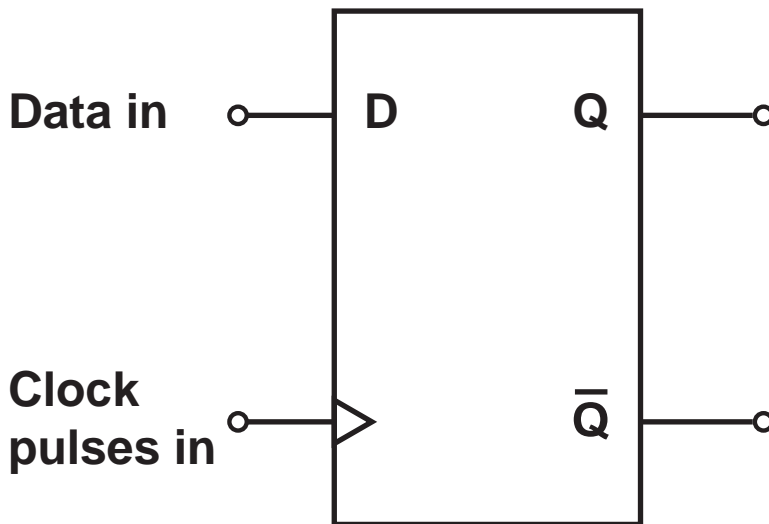
Without the NOT gate, the time delay would be much shorter.

It produces an analogue output voltage.

It ensures that the output current does not affect the time delay.

It inverts the signal from the switch.

- 4(a) Which of the following statements describes the action of the rising-edge triggered D-type flip-flop? (Tick (✓) the correct answer.) [1]



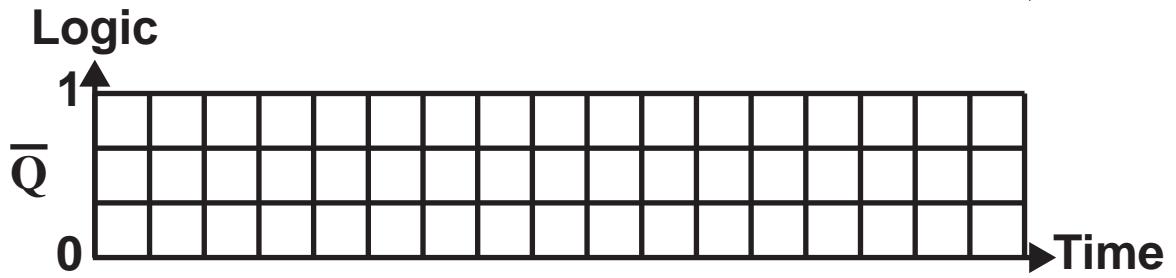
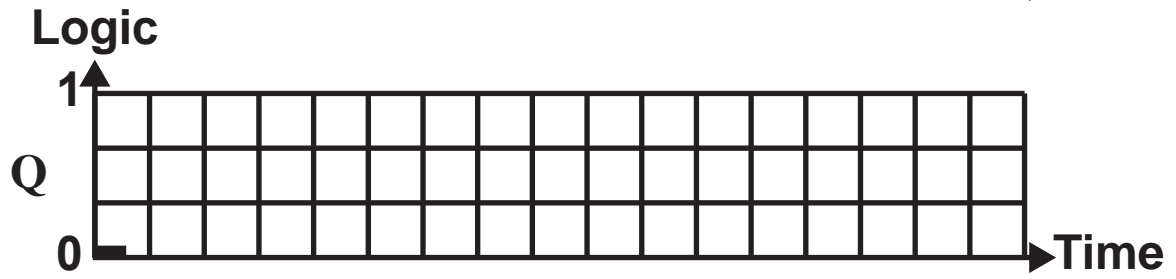
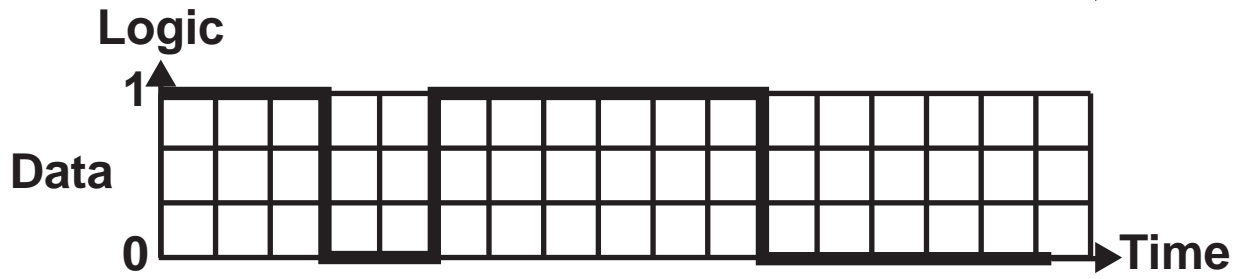
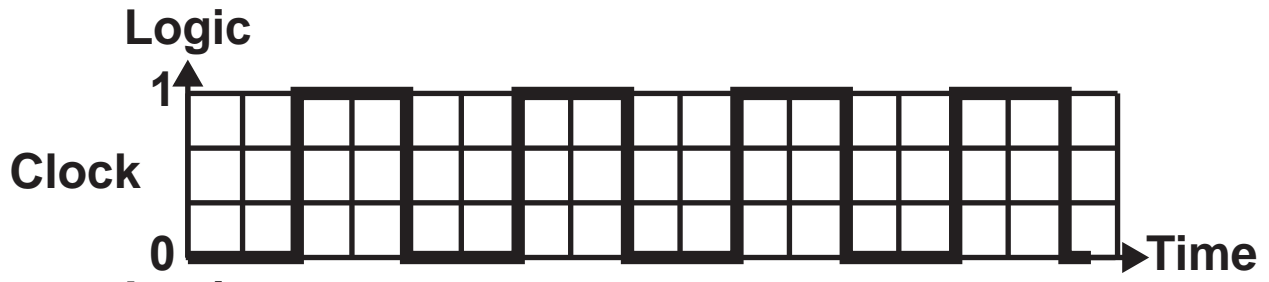
When the clock signal rises from logic 0 to logic 1:

the Q output copies the logic level present on the clock input.

the Q output copies the logic level present on the data input.

the \bar{Q} output copies the logic level present on the clock input.

the \bar{Q} output copies the logic level present on the data input.

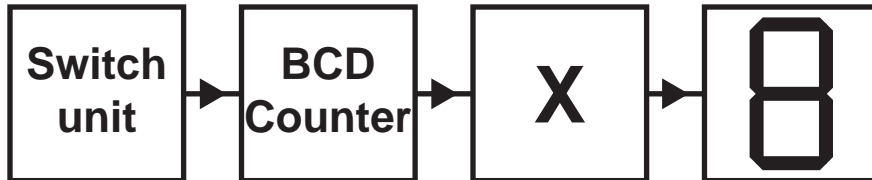


4(b) A rising-edge triggered D-type flip-flop receives the clock and data signals shown in the graphs opposite.

Complete the graphs to show the Q and \bar{Q} outputs. [3]

The Q output starts at logic 0.

5. Here is the block diagram for a single digit decimal counting system.



- (a) Which of the following is the best reason for using a BCD counter for this application? (Tick (✓) the correct answer.) [1]

The system displays only one digit.

It resets automatically on the tenth pulse.

It is the simplest, as it just uses logic 0's and logic 1's.

The system is based on the decimal numbering system.

5(b) Which one of the following sub-systems is the best to use for 'X' in the block diagram on page 12? (Tick (✓) the correct answer.) [1]

Transistor switch

Comparator

Transducer driver

Decoder/driver

6. The boxes on the left give the names of two interface devices.

The boxes on the right give three descriptions.

Draw a line to link each device to its correct description. [2]

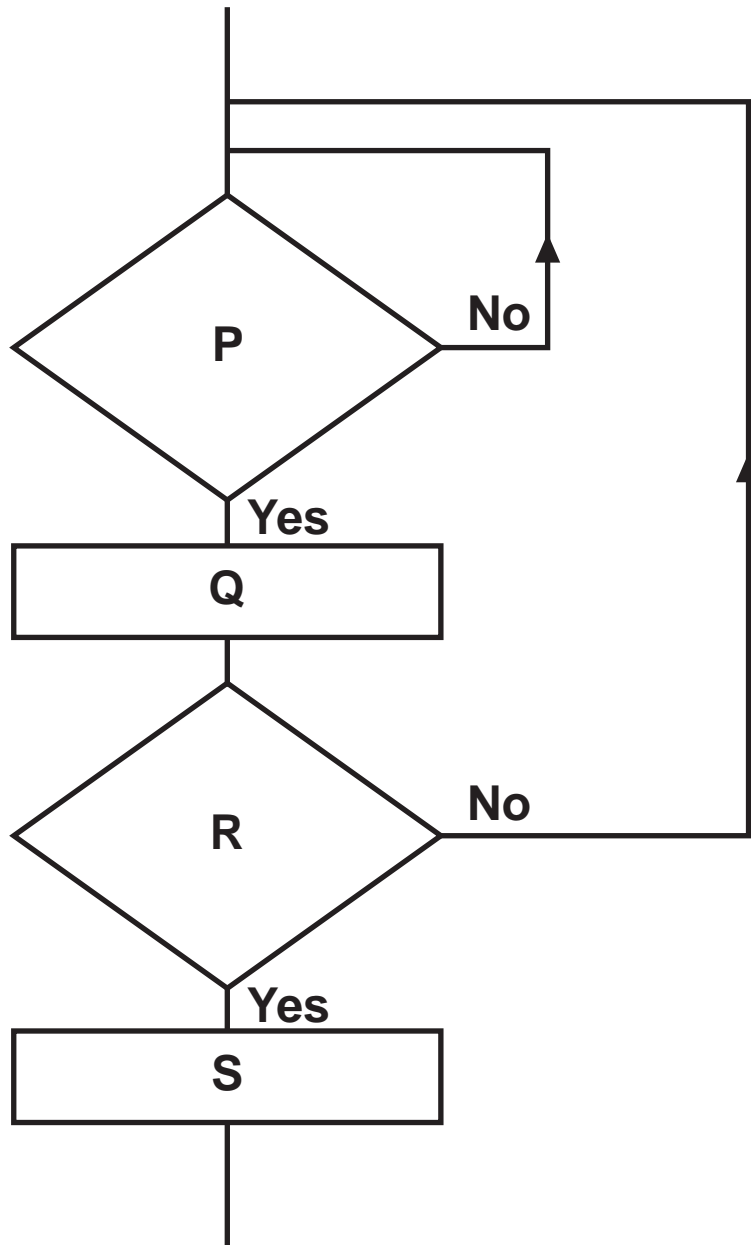
Comparator

Has two fixed switching thresholds

Has one switching threshold which can be changed easily

Schmitt trigger

Has one fixed switching threshold of 0.7 V



This part of the system:

- **waits until a switch is pressed**
- **then it adds 1 to a variable called 'total'**
- **it checks to see if 'total' has reached 12**
- **if it has, it resets the counter**
- **if it has not, it goes back to check the switch again.**

The flowchart contains the following four instructions:

Instruction A Is 'total' = 12?

Instruction B Is the switch pressed?

Instruction C Add 1 to 'total'

Instruction D Reset 'total'.

7. Shown opposite is a flowchart for part of a control system.

(a) Which of these instructions will be found in box P?
(Tick (✓) the correct answer.) [1]

- A
- B
- C
- D

(b) Which of these instructions will be found in box Q?
(Tick (✓) the correct answer.) [1]

- A
- B
- C
- D

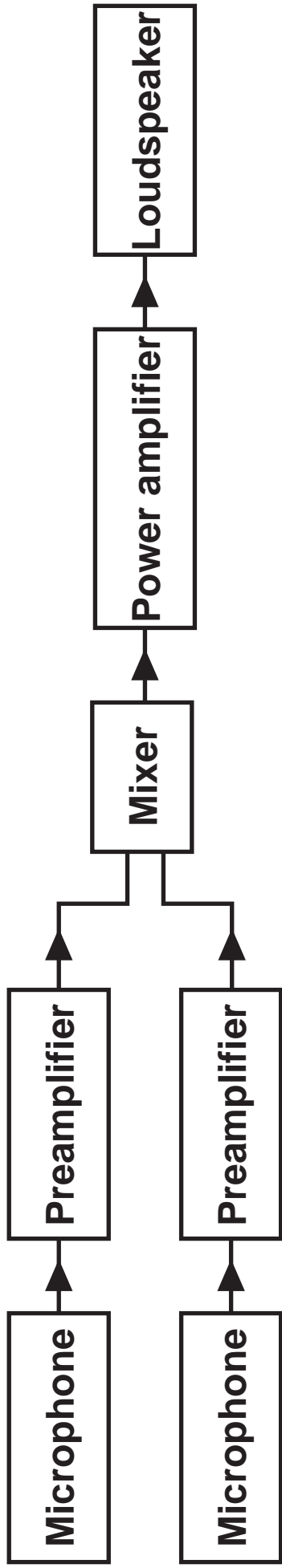
7(c) Which of these instructions will be found in box R?
(Tick (✓) the correct answer.) [1]

A

B

C

D



8. Shown opposite is the block diagram for a simple public address system.

The sub-systems used in this are:

Mixer Loudspeaker Preamplifier
Microphone Power amplifier

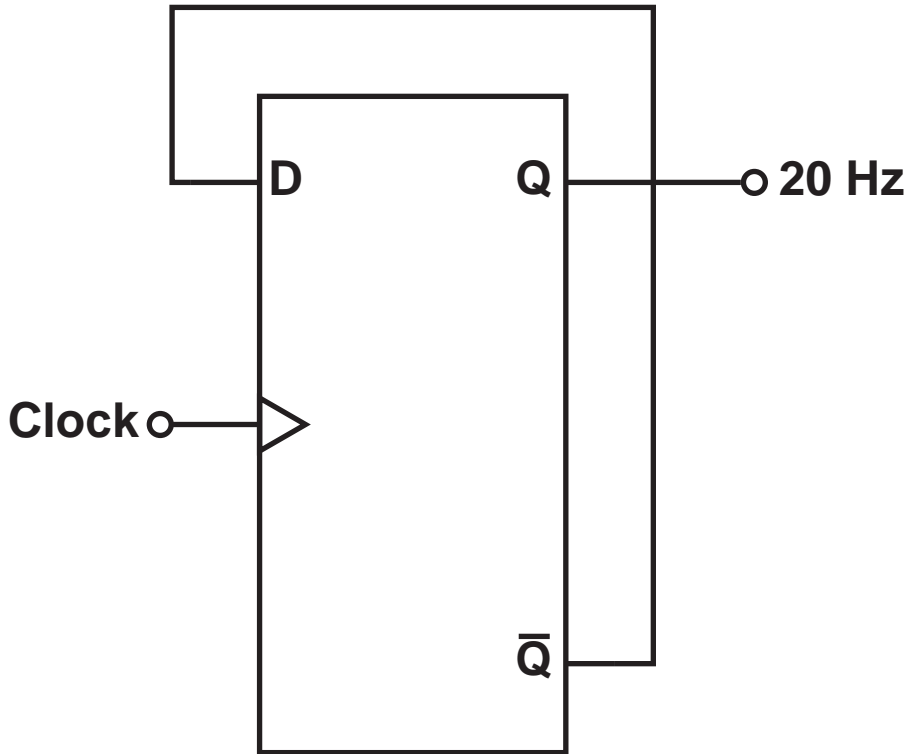
Which sub-system:

- (a) turns sound into electrical signals; [1]
-

- (b) boosts the current; [1]
-

- (c) combines the signal from a number of sources? [1]
-

9. The diagram shows a D-type flip-flop used as a 'divide-by-two' sub-system.

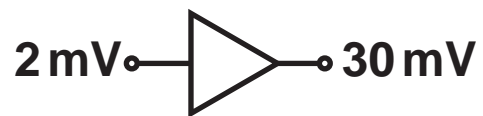


The Q output generates pulses with a frequency of 20 Hz.

What is the frequency of the signals at:

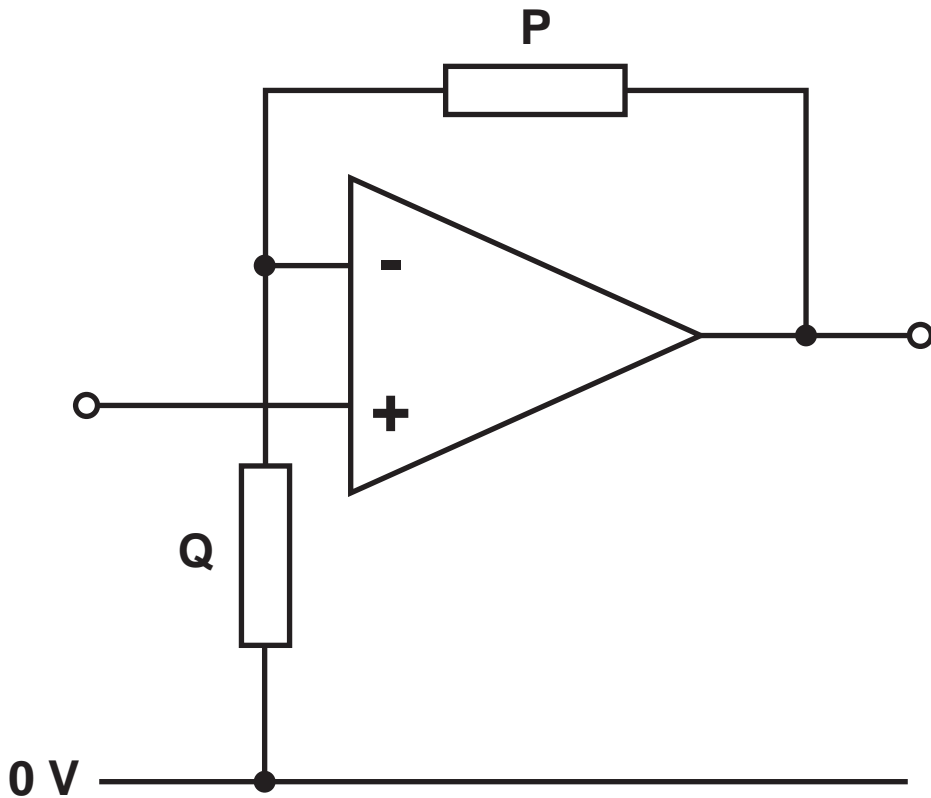
- (a) the clock input _____ Hz; [1]
- (b) the \bar{Q} output _____ Hz? [1]

10(a) What is the voltage gain of the amplifier shown below? [1]



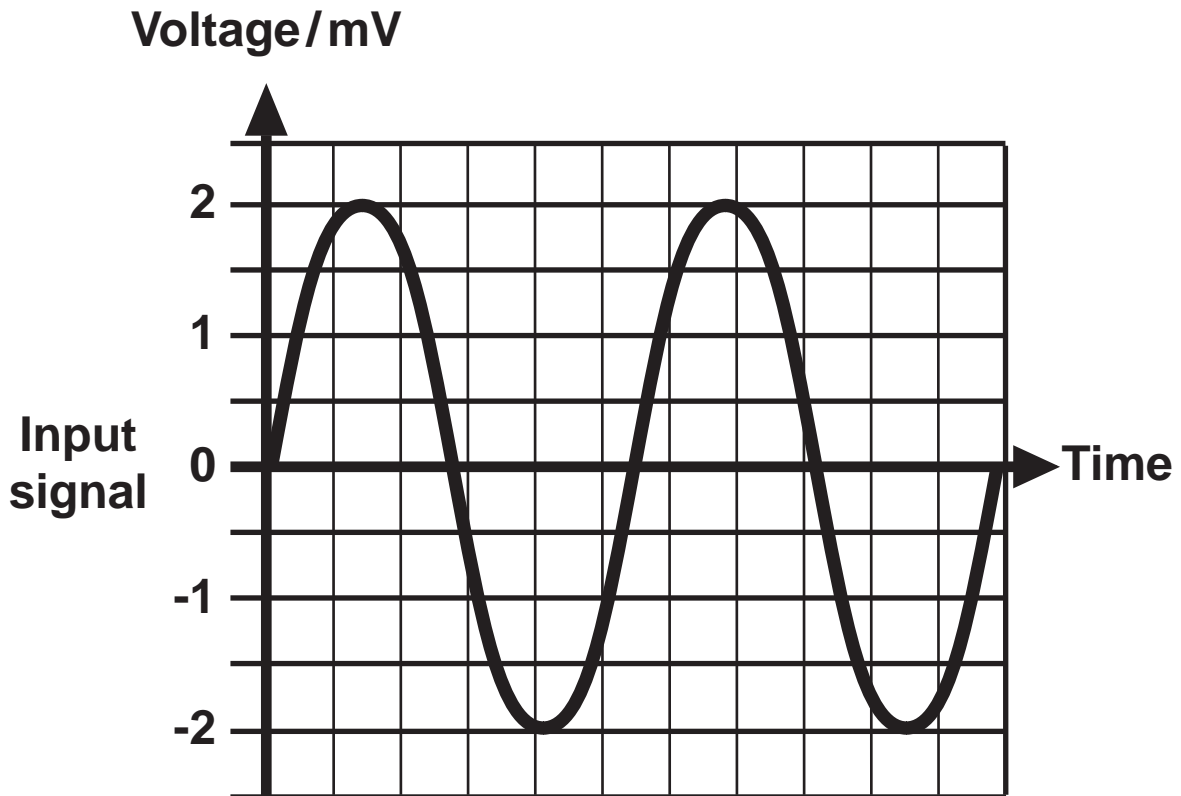
Voltage gain = _____

10(b) Which one of the following options would give the amplifier a voltage gain of 10?
 (Tick (✓) the correct answer.) [1]



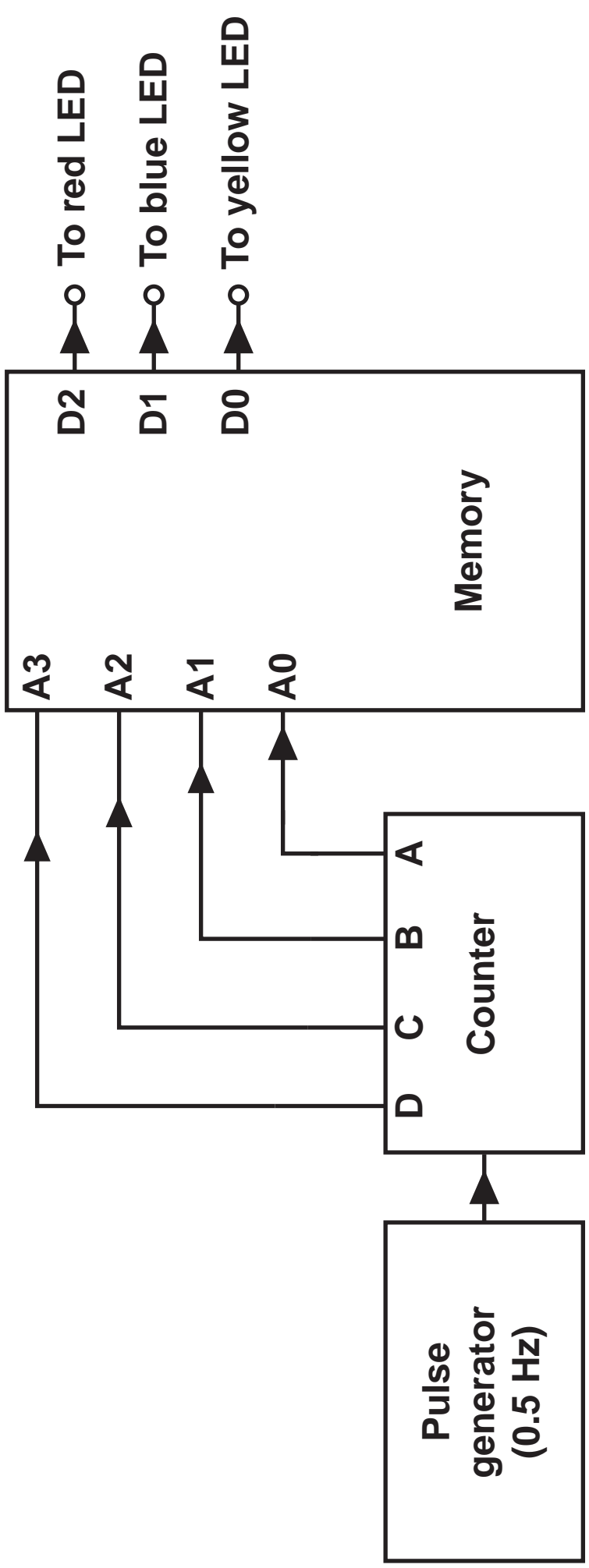
RESISTOR P	RESISTOR Q
9 k Ω	1 k Ω
10 k Ω	1 k Ω
20 k Ω	2 k Ω
22 k Ω	2 k Ω

10(c) The signal shown in the graph is applied to an amplifier having a voltage gain of 20.



What is the amplitude of the output signal? [1]

_____ mV



11. A light sequence controller shown opposite uses a simple memory IC to control a number of LEDs.

The memory IC has four address pins and three data pins.

A logic 1 signal from a memory IC output causes the corresponding LED to light.

- (a) Complete the statement.

The pulse generator has a period of

_____ seconds. [1]

- (b) Complete the statement by circling the correct answer below: [1]

0.25 0.5 2 4 8

The pulses applied to A1 have a period of

_____ seconds.

11(c) Which of the following statements about the memory is true?

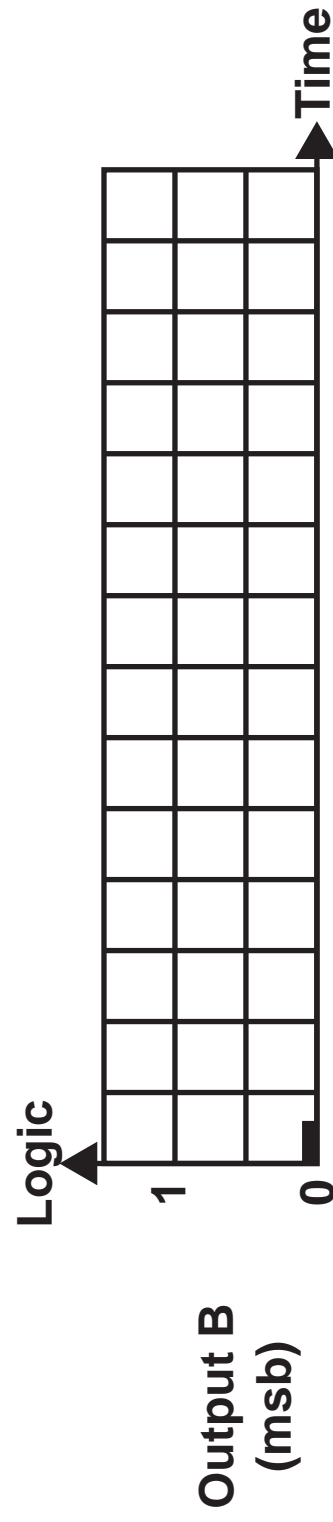
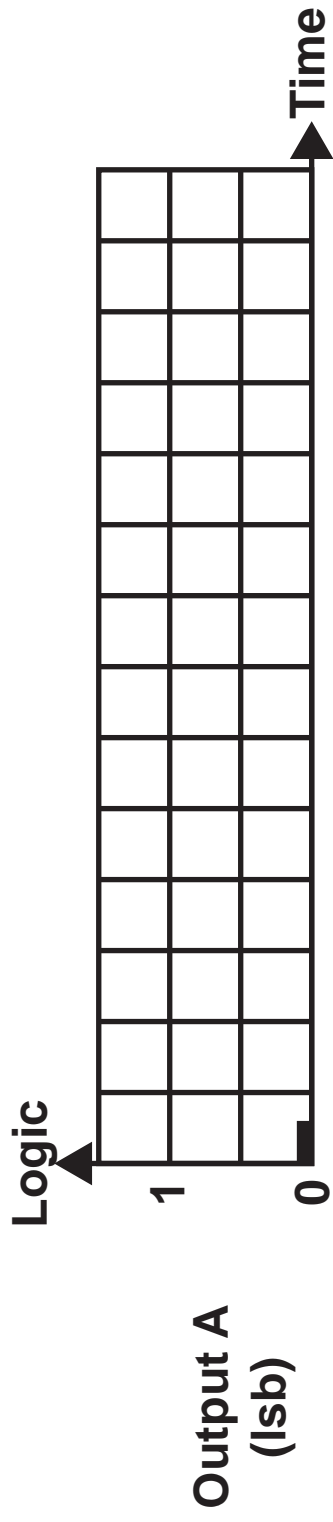
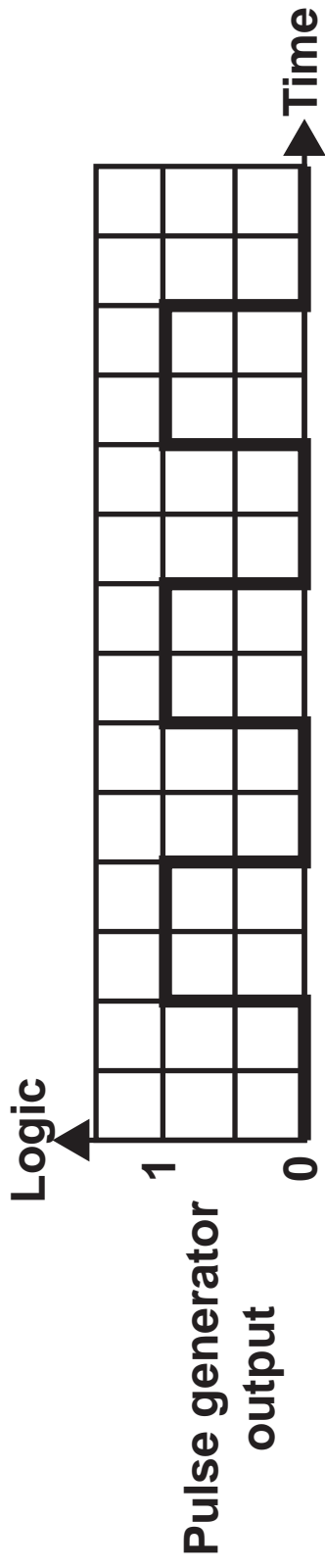
(Tick (✓) the correct answer.) [1]

It has 4 memory locations, each storing a 3 bit-number.

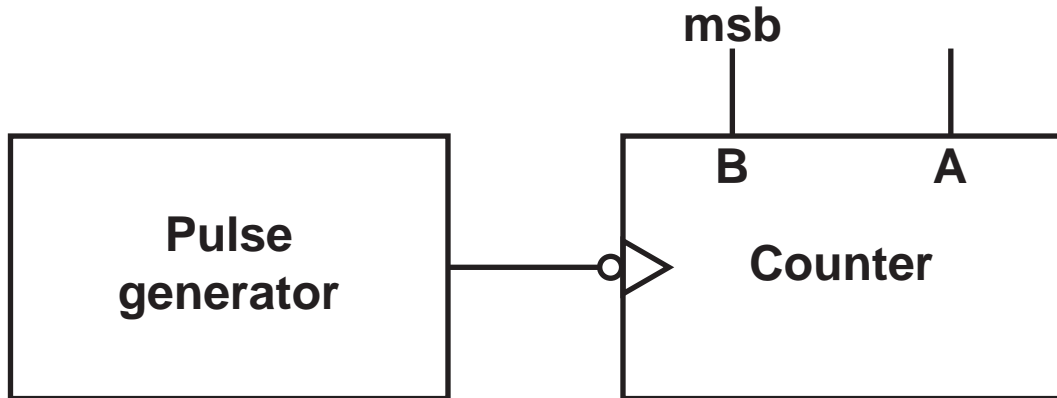
It has 4 memory locations, each storing an 8 bit-number.

It has 16 memory locations, each storing a 3 bit-number.

It has 16 memory locations, each storing an 8 bit-number.



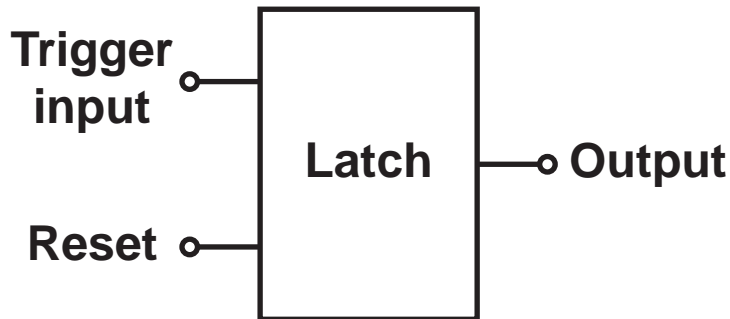
12. The 2-bit counter IC in the following diagram is falling-edge triggered.



Initially the counter is reset.

Use the axes provided opposite to draw the signals produced at counter outputs A and B caused by the pulses from the pulse generator. [3]

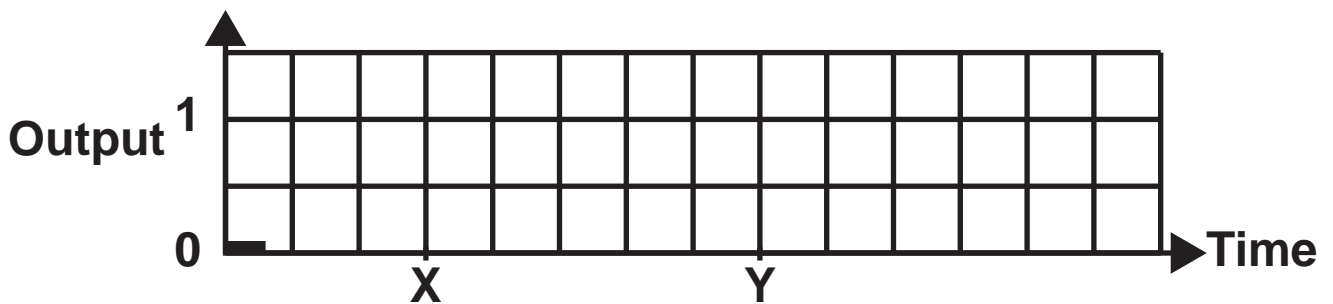
13(a) Here is the block diagram for a latch.

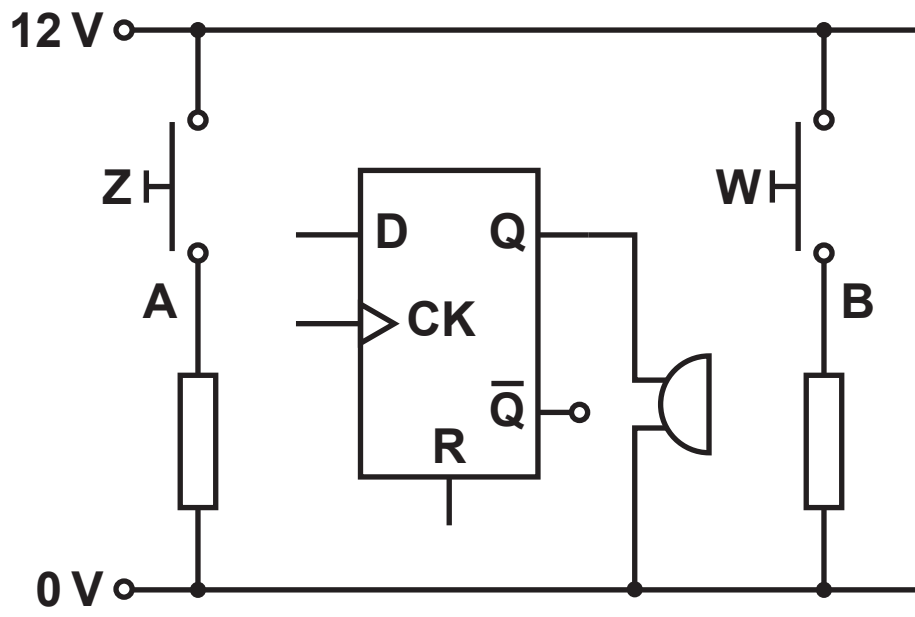


The latch sub-system:

- is initially reset;
- is triggered at time X;
- is reset at time Y.

Complete the timing diagram for the output of the latch. [2]





13(b) The diagram opposite shows the incomplete circuit for a latch based on a rising-edge triggered D-type flip-flop. Switch Z is used to trigger the latch. Switch W is used to reset it. The buzzer sounds when the latch is triggered.

Three connections are needed to complete the circuit:

(Tick (✓) the correct answer.)

(i) A must be connected to: [1]

Data input

Clock input

Reset input

12 V power rail

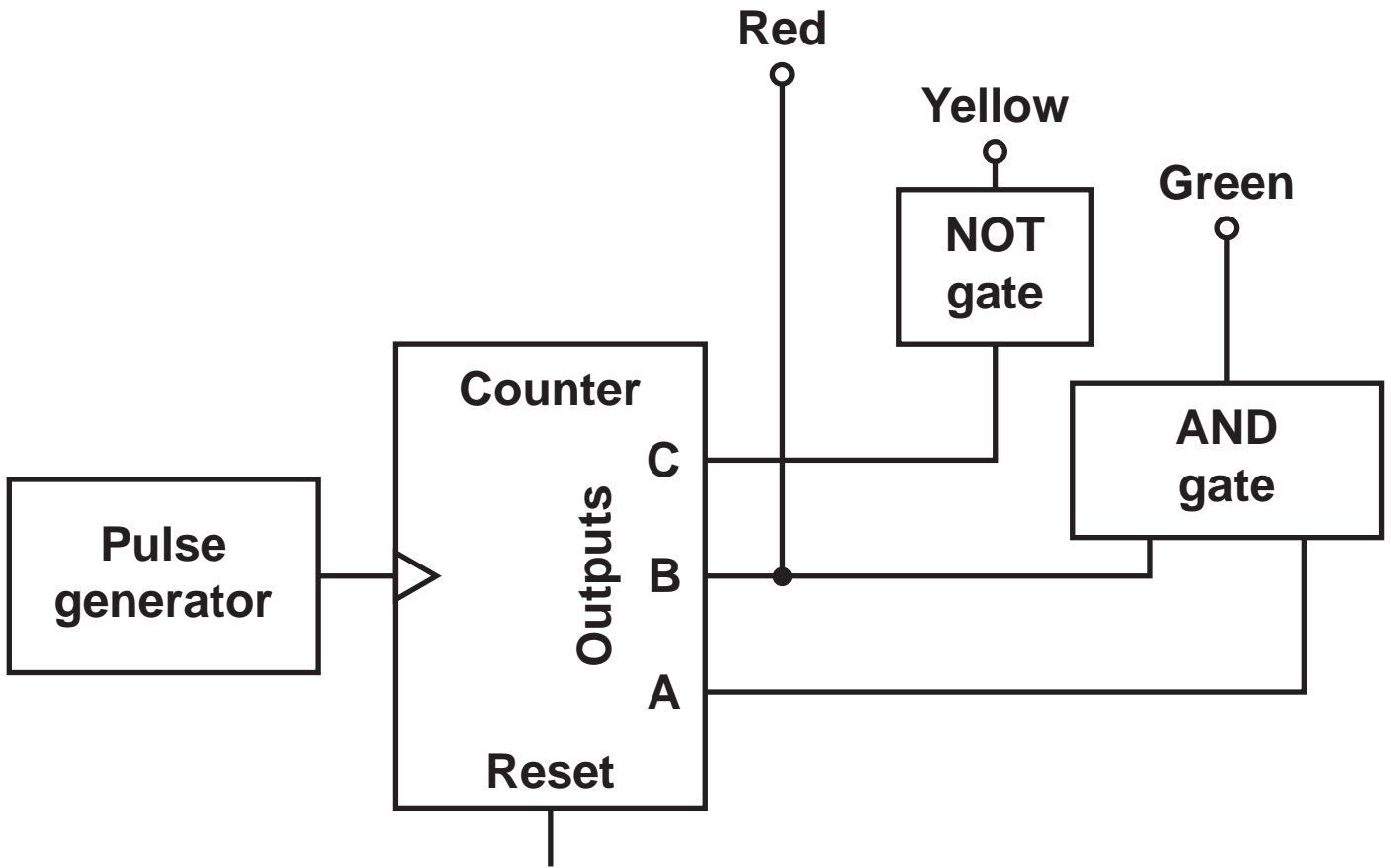
0 V power rail

13(b) (ii) B must be connected to: [1]

Data input	<input type="checkbox"/>
Clock input	<input type="checkbox"/>
Reset input	<input type="checkbox"/>
12 V power rail	<input type="checkbox"/>
0 V power rail	<input type="checkbox"/>

(iii) D must be connected to: [1]

Data input	<input type="checkbox"/>
Clock input	<input type="checkbox"/>
Reset input	<input type="checkbox"/>
12 V power rail	<input type="checkbox"/>
0 V power rail	<input type="checkbox"/>



14. The diagram opposite shows part of a light sequence controller circuit, for three LEDs.

A LED lights when it receives a logic 1 signal.

The incomplete table below describes the counter outputs as more pulses arrive at its input, and the resulting states of the LEDs.

PULSE	COUNTER OUTPUTS			LED		
	C	B	A	RED	YELLOW	GREEN
None	0	0	0	Off	On	Off
1	0	0	1			
2	0	1	0			
3						
4						

**14(a) Which one of the following would make the counter reset on pulse 4?
(Tick (✓) the correct answer.) [1]**

Connect counter output A directly to the Reset input.

Connect counter output B directly to the Reset input.

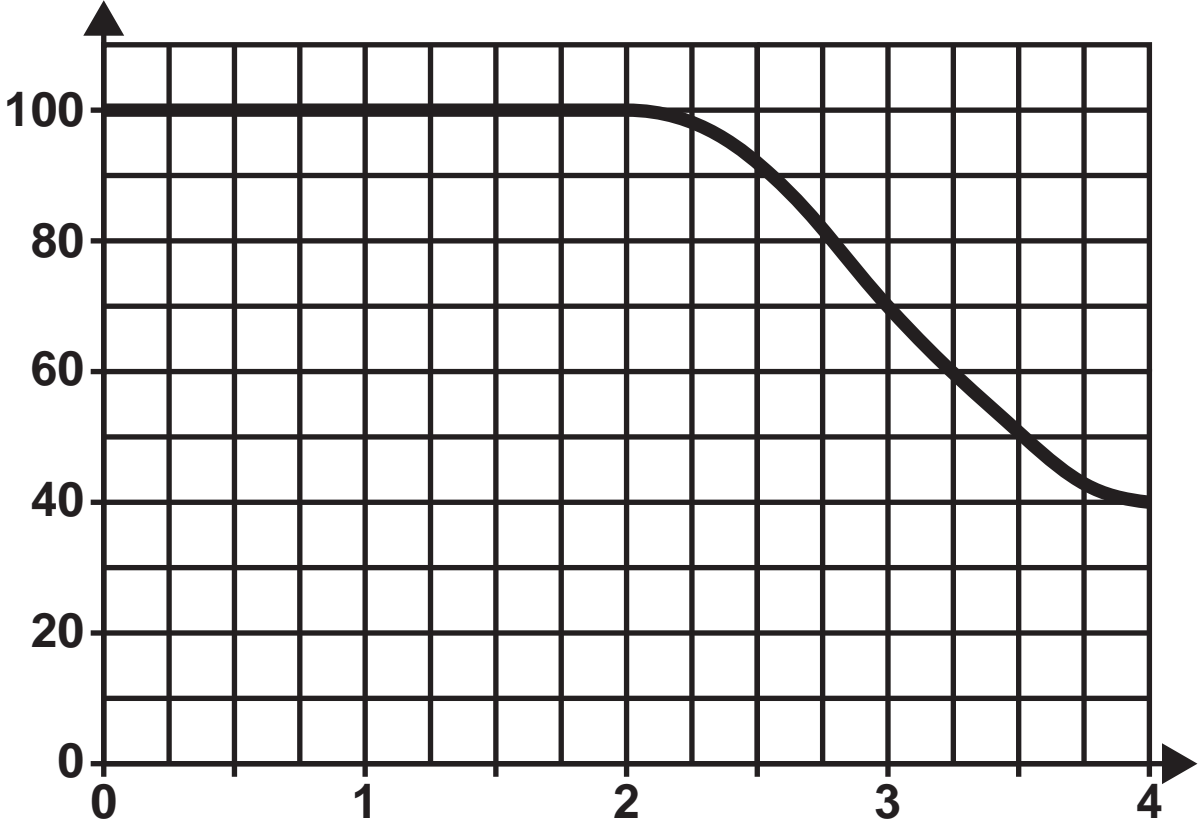
Connect counter output C directly to the Reset input.

Connect counter outputs A and C to the inputs of a 2-input AND gate, with its output connected to the Reset input.

(b) COMPLETE the 'C', 'B', 'A' columns in the table on page 29, by adding a '0' or a '1', to show the counter outputs when pulse 3 has arrived. [1]

(c) COMPLETE the 'Red', 'Yellow' and 'Green' columns in the table on page 29 by adding either 'On' or 'Off' to show the state of each LED for each set of counter outputs. [3]

Voltage gain



Frequency/kHz

15. The graph opposite shows the way in which the voltage gain of an amplifier changes as the frequency of the signal changes.

(a) Use the graph to measure the bandwidth of the amplifier. [1]

Bandwidth = _____ kHz

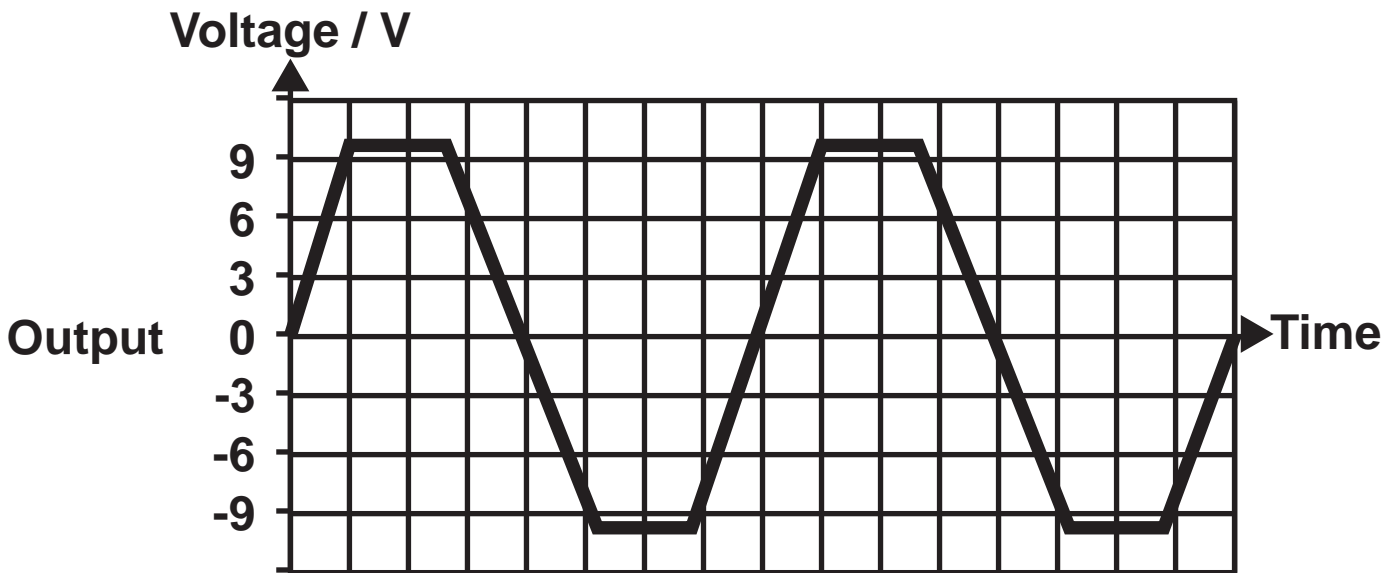
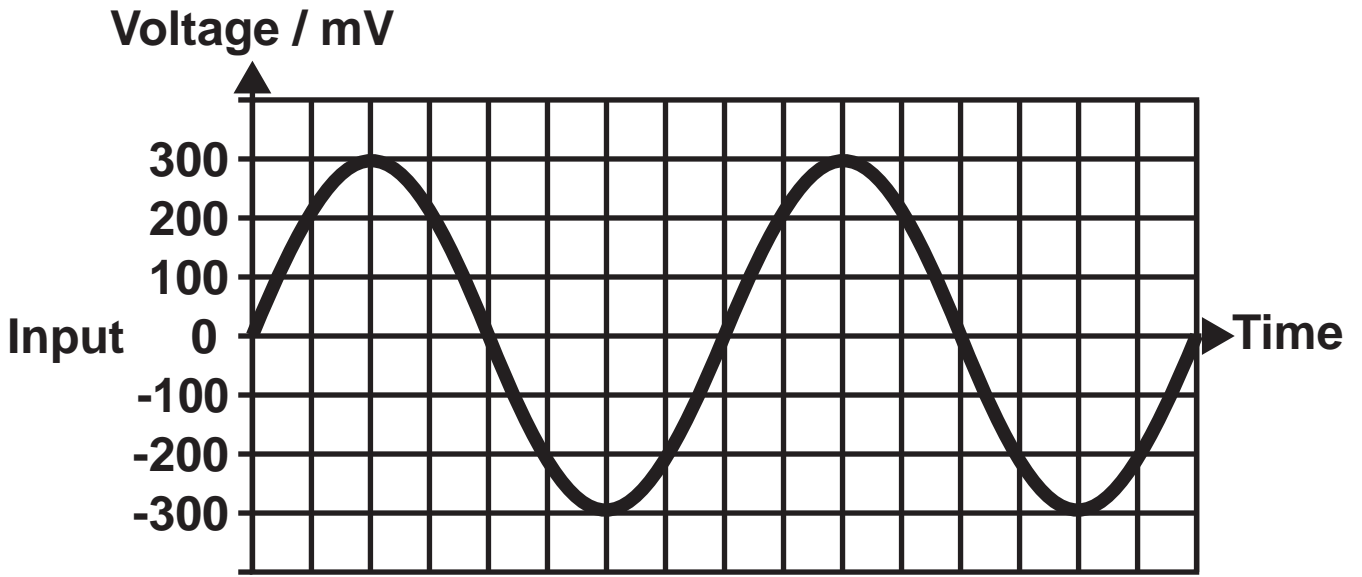
(b) Which one of the following could increase the bandwidth but leave the voltage gain unchanged? (Tick (✓) the correct answer.) [1]

Use a higher power supply voltage.

Increase the amplitude of the input signal.

Combine several amplifiers in a multi-stage amplifier.

Replace the amplifier with a non-inverting voltage amplifier.



16. A non-inverting amplifier has a voltage gain of 40.

The upper graph opposite shows the signal applied to its input.

The lower graph opposite shows the signal produced at its output.

(a) Name the effect illustrated in the graphs. [1]

(b) Which of the following could eliminate this problem?

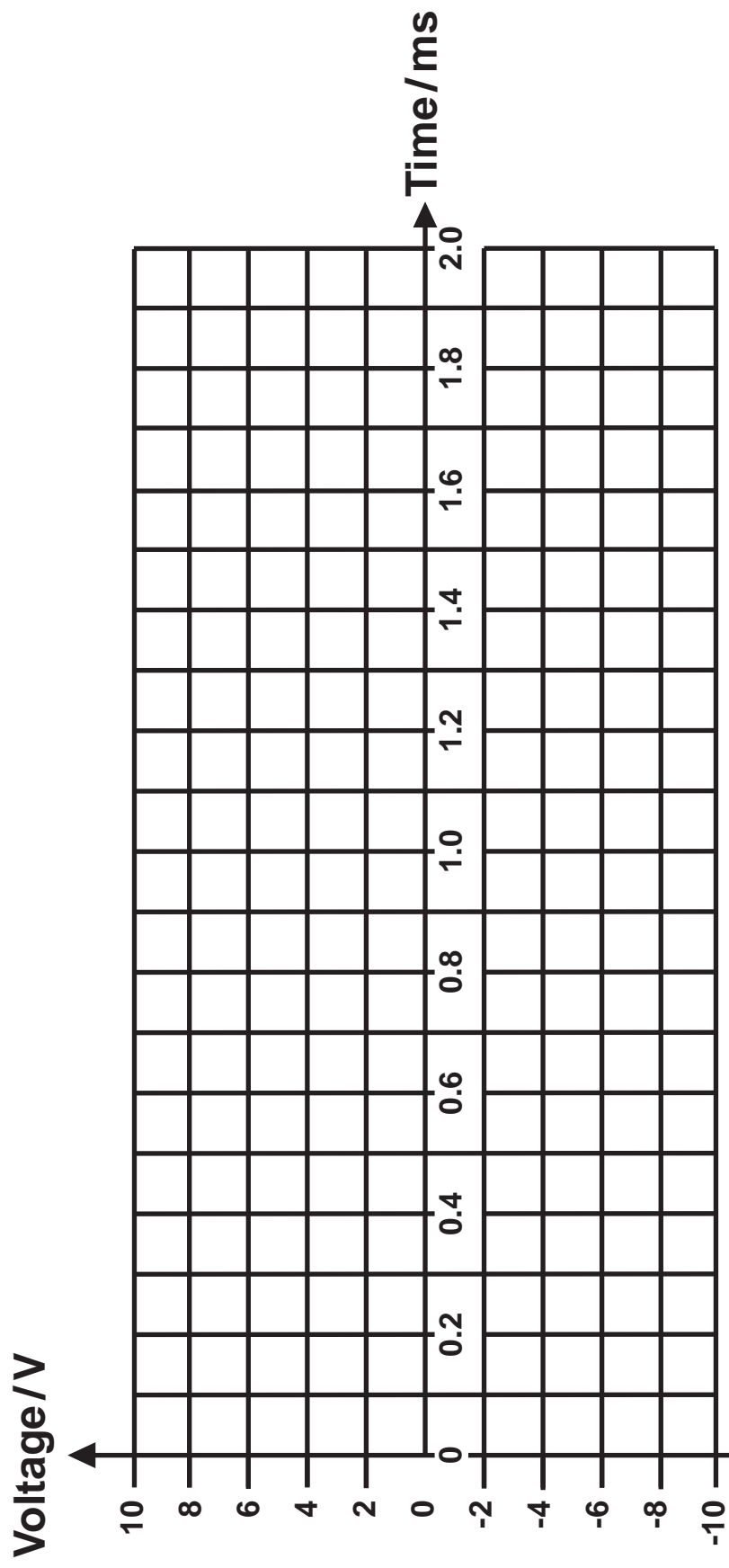
(Tick (✓) the correct answer.) [1]

Reduce the voltage gain of the amplifier.

Increase the voltage gain of the amplifier.

Reduce the bandwidth of the amplifier.

Increase the bandwidth of the amplifier.

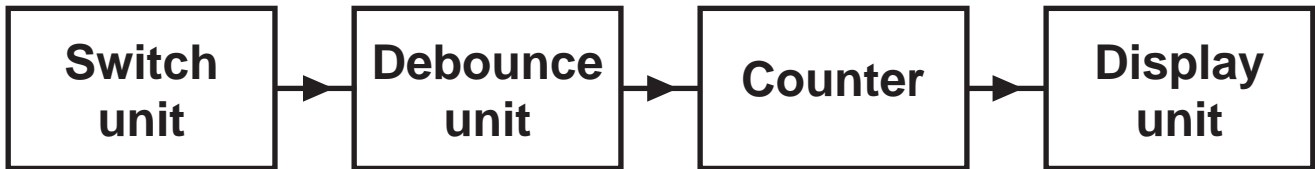


17. An inverting amplifier has a voltage gain of 40.

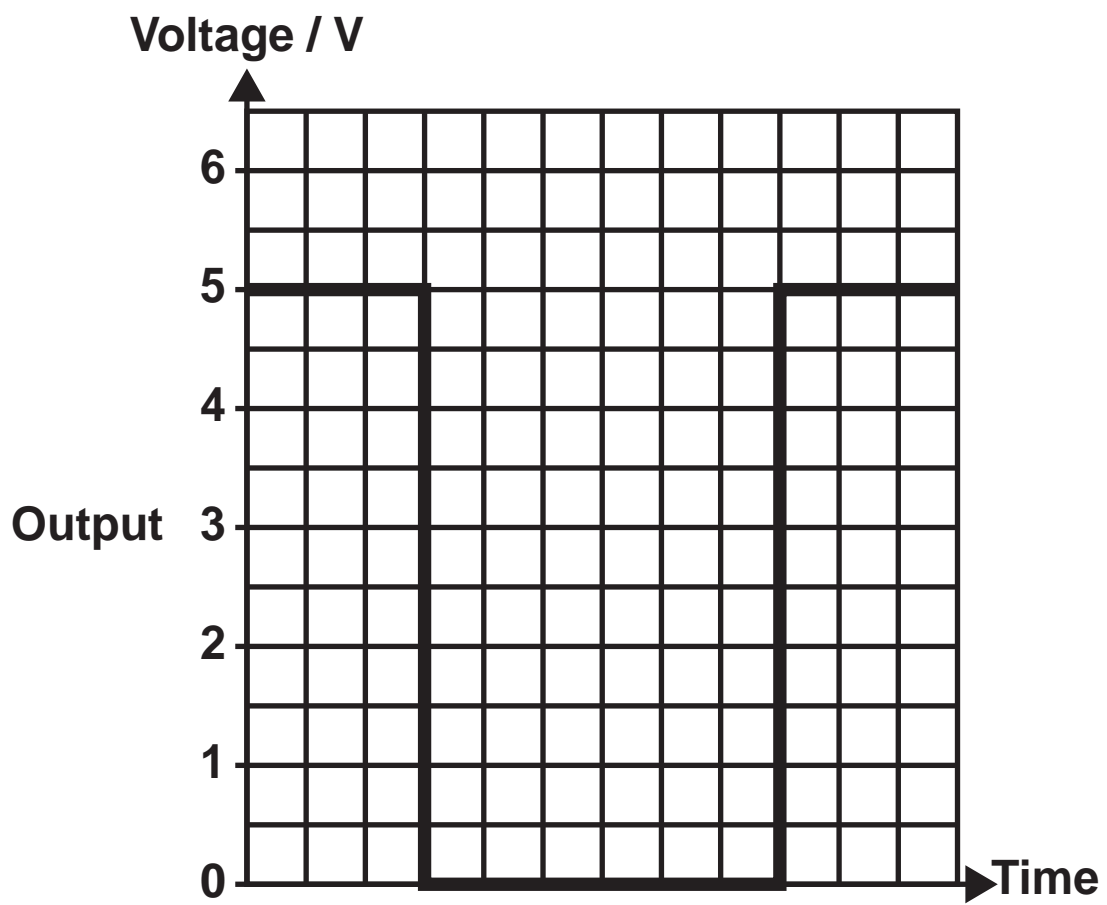
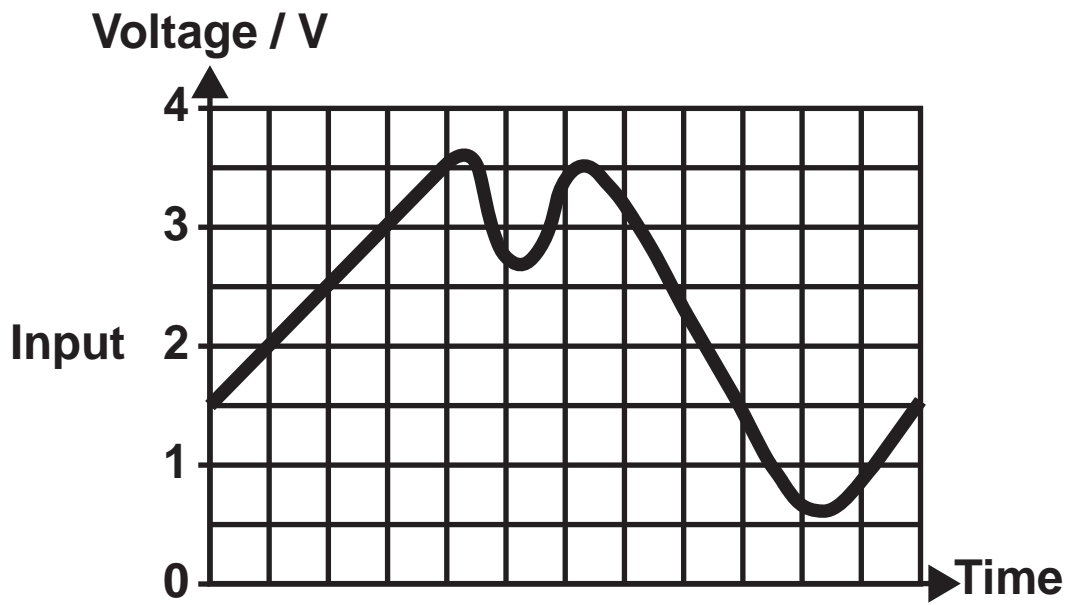
The input signal has an **AMPLITUDE OF 0.2V** and a **PERIOD OF 1 ms**.

Draw the wave on the graph opposite so that it shows the corresponding output signal. [2]

18(a) The block diagram shows a system used to count how many times the switch is pressed.



Explain why it is necessary to debounce the switch. [1]



18(b) The debounce unit contains a Schmitt inverter. The performance of a Schmitt inverter is shown below.

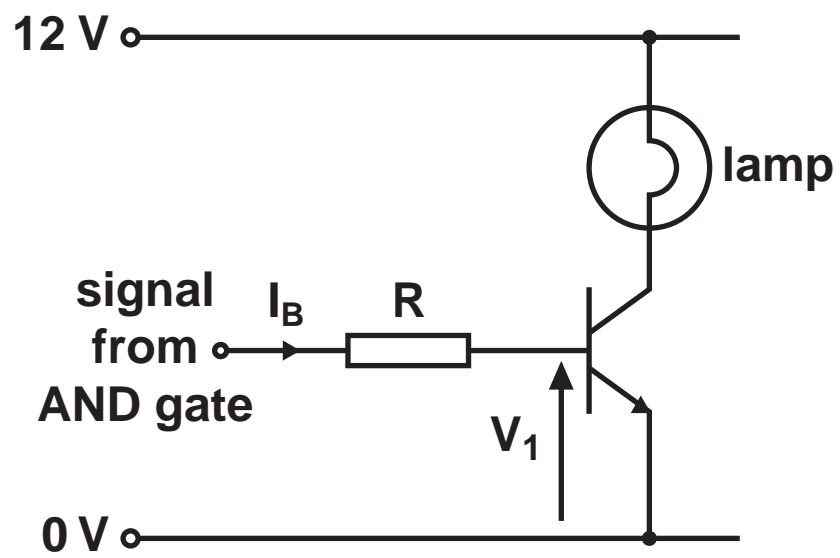
The input signal is shown in the top graph opposite.

The corresponding output signal is shown in the bottom graph opposite.

Complete the following sentences:

(i) The output of the Schmitt inverter changes from logic 1 to logic 0 when a rising input voltage reaches _____ V. [1]

(ii) The output of the Schmitt inverter changes from logic 0 to logic 1 when a falling input voltage reaches _____ V. [1]



19. The circuit diagram for an interface and lamp unit is shown opposite.

(a) The signal from the logic gate switches from 0.5V (logic 0) to 7.7V (logic 1).

Complete the table below by:

- (i) adding the correct voltages to the V_1 column; [2]
- (ii) writing either 'On' or 'Off' to show the state of the lamp. [1]

OUTPUT OF AND GATE	V_1	STATE OF LAMP
0.5V	V	
7.7V	V	

19(b) The bulb in the lamp unit is rated at 12 V, 100 mA.

The transistor has a current gain (h_{FE}) of 50.

Calculate the base current, I_B , when the transistor is just saturated. [1]

Base current = _____ mA

19(c) The logic gate outputs 7.7 V. The transistor is just saturated.

What is the voltage drop across resistor R? [1]

Voltage drop = _____ V

19(d) Hence calculate the value of resistor R. [1]

Resistor R = _____ k Ω

END OF PAPER

INFORMATION SHEET FOR UNIT E2

This information may be of use in answering the questions.

1 RESISTOR COLOUR CODES

BLACK	0	GREEN	5
BROWN	1	BLUE	6
RED	2	VIOLET	7
ORANGE	3	GREY	8
YELLOW	4	WHITE	9

The fourth band colour gives the tolerance as follows:

GOLD $\pm 5\%$

SILVER $\pm 10\%$

2 PREFERRED VALUES FOR RESISTORS – E24 SERIES

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

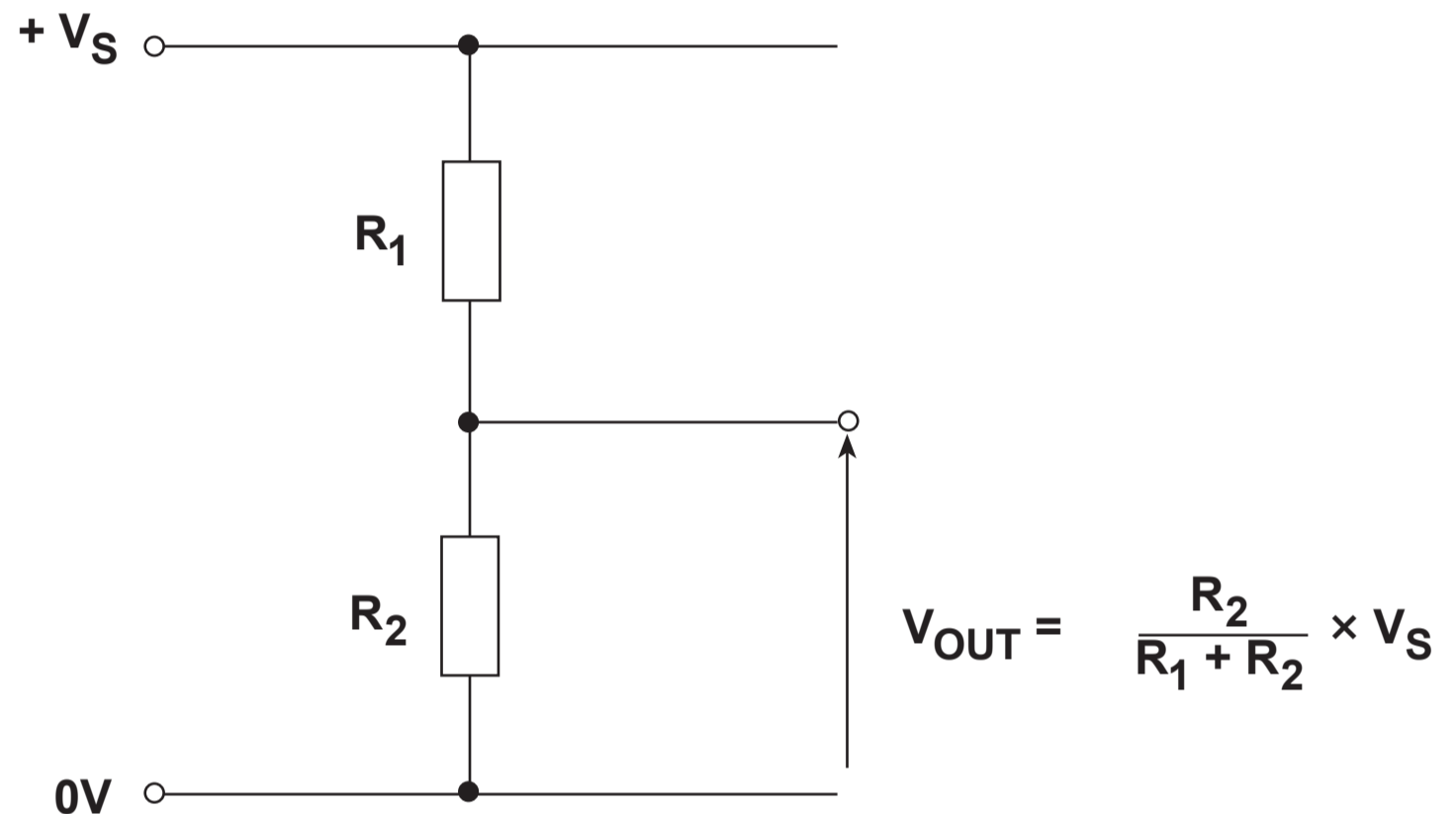
3 **RESISTANCE** = $\frac{\text{voltage}}{\text{current}}$; $R = \frac{V}{I}$

4 **EFFECTIVE RESISTANCE, R**, of two resistors R_1 and R_2 in series is given by $R = R_1 + R_2$.

5 EFFECTIVE RESISTANCE, R , of two resistors R_1 and R_2 in parallel is given by

$$R = \frac{R_1 R_2}{R_1 + R_2}$$

6 VOLTAGE DIVIDER



7 POWER = voltage \times current; $P = VI = I^2 R = \frac{V^2}{R}$

8 LED The forward voltage drop across a LED is 2 V.

9 NPN TRANSISTORS

(i) Current gain = $\frac{\text{Collector current}}{\text{Base current}}$; $h_{FE} = \frac{I_C}{I_B}$.

(ii) The forward voltage drop across the base emitter junction is 0.7 V.

10. AMPLIFIERS

Voltage gain: $A = \frac{V_{OUT}}{V_{IN}}$

Non-inverting amplifier: $A = 1 + \frac{R_F}{R_1}$

Inverting amplifier: $A = - \frac{R_F}{R_{IN}}$

Summing amplifier: $V_{OUT} = - R_F \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \dots \right)$