Candidate Name	Centre Number	Candidate Number

WELSH JOINT EDUCATION COMMITTEE

General Certificate of Secondary Education

CYD-BWYLLGOR ADDYSG CYMRU

Tystysgrif Gyffredinol Addysg Uwchradd

294/02

ELECTRONICS

MODULE TEST E2

HIGHER TIER

A.M. THURSDAY, 7 June 2007

(45 minutes)

For Examiner's use only

Total Mark	

ADDITIONAL MATERIALS

In addition to this examination paper you may need a calculator.

INSTRUCTIONS TO CANDIDATES

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** the questions in the spaces provided in this booklet.

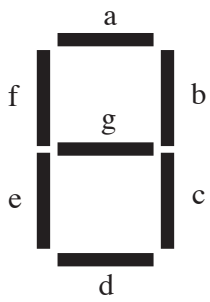
INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.

No certificate will be awarded to a candidate detected in any unfair practice during the examination.

Answer **all** *questions.*

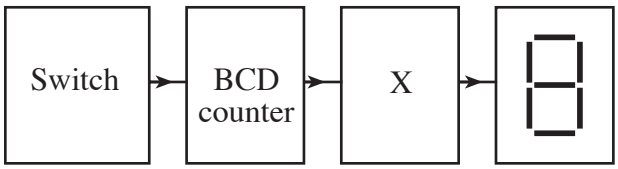
1. *(a)* The diagram shows the arrangement of the LEDs in a seven-segment display.



Complete the following table to show the number displayed when different segments are lit. [3]

SEGMENTS							NUMBER DISPLAYED
a	b	c	d	e	f	g	
1					0		**7**
							9
1	1	1	1	0	0	1	

(b) Here is the block diagram for a counting system. The system shows how many times the switch has been pressed.



(i) What does BCD stand for? [1]

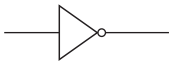
.....

(ii) The table shows the output of the BCD counter after the switch has been pressed a number of times.

Complete the table. [2]

Number of times debounced switch has been pressed	Counter Outputs			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9				
10				

2. *(a)* (i) Which logic gate has the following symbol?



Answer ..... [1]

(ii) Which logic gate has the following truth table?

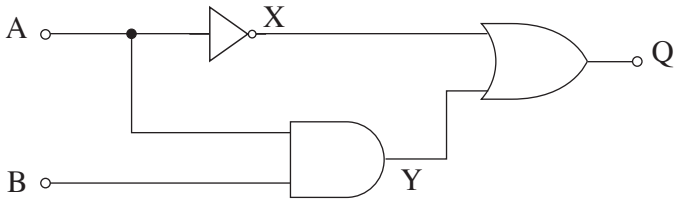
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

Answer ..... [1]

(iii) Which logic gate outputs logic 0 **only** when both inputs are logic 0?

Answer ..... [1]

(b) (i) Complete the truth table for the following logic system. [3]

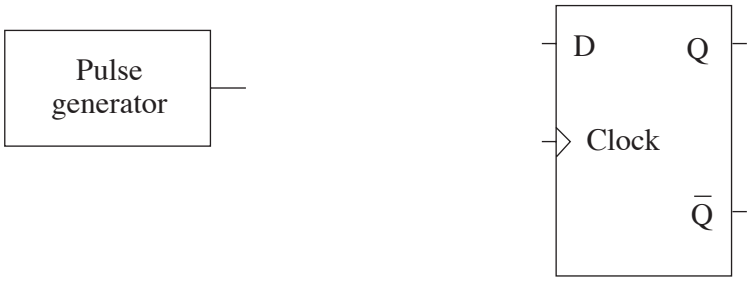


A	**B**	**X**	**Y**	**Q**
0	0			
0	1			
1	0			
1	1			

(ii) Redraw the system replacing each of the three gates with its equivalent NAND gate arrangement. [3]

(iii) **Draw a line** through each redundant gate. [1]

3. The diagram shows a pulse generator and a D-type flip-flop.



(a) Draw the two connections needed to make the D-type perform a divide-by-two action. [2]

(b) The frequency of the signal at the Q output is 100 Hz.

(i) What is the frequency of the $\overline{Q}$ output? .....

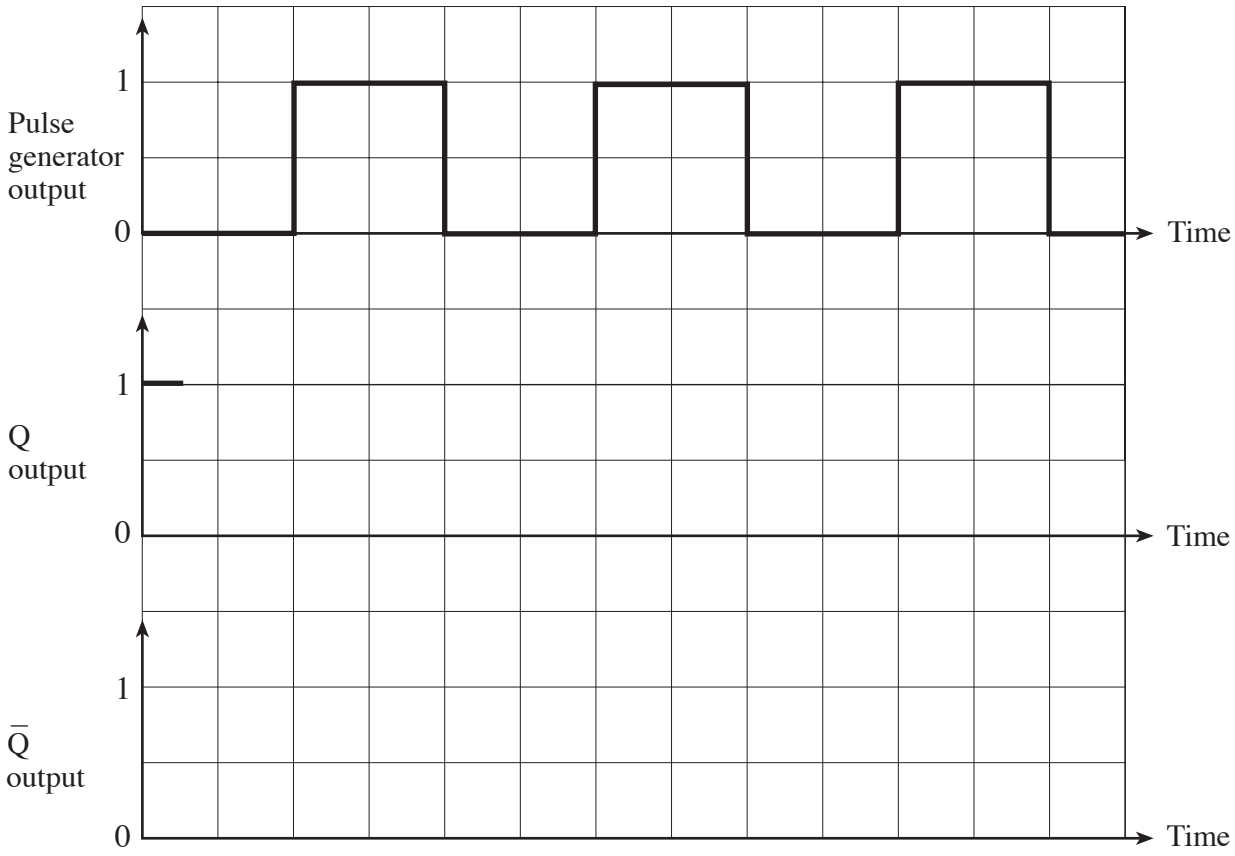
(ii) What is the frequency of the pulse generator output? ..... [2]

(c) The D-type flip-flop is rising-edge triggered.

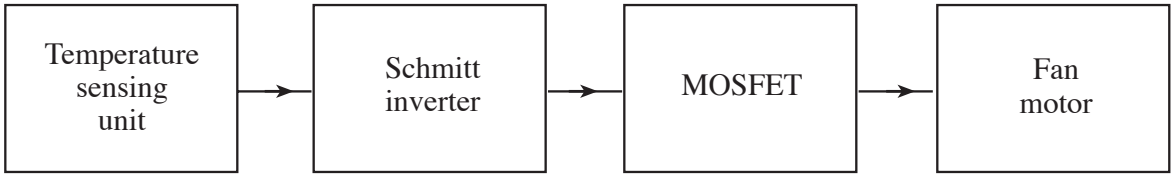
(i) Label a rising-edge on the pulse generator output graph. [1]

(ii) The Q output is initially at logic 1.
Complete the graph to show the signal at the Q output. [2]

(iii) Draw the graph to show the signal at the $\overline{Q}$ output. [1]



4. The block diagram shows the control system for an automatic fan, which switches on when the room gets too hot.

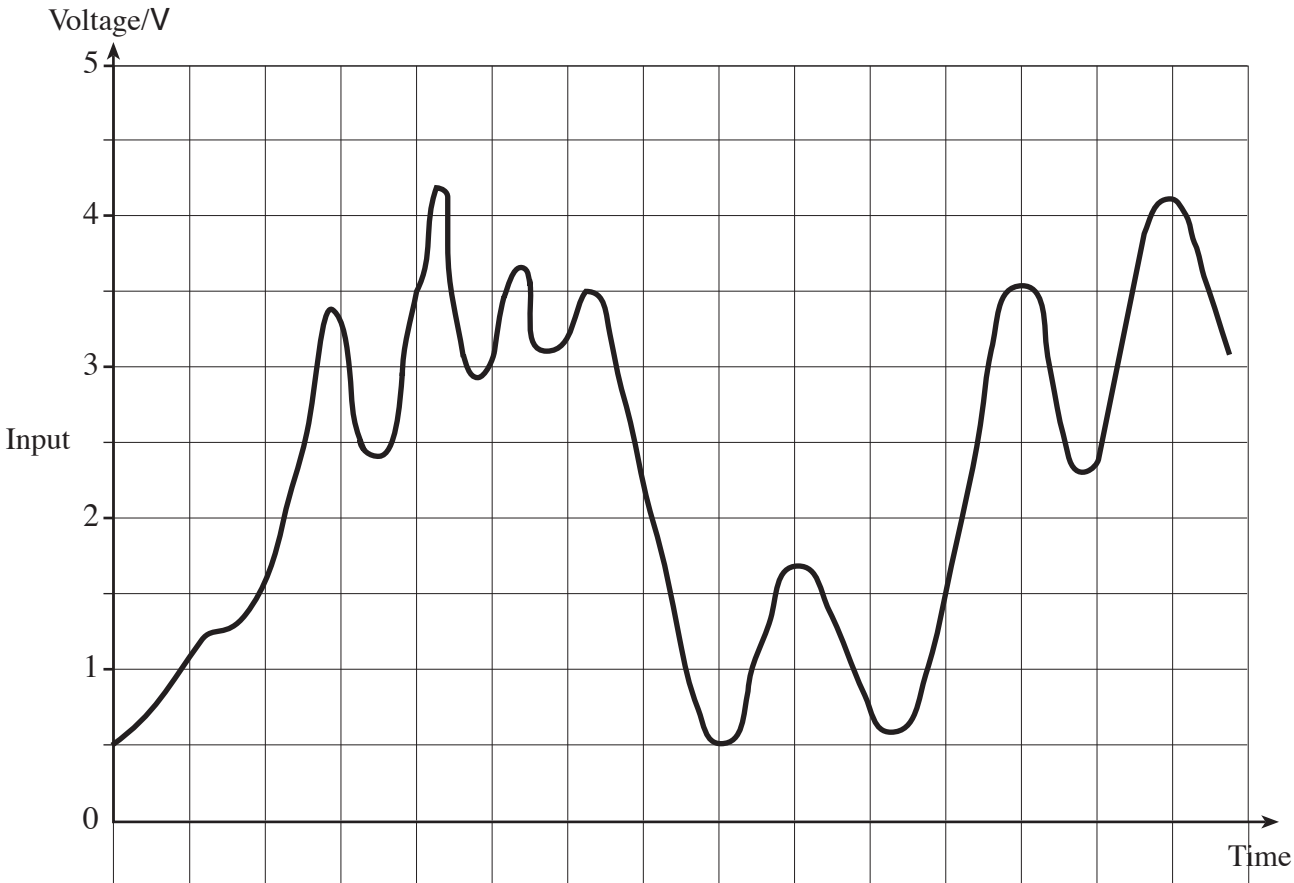


Here is part of the data sheet for the Schmitt inverter:

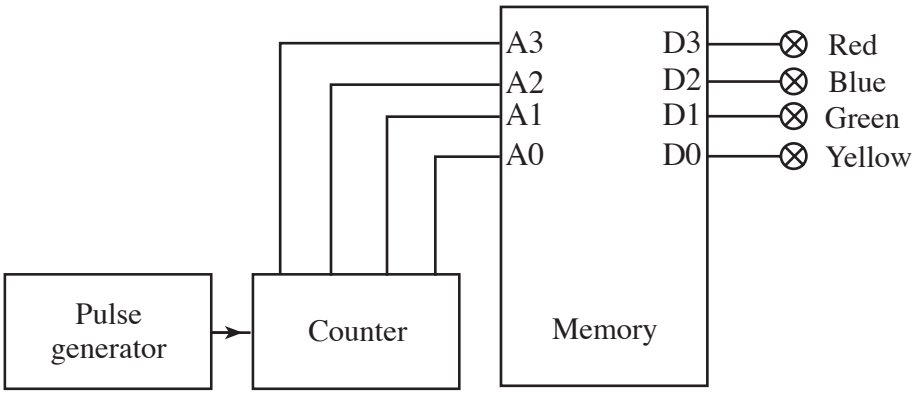
When connected to a 5V power supply:	Output changes from logic 1 to logic 0 when a rising input voltage reaches 3V.
	Output changes from logic 0 to logic 1 when a falling input voltage reaches 1V.
	Logic 1 = 5V
	Logic 0 = 0V

The signal from the temperature sensing unit is shown below.

Use the axes provided to draw the corresponding output signal from the Schmitt inverter. [4]



5. The next block diagram shows a system which repeatedly generates a sequence of disco lights. It uses a memory IC to store the sequence.
The pulse generator and counter select each memory location in turn.



The memory stores the following data:

Address				Data			
A3	**A2**	**A1**	**A0**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0
0	0	1	0	1	1	0	0
0	0	1	1	1	1	1	0
0	1	0	0	1	1	1	1
0	1	0	1	Reset			

(a) Complete the following table by adding either ***Off*** or ***On*** to show the sequence of lights produced by the system. [2]

Red	**Blue**	**Green**	**Yellow**
Off			

(b) The circuit for the pulse generator uses a 555 timer. The frequency of the pulses is controlled by a resistor R and a capacitor C with the following values:

Resistor R = 100 kΩ, Capacitor C = 10 μF

The approximate value of the frequency f, in Hz, of the pulse generator is given by the formula:

$$f = \frac{0{\cdot}7}{RC}$$

where R is in MΩ and C is in μF.

Use this formula to calculate the frequency of the pulse generator. [3]

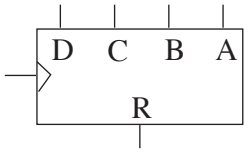
.....

.....

.....

(c) For how many seconds is the yellow LED lit, in the sequence? ..... [1]

(d) The counter resets when the reset pin receives a logic 1 signal.
Output A is the least significant bit of the counter output.
Complete the following circuit diagram by adding a logic gate and the connections necessary to make the counter reset when the counter output reaches 0101. [3]



(e) The red, blue, green and yellow lamps are rated at 9V, 3A.

(i) Choose a suitable device to interface one of these lamps to the memory chip.

..... [1]

(ii) Complete the circuit diagram to show how this interface connects the yellow lamp to the D0 output of the memory chip. [2]