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General Certificate of Secondary Education
June 2013

Electronics 44301

(Specification 4430)

Unit 1: Written Paper

Final

Mark Scheme

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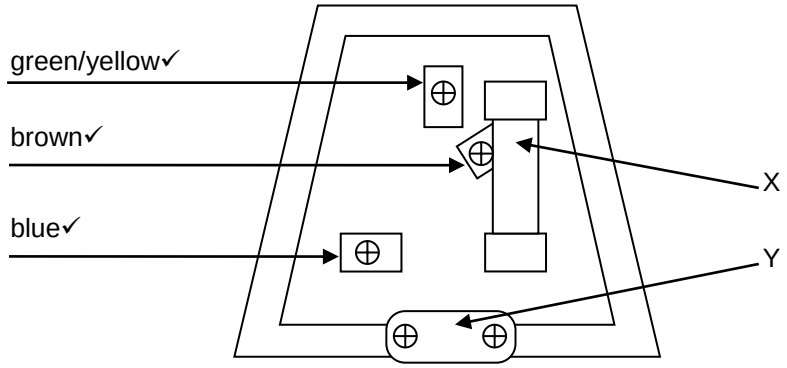
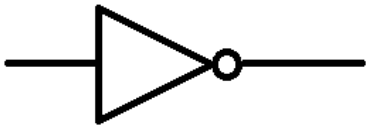
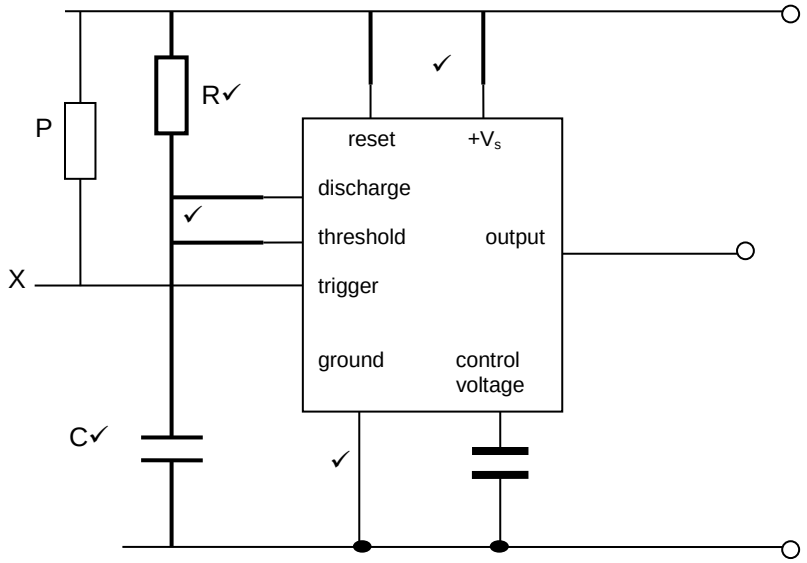
Question	Part	Sub	Marking guidance		Mark
1	(a)	(i)	neutral✓ live✓ earth✓		**3**
1	(a)	(ii)			**3**
1	(a)	(iii)	Fuse✓		**1**
1	(a)	(iv)	It stops any strain on the cable pulling wires out✓		**1**
1	(b)	(i)	Transformer/ step-down or isolating transformer✓		**1**
1	(b)	(ii)	diode/bridge rectifier/rectifier✓		**1**
2	(a)	(i)	temperature sensor✓		**1**
2	(a)	(ii)	display✓		**1**
2	(a)	(iii)	memory✓		**1**
2	(a)	(iv)	ADC✓		**1**
2	(b)	(i)	temperature sensor✓		**1**

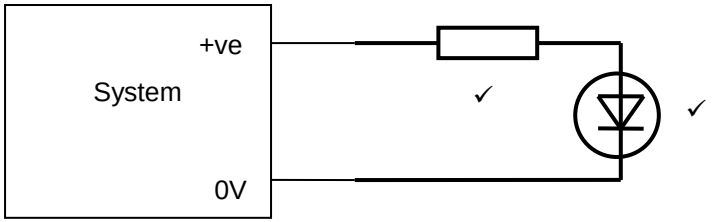
2	(b)	(ii)	display✓		**1**
2	(b)	(iii)	ADC✓		**1**
2	(b)	(iv)	memory✓		**1**
2	(c)	(i)	temperature sensor✓		**1**
2	(c)	(ii)	memory✓		**1**
3	(a)		<table><tr><th>Sensor A</th><th>Input Valve C</th><th>Sensor B</th><th>Output valve D</th></tr><tr><td>0</td><td>1 ✓</td><td>0</td><td>0 ✓</td></tr><tr><td>1</td><td>0 ✓</td><td>1</td><td>1 ✓</td></tr></table>		**4**
3	(b)		Valve C will be closed ✓ Valve D will be open ✓		**2**
3	(c)		NOT gate ✓		**1**
3	(d)		 ✓ ✓ or ecf. from (c) (symbol ✓)		**3**
4	(a)	(i)	monostable✓		**1**

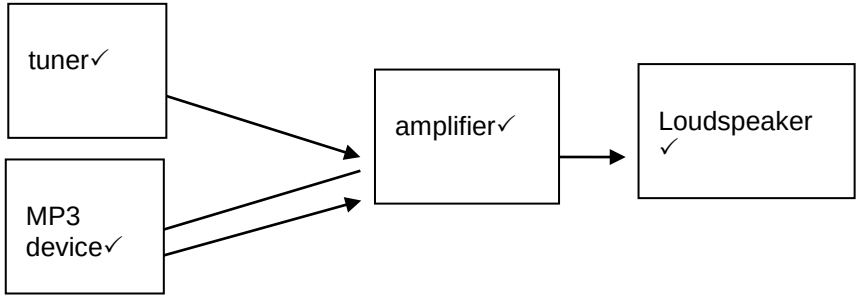
4	(a)	(ii)			**5**

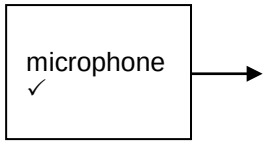
4	(a)	(iii)	P is a pull-up resistor✓		**1**

4	(a)	(iv)	The signal at X must go low ✓ (below one-third of the supply)		**1**

4	(b)		Use T = 1.1 RC, so C = T/1.1 R✓ C = 10/1.1 x 3 x 10^5✓ C = 30.3 µF✓		**3**

5	(a)	(i)			**2**
5	(a)	(ii)	it limits the current✓		**1**
5	(b)	(i)	8 – 2.4 = 5.6V✓		**1**
5	(b)	(ii)	5.6 / 0.3✓ = 18.66Ω✓ or ecf.		**2**
5	(b)	(iii)	20Ω✓ ecf.		**1**
5	(b)	(iv)	5.6 x 0.3 = 1.68W✓ ecf.		**1**
5	(b)	(v)	20✓R✓J✓ ecf.		**3**

6	(a)	(i)	Minus 1 for lines not arrows.  		**4**

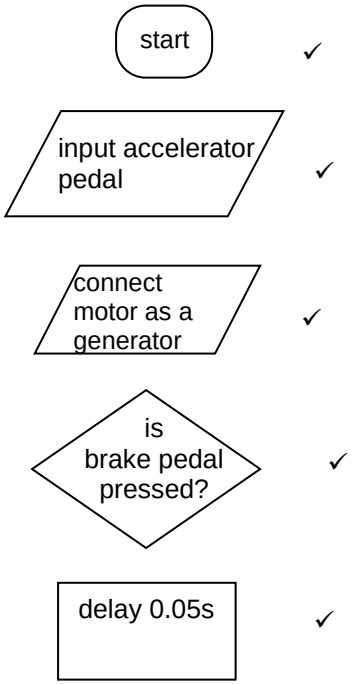
6	(a)	(ii)	 To be added connecting to the left hand side of the MP3 device		**1**

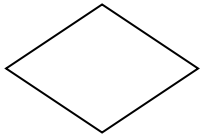
6	(b)	(i)	Amplitude modulation✓		**1**

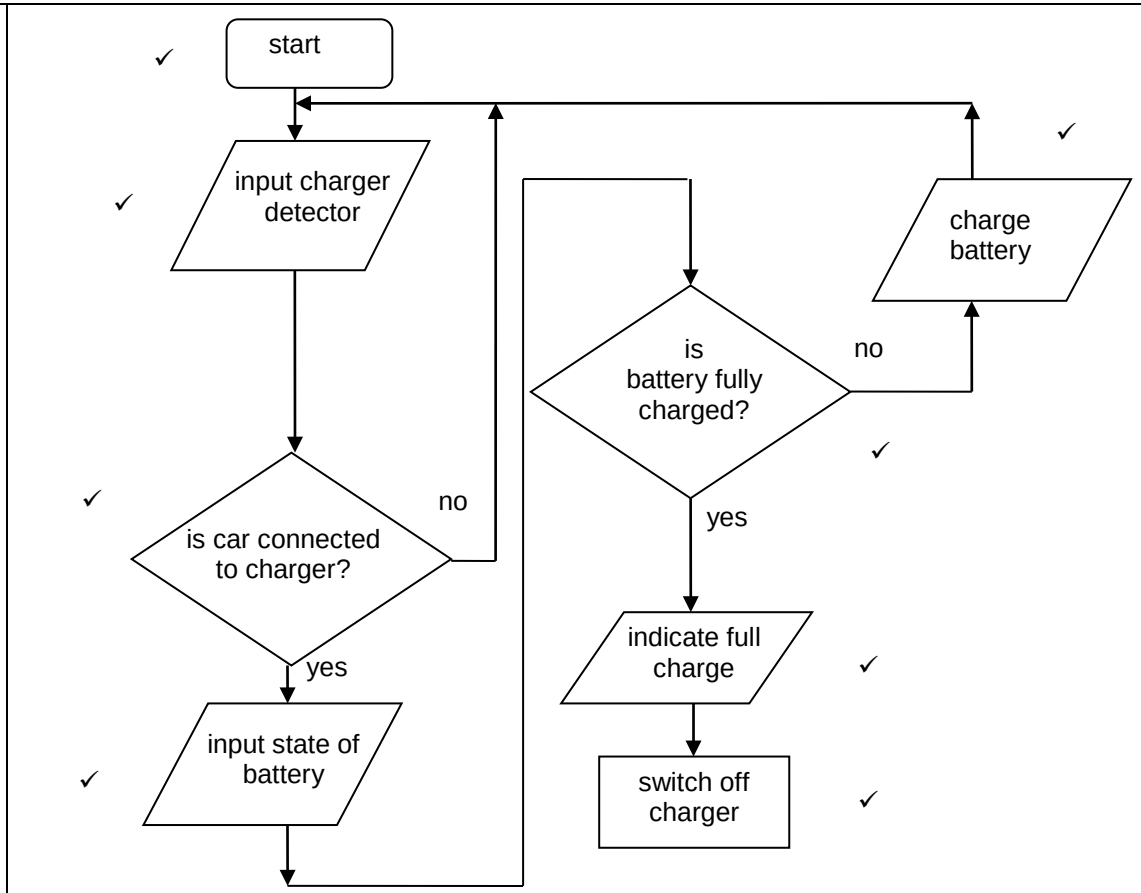
6	(b)	(ii)	Frequency modulation✓		**1**

6	(b)	(iii)	Showing constant frequency✓ variation in amplitude✓		**2**

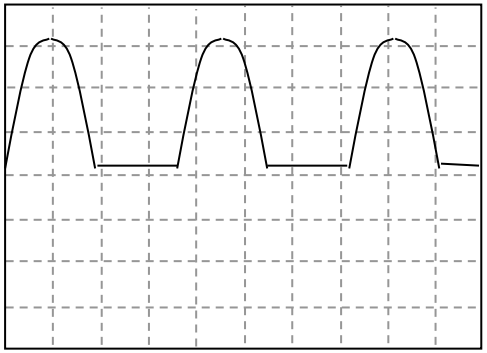
6	(b)	(iv)	tuned circuit/tuner ✓		**1**

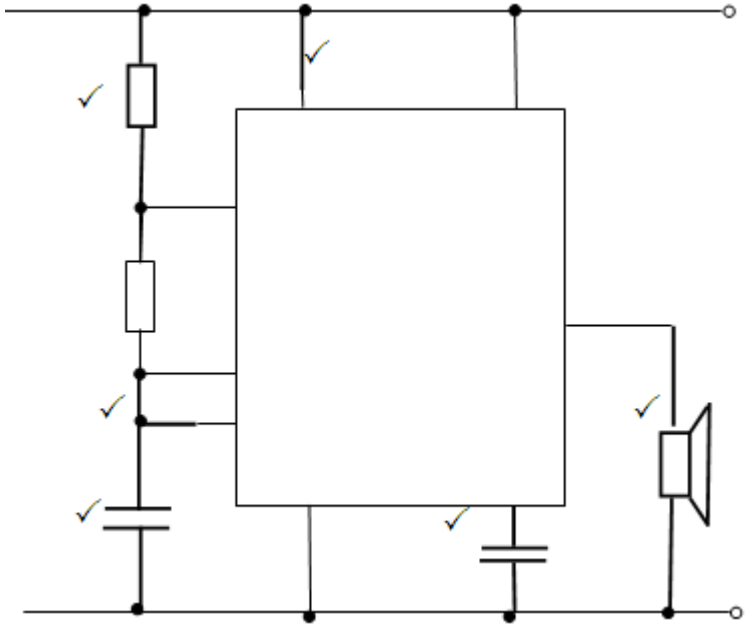
7	(a)		 start input accelerator pedal connect motor as a generator is brake pedal pressed? delay 0.05s ✓ ✓ ✓ ✓ ✓		**5**

7	(b)		decision box  ✓ input box  ✓ a loop is any line that returns to a point earlier in the flow chart✓ output box  ✓ process box  ✓		**5**

7	(c)		 Max 8 Marks		**8**

8	(a)	(i)	fuse✓ diode✓ transformer✓		**3**

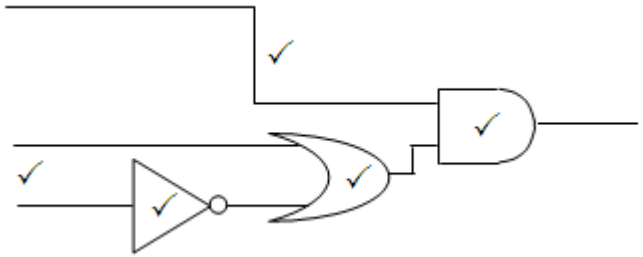
8	(a)	(ii)	 Half sine wave shape, and gap✓ Half sine wave shape at least one div. amplitude✓ Sine wave shape and gap approx equal times✓ (Full wave rectified 1 max)		**3**
8	(a)	(iii)	half wave✓		**1**
8	(a)	(iv)	capacitor symbol across output✓ symbol for electrolytic/polarised✓		**2**
8	(b)		Wire from astable out to NC ✓ Wire from COM to +ve terminal of 9V battery ✓ Wire from negative of 9V battery to bottom of astable ✓		**3**

8	(c)	(i)			**6**

8	(c)	(ii)	$T = (R_1 + 2R_2)\, C_1/1.44 = (1\times10^3 + 2 \times 12 \times10^3) \times 0.1 \times 10^{-6}/1.44$ ✓ $= 1.74$✓$\times10^{-3}$ s✓		**2**

8	(c)	(iii)	f =1/T = 1/1.74 $\times10^{-3}$ ✓ = 576 Hz ecf		**2**

8	(c)	(iv)	Suitable✓ in range of human hearing✓ ecf		**2**

9	(a)				**5**

9	(b)	(i)	<table><tr><td></td><td></td><td></td></tr><tr><td></td><td></td><td>1</td></tr><tr><td></td><td></td><td>1</td></tr><tr><td></td><td></td><td>1</td></tr><tr><td></td><td></td><td>0</td></tr></table> ✓		**1**

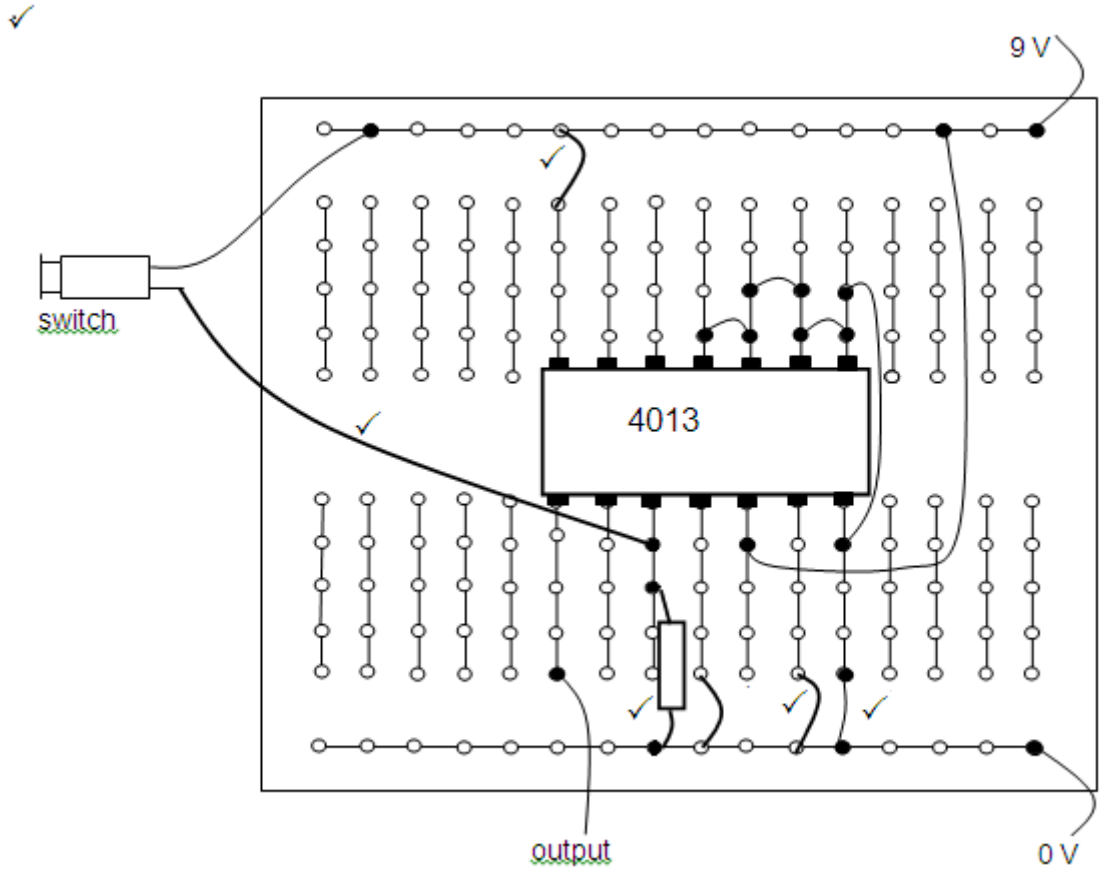
9	(b)	(ii)			**4**

			1	1	1	0	
			1	0	1	0	
			0	1	1	0	
			0	1	1	0	
			1	1	0	1	
			1	0	1	0	
			0	1	0	1	
			0	1	0	1	
			✓	✓	✓	✓	

9	(c)	(i)	Two series resistors✓ connected across supply rails and to V+✓		**2**
9	(c)	(ii)	The two inputs are called the inverting✓ and non-inverting✓ inputs. If the voltage at the inverting input is higher than the voltage at the non-inverting input ✓then the output voltage is low.✓If the voltage at the inverting input is lower than the voltage at the non-inverting input then the output voltage is high.✓		**5**
9	(d)	(i)	2.0 kΩ ✓		**1**
9	(d)	(ii)	100 lux ✓		**1**
9	(d)	(iii)	4.0 kΩ✓ because resistance should be equal to resistance of LDR/ so switch over occurs at correct voltage/gives 4.5 V at V^- ✓		**3**

10	(a)		Display box with arrow from counter✓ Reset box with arrow to counter✓		**2**
10	(b)		Switch B ✓ Then output from gate 1 goes high and gate 2 will then allow astable pulses to pass ✓		**2**
10	(c)	(i)	resistor and switch in series✓ connected to reset✓ switch above resistor✓		**3**
10	(c)	(ii)	connection output 9 to CI✓		**1**
10	(d)	(i)	1.2 × 100✓ = 120 ms (= 0.12 s)✓		**2**
10	(d)	(ii)	Tolerance of resistors/tolerance of capacitor/in accurate calibration of oscilloscope any two✓✓		**2**

10	(e)	(i)	CK becomes high ✓ high state at D copied to Q✓ Q stays high when switch released/latches✓		**3**

10	(e)	(ii)			**5**

10	(f)		brown, black✓ yellow✓, gold✓		**3**