

# General Certificate of Secondary Education 

## Electronics 3432

Tier H Higher

## Mark Scheme

2007 examination - June series

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1
(a) loudspeaker/siren/buzzer etc $\checkmark$ (1 mark)
(b) light dependent resistor/LDR/photodiode etc $\checkmark$
(c) process/processing (subsystem)/power supply $\checkmark$
(d) multimeter $\checkmark$
(e) parallel $\checkmark$, series $\checkmark$
(f) byter
(g) address $\checkmark$
(h) write/store $\checkmark$
(i) frequency $\checkmark$

2 (a) (i) $0.1(\mathrm{~A})^{\checkmark}$
(ii) $0.1 \times 30=3 \vee \checkmark \checkmark$
(iii) $\mathrm{P}=\mathrm{I}^{2} \mathrm{R} / \mathrm{VI} / \mathrm{V}^{2} / \mathrm{R}=0.3 \mathrm{~W} \checkmark \checkmark$
(iv) $0.5 \mathrm{~W} \checkmark$
(b) (i) $6(\mathrm{~V})^{\checkmark}$
(ii) correct symbol $\checkmark$, in parallel $\checkmark$
(c) orange $\checkmark$, black $\checkmark$, black $\checkmark$, gold $\checkmark$
(d) (i) correct symbol $\checkmark$ correct names $\checkmark$ in correct order $\checkmark$

(ii) high input resistance $\checkmark$ high "gain" (or equivalent) $\checkmark$

3 (a)

(b) decision box

input box

a loop - any line that returns to a point earlier in the flow chart $\checkmark$
output box

process box

(c) (i) $23 \mathrm{~s} \checkmark$
(ii) green on for 10s longer $\checkmark$
(iii) $\quad 2 \checkmark$
(iv) $6 s \checkmark$
(v) $56 s \checkmark$
(d)

(5 marks)
(Total 20 marks)

4 (a)

(8 marks)
(b) the maximum output current from logic gate or timer
is less than 450 mA (required by LED), or 12 V o/p $>4 \mathrm{~V}$ required $\checkmark$
(1 mark)
(c) (i) $8 \vee \checkmark$
(ii) $450 \mathrm{~mA} \checkmark$
(iii) $R=V \div I=8 \div 0.45 \checkmark=17.77 \Omega \checkmark$
(iv) $18 \Omega$ (allow $20 \Omega$ ) $\checkmark$
(d)

(6 marks)
(e)

(10 marks)
(Total 30 marks)

5
(a) (i) $3 \times 2=6 \vee \checkmark \checkmark$
(ii) $4 \times 0.5=2 \mathrm{~ms} / 0.002 \mathrm{~s} \checkmark \checkmark$
(iii) $1 / 0.002=500 \mathrm{~Hz} / 0.5 \mathrm{kHz} \checkmark \checkmark$
(iv) $6 / 50=0.12 \vee \checkmark \checkmark$
(8 marks)
(b) (i) range of frequencies $\checkmark$ for which the gain is at least half the maximum $/ V_{0}>\left(\mathrm{V}_{\text {max }} / \sqrt{ } 2\right)^{\checkmark}$
(ii) $25 \mathrm{kHz} \checkmark$
(iii) gain $\checkmark$ decreases $\checkmark$
(c) (i) $\quad \mathrm{V}_{\mathrm{RMS}}=6 / 1.4=4.2 / 4.3(\mathrm{~V})^{\checkmark}$
(ii) $\quad V_{\text {RMS }} I_{R M S}$ or $V_{R M S}{ }^{2} / R$ or $V_{P}^{2} / 2 R=4.4-4.6 \mathrm{~W} \checkmark \checkmark$

6
(a) (i) e.g.

(ii)

|  |  |  |  |
| :--- | :--- | :--- | :--- |
|  |  | 1 | 0 |
|  |  | 1 | 0 |
|  |  | 0 | 1 |
|  |  | 0 | 0 |
| $\checkmark$ |  |  |  |
| $\checkmark$ |  |  |  |

(iii)

(b) (i) out put is high if $\mathrm{V}_{+}>\mathrm{V}_{-} \checkmark$ out put is low if $\mathrm{V}_{+}<\mathrm{V}_{-} \checkmark$
(ii) $6 \times(30 / 50)=3.6 \vee \checkmark \checkmark$
(iii) ratios or current calc. $10 \mathrm{k} \Omega \checkmark \checkmark$
(iv) $\quad$ low/0 $\mathrm{V} / \leq 2 \mathrm{~V} \checkmark$
(c) (i) $\quad \mathrm{D}$ to bar $\mathrm{Q} \checkmark$ CK input $\checkmark \mathrm{Q}$ output $\checkmark$
(ii) All bar Qs to $D \checkmark$ both Qs to clock $\checkmark$ input $1^{\text {st }}$ CK $\checkmark$ output 3rdQ $\checkmark$
(iii)
$\left\{\begin{array}{l}0010 \\ 0011 \\ 0100 \\ 0101 \\ 0110 \\ 0111\end{array}\right.$
(9 marks)
(d) (i)

|  |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
|  |  |  | 1 | 0 | 1 | 0 |
|  |  |  | 1 | 0 | 1 | 0 |
|  |  |  | 1 | 0 | 1 | 0 |
|  |  |  | 1 | 0 | 1 | 0 |
|  |  |  | 1 | 0 | 1 | 0 |
|  |  |  | 1 | 0 | 1 | 0 |
|  |  |  | 0 | 1 | 1 | 0 |
|  |  |  | 0 | 1 | 0 | 1 |
| $\checkmark$ |  |  |  |  |  |  |

(ii) safe for car to set off/all safety sensors give $1 \checkmark$

7
(a) $\mathrm{T}=\left(\mathrm{R}_{1}+2 \mathrm{R}_{2}\right) \mathrm{C} / 1.44=(10+2 \times 30) \times 10^{3} \times 10 \times 10^{-6} / 1.44$
$=0.49 \mathrm{~s} \checkmark \checkmark \checkmark$
(3 marks)
(b) (i) battery wrong way round $\checkmark$
(ii) capacitor wrong way round $\checkmark$
(iii) resistors wrong way round $\checkmark$
(iv) supply to pins 4 and 8 missing $\checkmark$
(v) connection to 10 nF missing $\checkmark$
(vi) connection to pin 6 missing $\checkmark$
(c) (i) set input goes high $\checkmark$
(ii) reset input goes high $\checkmark$
(d)



(7 marks)
(e) (i) output goes high $\checkmark$ and stays high even if input goes low $\checkmark$
(ii) cannot (easily) be reset $\checkmark$
(f) (i) $0 \vee \checkmark$
(ii) pull up resistor/to keep $X$ high when switch is not pressed $\checkmark$
(iii) out put goes high $\checkmark$ because the AND gate already has one high input $\checkmark$
when the switch is pressed out put goes low(resets) $\checkmark$ provided that the input has gone low $\checkmark$ ( 3 max)

