OCR
RECOGNISING ACHIEVEMENT

ADVANCED SUBSIDIARY GCE

ELECTRONICS

Signal Processors

F612

Candidates answer on the question paper.

OCR supplied materials:
- None

Other materials required:
- Scientific calculator

Thursday 19 May 2011
Morning

Duration: 1 hour 30 minutes

OCE/27813

F6122

Candidate forename		Candidate surname	

Centre number						Candidate number				

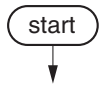
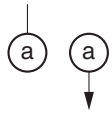
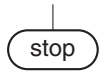
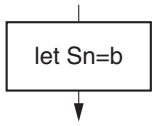
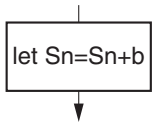
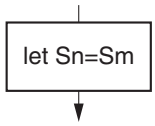
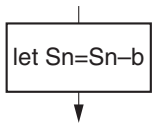
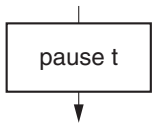
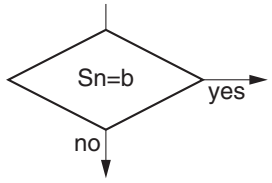
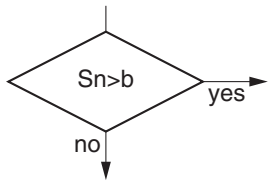
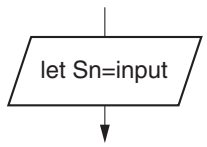
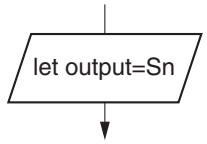
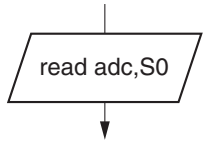
INSTRUCTIONS TO CANDIDATES

- Write your name, centre number and candidate number in the boxes above. Please write clearly and in capital letters.
- Use black ink. Pencil may be used for graphs and diagrams only.
- Read each question carefully. Make sure you know what you have to do before starting your answer.
- Write your answer to each question in the space provided. Additional paper may be used if necessary but you must clearly show your candidate number, centre number and question number(s).
- Answer **all** the questions.
- Do **not** write in the bar codes.

INFORMATION FOR CANDIDATES

- The number of marks is given in brackets **[ ]** at the end of each question or part question.
- The total number of marks for this paper is **90**.
- You will be awarded marks for your quality of written communication where this is indicated in the question.
- You are advised to show all the steps in any calculations.
- This document consists of **20** pages. Any blank pages are indicated.

A scientific calculator may be used for this paper

symbol	meaning
	start the program
	link to part of the program with the same label a
	stop the program
	place the byte b in register Sn
	add the byte b to the byte in register Sn
	copy the byte in register Sm into register Sn
	subtract the byte b from the byte in register Sn
	introduce a time delay of t milliseconds
	branch if the byte in register Sn is equal to the byte b
	branch if the byte in register Sn is greater than the byte b
	copy the byte at the input port to register Sn
	copy the byte in register Sn to the output port
	activate the analogue-to-digital converter and store the result in register S0

Data Sheet

Unless otherwise indicated, you can assume that:

- op-amps are run off supply rails at +15V and –15V
- logic circuits are run off supply rails at +5V and 0V.

resistance	$R = \frac{V}{I}$
power	$P = VI$
series resistors	$R = R_1 + R_2$
time constant	$\tau = RC$
monostable pulse time	$T = 0.7RC$
relaxation oscillator period	$T = 0.5RC$
frequency	$f = \frac{1}{T}$
voltage gain	$G = \frac{V_{out}}{V_{in}}$
open-loop op-amp	$V_{out} = A(V_+ - V_-)$
non-inverting amplifier gain	$G = 1 + \frac{R_f}{R_d}$
inverting amplifier gain	$G = -\frac{R_f}{R_{in}}$
summing amplifier	$-\frac{V_{out}}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} \ldots$
break frequency	$f_0 = \frac{1}{2\pi RC}$
Boolean Algebra	$A.\overline{A} = 0$
	$A + \overline{A} = 1$
	$A.(B + C) = A.B + A.C$
	$\overline{A.B} = \overline{A} + \overline{B}$
	$\overline{A + B} = \overline{A}.\overline{B}$
	$A + A.B = A$
	$A.B + \overline{A}.C = A.B + \overline{A}.C + B.C$

Answer **all** the questions.

1 Fig. 1.1 shows an amplifier based on an op-amp.

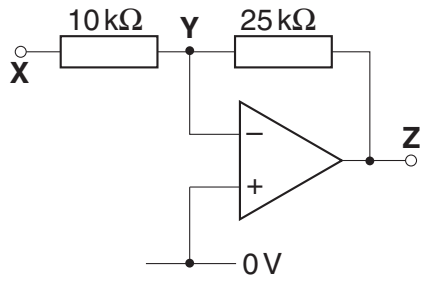


Fig. 1.1

(a) The amplifier processes the ac signal placed at its input.

(i) On Fig. 1.1, label the **input** of the amplifier. **[1]**

(ii) Three different properties of an ac signal are shown below.

Put a tick (✓) in the box next to each property which is altered by an **ideal** amplifier.

shape ☐

amplitude ☐

frequency ☐

[1]

(b) (i) Calculate the gain *G* of the amplifier of Fig. 1.1.

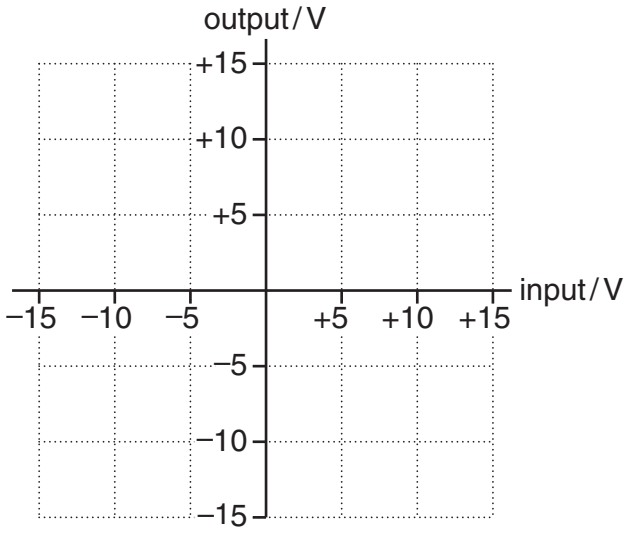
G = ... **[2]**

(ii) Complete the table for the amplifier for Fig. 1.1.

voltage at **X**	voltage at **Y**	voltage at **Z**
+5 V		

[2]

(iii) Use your value for *G* to draw the transfer characteristic of the amplifier, shown in Fig. 1.1, on the axes below.



[3]

(c) The amplifier of Fig. 1.1 is only ideal for ac signals which have small enough amplitudes at the input.

(i) Calculate the maximum amplitude of input signal which allows the amplifier to have ideal behaviour.

amplitude = ... V **[2]**

(ii) Describe a practical test to show that the amplifier of Fig. 1.1 has non-ideal behaviour for large enough input signals.

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.....

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.....

.....

..... **[3]**

[Total: 14]

2 Fig. 2.1 shows a microcontroller connected to five different sub-systems.

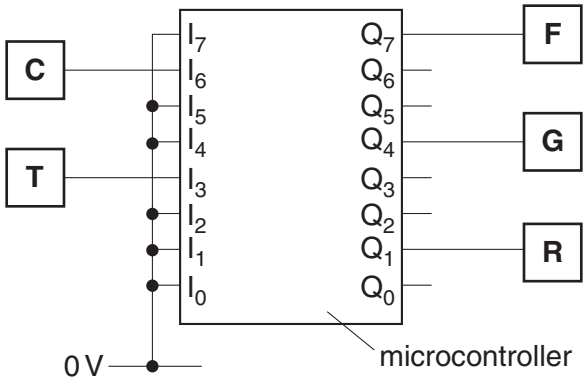


Fig. 2.1

The system controls the ceiling fan in a room depending on the time of day and the temperature. The table summarises the behaviour of the sub-systems.

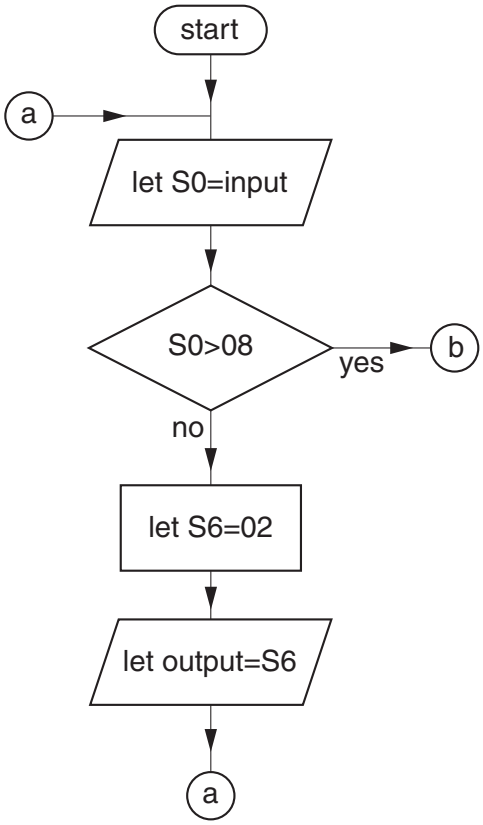
sub-system	device	transfer characteristic
C	clock	only goes high during the night
T	sensor	only goes high when the room is hot
F	fan	only turns on when high
G	green LED	only glows when high
R	red LED	only glows when high

(a) Complete the truth table for the word at the input port.

room conditions	binary	hexadecimal
hot at night	0100 1000	48
cold at night		40
hot during the day	0000 1000	
cold during the day		

[3]

(b) The flowchart for part of the program in the microcontroller is shown below.



(i) Explain why program control passes to **b** only during the night.

.....

.....

.....

..... **[2]**

(ii) State and explain the state of the three output devices during the day.

.....

.....

.....

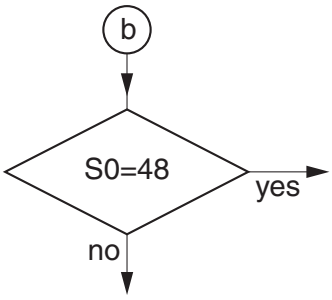
.....

..... **[3]**

(c) The incomplete flowchart for the rest of the program is shown below.
It has to make the system behave as follows:

- only turn on the fan for 60 s if the room is hot, then return to **a**
- only make the green LED glow when fan is on
- make the red LED glow all the time

Complete the flowchart below using only the symbols in the Data Sheet on page 2.



[4]

[Total: 12]

3 Fig. 3.1 shows the inputs and outputs of a D flip-flop.

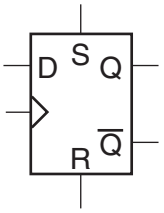
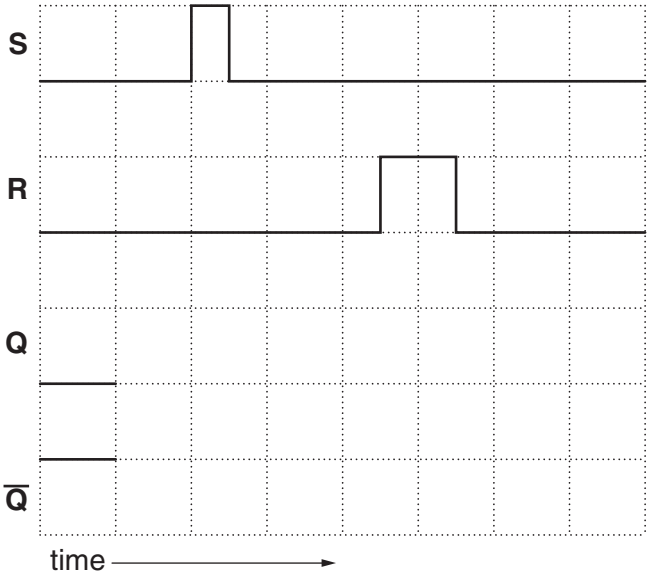


Fig. 3.1

(a) Complete the timing diagram below for the flip-flop.
Assume that unused inputs are held at 0 V and Q is initially low.



[3]

(b) Q is initially low. Explain how to make Q high by using the D and clock terminals.
Assume that unused inputs are held at 0 V.

.....

.....

..... **[3]**

(c) The registers and ports of a microcontroller are made from D flip-flops.

(i) Describe the function of a register in a microcontroller.

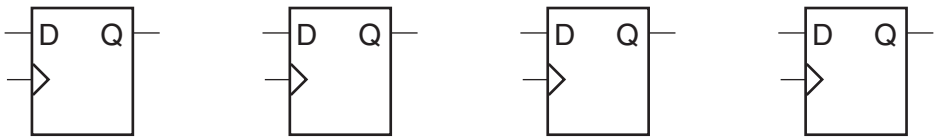
.....

.....

.....

..... **[3]**

(ii) Draw on Fig. 3.2 to show how D flip-flops can be used to make a four-bit register. Label the input, output and clock terminals.



[3]

Fig. 3.2

(iii) Describe the function of the ports of a microcontroller.

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.....

.....

..... **[2]**

[Total: 14]

4 Fig. 4.1 is the circuit diagram of a simple passive filter.

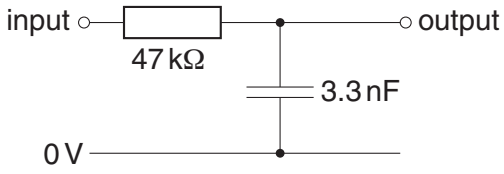


Fig. 4.1

(a) Show that the break frequency of the filter is about 1 kHz.

[2]

(b) (i) Put a (ring) around the correct name for the filter shown in Fig. 4.1.

bandpass **bass cut** **treble cut**

[1]

(ii) Complete the sentences to explain the operation of the filter.
Choose the best words from this list.

larger than **smaller than** **the same as**

At a frequency of 1 Hz the capacitor's impedance is ..... 47 kΩ.

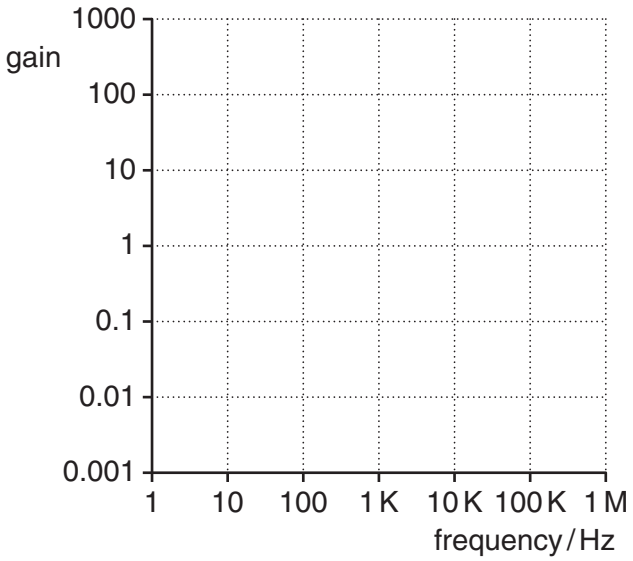
So the signal at the output is ..... the signal at the input.

At a frequency of 1 MHz the capacitor's impedance is ..... 47 kΩ.

So the signal at the output is ..... the signal at the input.

[4]

(c) On the axes below, draw the transfer characteristic of the filter shown in Fig. 4.1.



[3]

(d) Fig. 4.2 shows the block diagram of an audio amplifier system.

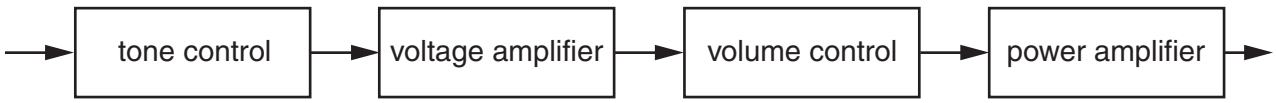


Fig. 4.2

(i) State which block could be made from a passive filter.
Describe its function in the whole audio amplifier system.

.....

.....

.....

..... **[2]**

(ii) Explain why the system has a power amplifier.

.....

.....

.....

..... **[2]**

[Total: 14]

5 Fig. 5.1 is the circuit diagram for a system which produces a train of pulses at **E** each time there is a short pulse at **S**.

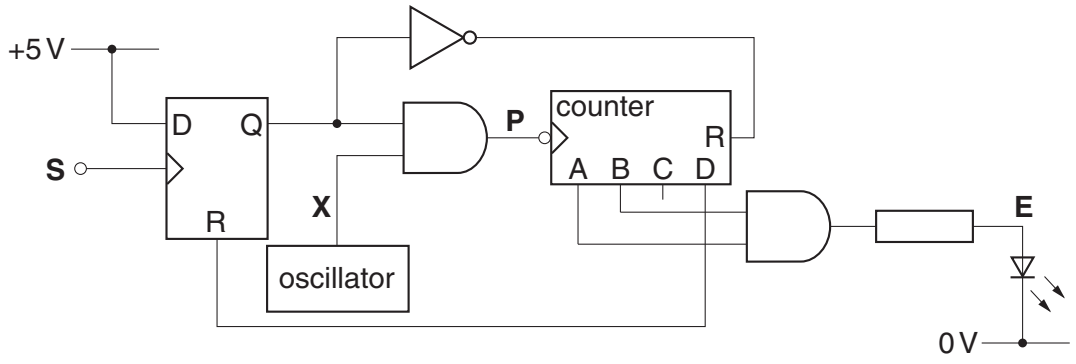


Fig. 5.1

(a) The oscillator produces a continuous train of pulses at **X**.
Those pulses only get through to **P** after there is a pulse at **S**.
Explain why.

.....

.....

.....

.....

..... **[3]**

(b) Explain why only eight pulses appear at **P** for each pulse at **S**.

.....

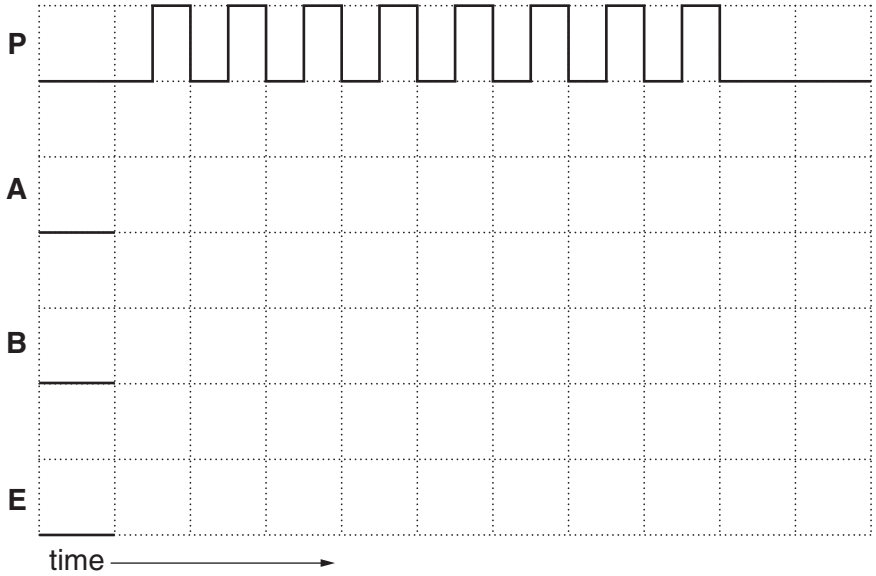
.....

.....

.....

..... **[4]**

(c) Complete the timing diagram below where **A**, **B** and **E** start off low. **[3]**



(d) The binary counter of Fig. 5.1 can be made from D flip-flops. Each D flip-flop of the counter has D connected to $\overline{Q}$, as shown in Fig. 5.2.

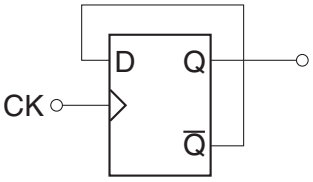


Fig. 5.2

(i) Explain how the flip-flop of Fig. 5.2 operates as a one-bit counter.

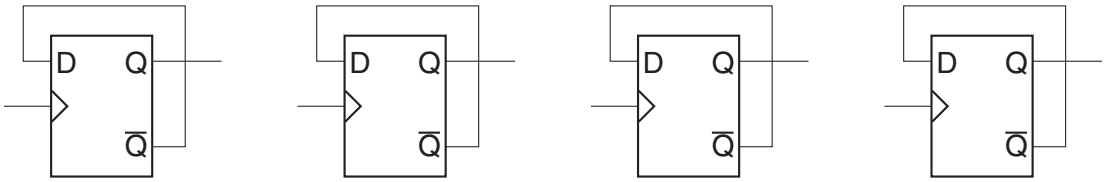
.....

.....

.....

..... **[3]**

(ii) On the diagram below show how the four one-bit counters of Fig. 5.2 and a NOT gate can be connected to make the counter of Fig. 5.1. Label **P**, **A**, **B**, **C** and **D**. **[4]**



[Total: 17]

6 A student designs the circuit of Fig. 6.1.

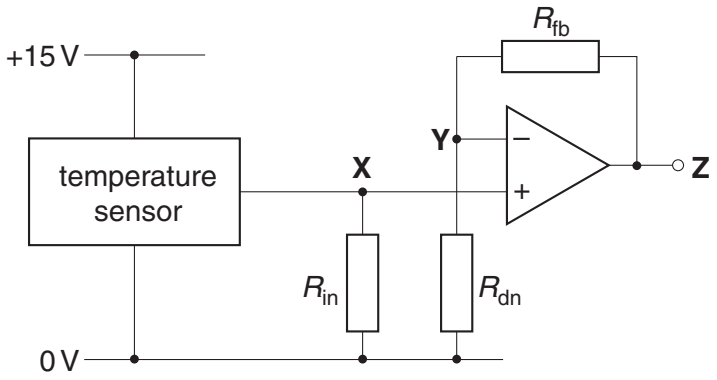


Fig. 6.1

The data sheet for the temperature sensor provides the following information.

parameter	**value**
supply voltage	9 V to 18 V
output voltage	0.10 T where T is the temperature in °C
output impedance	10 kΩ

(a) The student decides to amplify the signal from the sensor at **X** by +5.
Suggest values for R_{fb} and R_{dn} which will achieve this.
Justify them with a calculation.

R_{fb} = ... Ω

R_{dn} = ... Ω
[3]

(b) The student tests the system by holding the sensor at a temperature of 15 °C and measuring the voltage at **Z**. This is shown in the circuit of Fig. 6.2.

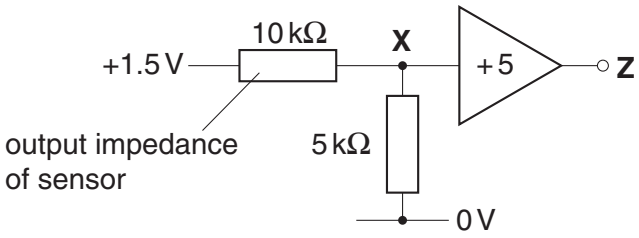


Fig. 6.2

(i) State the value of R_{in} selected by the student.

R_{in} = ... Ω **[1]**

(ii) Do calculations to show that the voltage at **Z** is +2.5 V.

[3]

(iii) Suggest a value for R_{in} which would allow the voltage at **Z** to be +7.5 V.
Give a reason for its value.

R_{in} = ... Ω **[2]**

[Total: 9]

7 Fig. 7.1 shows a pair of NOR gates connected as a bistable.

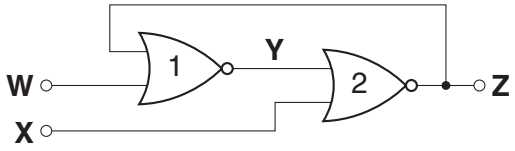


Fig. 7.1

(a) Complete the truth table for gate 2.

X	Y	Z

[2]

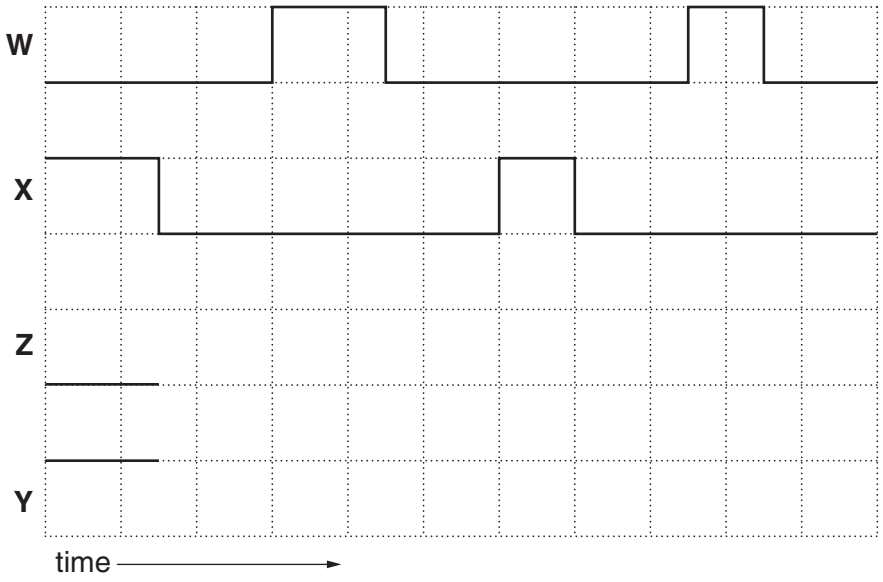
(b) Use the table to explain why **X** is an active-high reset for the bistable.

.....

.....

..... **[2]**

(c) Complete the timing diagram below for the bistable of Fig. 7.1.
Z is initially low and **Y** is initially high.



[3]

[Total: 7]

Quality of Written Communication **[3]**

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