OCR
RECOGNISING ACHIEVEMENT

GCE

Electronics

Advanced Subsidiary GCE

Unit **F612:** Signal Processors

Mark Scheme for June 2011

This mark scheme is published as an aid to teachers and students, to indicate the requirements of the examination. It shows the basis on which marks were awarded by Examiners. It does not indicate the details of the discussions which took place at an Examiners' meeting before marking commenced.

All Examiners are instructed that alternative correct answers and unexpected approaches in candidates' scripts must be given marks that fairly reflect the relevant knowledge and skills demonstrated.

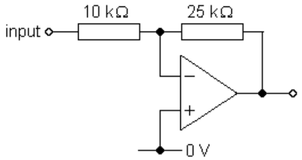
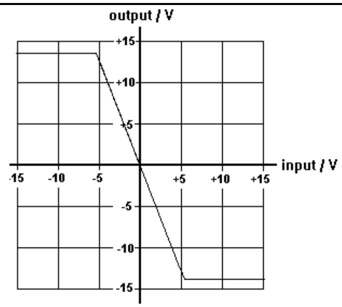
Mark schemes should be read in conjunction with the published question papers and the Report on the Examination.

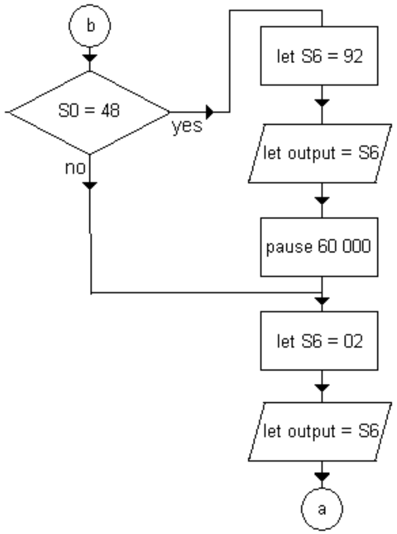
OCR will not enter into any discussion or correspondence in connection with this mark scheme.

Any enquiries about publications should be addressed to:

OCR Publications
PO Box 5050
Annesley
NOTTINGHAM
NG15 0DL

Telephone: 0870 770 6622
Facsimile: 01223 552610
E-mail: publications@ocr.org.uk

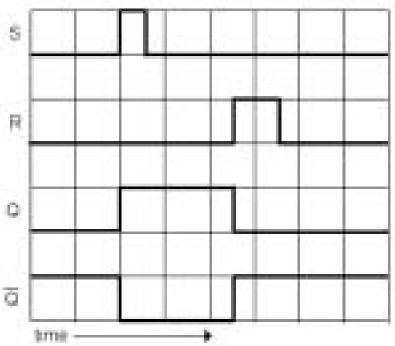
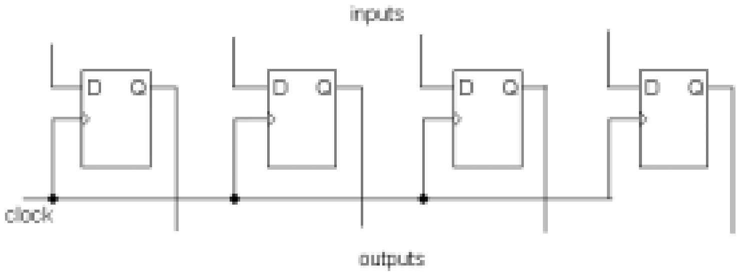
Question			Grade	Expected Answer	Mark	Additional Guidance
1	(a)	(i)	E		[1]	any unambiguous indication of correct terminal
		(ii)	E		[1]	correct pattern for [1]
	(b)	(i)	E E	-25/10 = -2.5	[2]	2.5 for [1] 3.5 for [1]
		(ii)	B B	+5 V / 0 V / -12.5 V	[2]	ecf: if G =+2.5, then 12.5 V if G = +3.5, then 13 V no other values ecf
		(iii)	C D E		[3]	saturation at +13 V and -13 V for [1] straight line through origin (by eye) between output +13 V and -13 V for [1] correct gradient (+12.5±0.5 V at -5 V) for [1] ecf from b i : accept +12.5 V for +5V accept saturates at +3.7 V otherwise no ecf
	(c)	(i)	A B	13/2.5 = 5.2 V	[2]	15 / 2.5 = 6.0 V for [1] allow ecf from bi: G = 3.5 gives 3.7 V for [2] and 4.3 V for [1] ignore sign of answer
		(ii)	A D E	any of the following for [1] each • signal generator / a.c. signal at input; • oscilloscope to look at input and output; • <u>increase</u> input signal • until flattening of peaks and troughs of ac signal at output / trace changes shape / signal is clipped / saturation occurs	[3]	**not** potentiometer to make d.c. signal **not** voltmeter / multimeter **not** just distortion, must describe change of shape

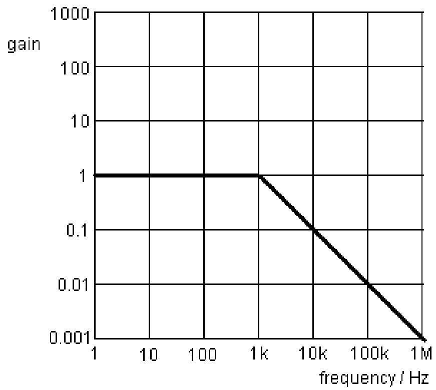
<table>
<tr><th colspan="3">Question</th><th>Grade</th><th>Expected Answer</th><th>Mark</th><th>Additional Guidance</th></tr>
<tr><td>2</td><td>(a)</td><td></td><td>D
E
E</td><td><table><tr><td>0100 0000</td><td></td></tr><tr><td></td><td>08</td></tr><tr><td>0000 0000</td><td>00</td></tr></table></td><td>[3]</td><td>each correct row for [1]
don't accept missing leading 0s, penalise once</td></tr>
<tr><td></td><td>(b)</td><td>(i)</td><td>A
E</td><td>S0 is 00 or 08 during the day;
S0 is 40 or 48 during night;</td><td>[1]
[1]</td><td>must mention both states for day
accept S0 at least 40 at night</td></tr>
<tr><td></td><td></td><td>(ii)</td><td>A
B
C</td><td>S6 loaded with 0000 0010;
R high/on, G and F low/off;
so red LED on, green LED off, fan off</td><td>[1]
[1]
[1]</td><td>
no ecf from incorrect binary in S6</td></tr>
<tr><td></td><td>(c)</td><td></td><td>A
B
C
D</td><td>
</td><td>[4]</td><td>from yes:
load any register with 92 and output [1]
time delay of 60 000 ms [1]
accept EA60 for 60 000
before returning output port to 02 (using any register) and pass to a [1]

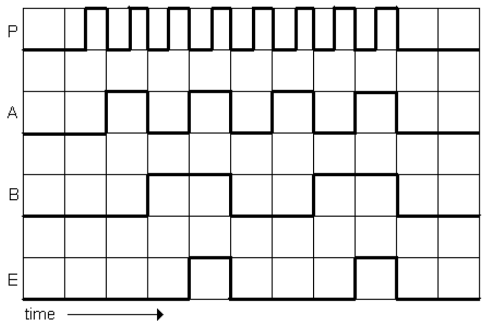
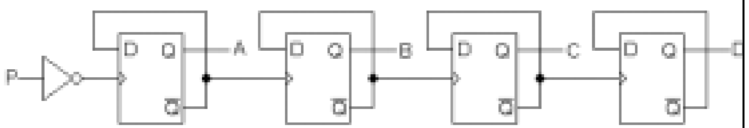
from no:
make output port to 02 (using any register) and pass to a [1]

penalise mistake in common code only once

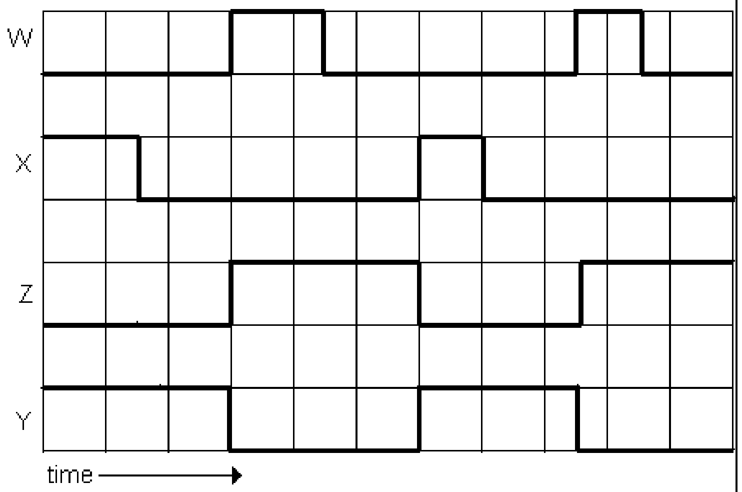
penalise incorrect syntax or box shape or lack of arrows only once
ignore $ in front of hexadecimal words</td></tr>
</table>

Question			Grade	Expected Answer	Mark	Additional Guidance
3	(a)		C D E		[3]	Q and $\overline{Q}$ have opposite states [1] Q high when S goes high, Q low when R high [1] state of Q unchanged when R and S go low [1] judge alignment of edges by eye, but only penalise once
	(b)		A D E	hold D high; feed one voltage pulse / rising edge into clock; D copied to Q;	[1] [1] [1]	**accept** connect to $\overline{Q}$ **not** just hold clock high / several pulses for D=$\overline{Q}$
	(c)	(i)	A A A	any three of the following for [1] each • holds / stores information • e.g. data / numbers / variables / instructions • as bits / words / bytes / binary • so that it can processed	[1] [1] [1]	**accept** one-word memory **accept** named process e.g. add, subtract, accept from input port, pass to output port, copy to or from another register
		(ii)	D E E		[3]	clock terminals labelled and in parallel [1] labelled D terminals as inputs/I_n [1] labelled Q terminals as outputs/Q_n [1]
		(iii)	A A	allows a word from register / microcontroller to output; allows a word from input to be copied to register / microcontroller;	[1] [1]	**accept** allows information / words / bytes / data / signals in **and** out for [1] **not** just input and output ports

Question			Grade	Expected Answer	Mark	Additional Guidance
4	(a)		D E	$f = \dfrac{1}{2\pi RC}$, $R = 47\times10^3\ \Omega$, $C = 3.3\times10^{-9}$ F 1.03×10^3 (Hz)	[1] [1]	substitution into correct equation for [1] evaluation for [1] (ecf on incorrect powers of 10) **accept** 1.0×10^3 Hz **not** 1 kHz **accept** $f = \dfrac{1}{2\pi \times 47\text{k} \times 3.3\text{n}}$
	(b)	(i)	E	treble cut	[1]	
		(ii)	A B A B	larger than the same as smaller than smaller than	[1] [1] [1] [1]	no ecf at all
	(c)		E C A		[3]	horizontal below 1 kHz [1] with a gain of 1 [1] dropping at 45 degrees above 1 kHz [1] must cover all frequencies (penalise only once). ecf for bass cut: horizontal above 1 kHz [1] with a gain of 1 [1] rising at 45 degrees below 1 kHz [1] ecf for bandpass: rising at 45 degrees at or below 1 kHz [1] dropping at 45 degrees at or above 1 kHz [1] maximum gain of 1 [1] **accept** correct plot regardless of bi for [3]
	(d)	(i)	E A	tone control; provides correct frequency balance of output signal / compensates for frequency balance of input signal / removes high frequency noise in signal	[1] [1]	**not** just reduces high frequency signals or a general description of a tone control **look for** sensible justification for use for treble cut filter
		(ii)	B C	power amp can provide lots of <u>current</u>; loudspeakers need large power / require high current / are low resistance	[1] [1]	**not** more power / voltage **not** just loudspeakers

Question			Grade	Expected Answer	Mark	Additional Guidance
5	(a)		C B A	when Q is low AND gate forces P low (as 0.X = 0) pulse at S copies 1 at D to Q so P = 1.X = X	**[1]** **[1]** **[1]**	AND gate blocks pulses when Q = 0 for [1] flip-flop copies 1 at D to Q when pulse at S for [1] AND gate transmits pulses when Q = 1 for [1]
	(b)		B C D E	any of the following for [1] each • pulses counted by binary counter • starting from 0000 • counter reset when Q = 0 • D / R goes high on eighth pulse • resetting flip-flop • forcing P to stay low again/stopping pulses getting through AND gate	**[4]**	
	(c)		E E E		**[3]**	A changes on each falling edge of P ecf A: B changes on each falling edge of A ecf A, B; E only high each time A and B both high must go all way across first ten squares, penalise only once.
	(d)	(i)	A A A	D is opposite state to Q; pulse / rising edge at CK copies D to Q; so need two pulses at CK for one pulse at Q / first pulse sets Q to 1 and second pulse resets it to 0 / Q changes state for each pulse at CK;	**[1]** **[1]** **[1]**	**not** just Q and $\overline{Q}$ have opposite states **ignore** timing diagrams
		(ii)	E E E C		**[4]**	outputs identified [1] correctly labelled [1] $\overline{Q}$ to next clock [1] input P to clock via NOT gate [1]

Question			Grade	Expected Answer	Mark	Additional Guidance
6	(a)		E E D	ratio $R_{fb} : R_{in}$ = 4:1 justified by use of $G = 1 + R_f/R_d$ resistors in range 1 kΩ to 10 MΩ	[1] [1] [1]	 **look** for substitution and evaluation
	(b)	(i)	E	5 kΩ	[1]	
		(ii)	E C E	voltage at X = 0.5 V justified by voltage divider calculation voltage at Z = 0.5 × 5 (= 2.5 V)	[1] [1] [1]	 **accept** resistor ratios argument **accept** correct sum without explanations for [3] e.g. $1.5 \times \frac{5\text{k}}{15\text{k}} \times 5 = 2.5\text{V}$
		(iii)	E D	anything greater or equal to 100 kΩ; make input impedance much larger than output impedance/less loss of signal in voltage divider/less lost volts in sensor/less current from sensor	[1] [1]	 **accept** correct calculation to justify value

<table>
<tr><th colspan="3">Question</th><th>Grade</th><th>Expected Answer</th><th>Mark</th><th>Additional Guidance</th></tr>
<tr><td>7</td><td>(a)</td><td></td><td>E
E</td><td><table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table></td><td>[2]</td><td>all four input states in any order [1]
correct Z column [1]</td></tr>
<tr><td></td><td>(b)</td><td></td><td>E
E</td><td>holding X high makes Z low;
by reference to the table or gate properties or boolean algebra;</td><td>[1]
[1]</td><td>
look for valid justification</td></tr>
<tr><td></td><td>(c)</td><td></td><td>E
D
C</td><td></td><td>[3]</td><td>Y and Z have opposite states throughout [1]
Y low when W is high, Z low when X high [1]
Z and Y unchanged when X or W go low [1]</td></tr>
</table>

Quality of Written Communication

3 The candidate expresses complex ideas extremely clearly and fluently. Sentences and paragraphs follow on from one another smoothly and logically. Arguments are consistently relevant and well structured. There will be few, if any, errors of grammar, punctuation and spelling.

2 The candidate expresses straightforward ideas clearly, if not always fluently. Sentences and paragraphs may not always be well connected. Arguments may sometimes stray from the point or be weakly presented. There may be some errors of grammar, punctuation and spelling, but not such as to suggest a weakness in these areas.

1 The candidate expresses simple ideas clearly, but may be imprecise and awkward in dealing with complex or subtle concepts. Arguments may be of doubtful relevance or obscurely presented. Errors in grammar, punctuation and spelling may be noticeable and intrusive, suggesting weaknesses in these areas.

0 The language has no rewardable features.

OCR (Oxford Cambridge and RSA Examinations)
1 Hills Road
Cambridge
CB1 2EU

OCR Customer Contact Centre

14 – 19 Qualifications (General)
Telephone: 01223 553998
Facsimile: 01223 552627
Email: general.qualifications@ocr.org.uk

www.ocr.org.uk

For staff training purposes and as part of our quality assurance programme your call may be recorded or monitored