

GCE MARKING SCHEME

ELECTRONICS AS/Advanced

JANUARY 2012

INTRODUCTION

The marking schemes which follow were those used by WJEC for the January 2012 examination in GCE ELECTRONICS. They were finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conferences were held shortly after the papers were taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conferences was to ensure that the marking schemes were interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conferences, teachers may have different views on certain matters of detail or interpretation.

WJEC regrets that it cannot enter into any discussion or correspondence about these marking schemes.

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1. EXOR gate (a)

(b) NAND (i)

(ii)

А	В	Q ₁	Q ₂	Q ₃
0	0	0	1	0
1	0	1	0	0
0	1	1	0	0
1	1	0	0	1

 Q_1 and Q_3 correct 1 mark each. Allow e.c.f. for Q_1 from (a)

(c)
$$Q_1 = A \oplus B \text{ or } \overline{A}.B + A.\overline{B}$$
 (1)
 $Q_2 = \overline{A.B} \text{ or } \overline{A} + \overline{B}$ (1)
 $Q_3 = A .B \text{ or } \overline{A \oplus B + \overline{A.B}}$ (any combination of the above) (1) 3
(d) AND allow e.c.f. from (b)(ii) 1
(e) D_3 to 5V D_0 , D_1 and D_2 to 0V allow e.c.f. from Q_3 in table 1
[9]

2.

(a)

(i) $Q = \overline{C}.B.\overline{A} + C.\overline{B}.\overline{A} + C.B.\overline{A}$

(ii) Correct map (1 mark)

(one mistake = 1 mark)

2

1 1

2

BA $Q = B.\overline{A} + C.\overline{A}$ 00 01 11 10 С (1 mark - 2 correct)terms) 0 1 $=\overline{A}$.(B+C) 1 1 1 (1 mark – fully simplified)

OR Correct simplified Boolean solution = 3 marks

3

 $Q = \overline{(\overline{A} + B)}.A.\overline{B}$

DeMorgan	$Q = (\overline{A} + B) + \overline{A.\overline{B}}$	
DeMorgan	$Q = \overline{A} + B + \overline{A} + B$ (2 marks by direct method)	
Simplify	$Q = \overline{A} + B$	3

[8]

Switch X	Switch Y	Input A	Input B	Output Q	State of LED
Open	Open	1	0	1	OFF
Open	Closed	1	1	1	OFF
Closed	Open	0	0	0	ON
Closed	Closed	0	1	1	OFF

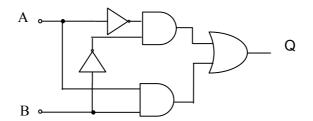
1 mark each correct column (4) allow e.c.f. on columns Q and LED	1	mark each	correct column	(4)	allow e.c.f.	on columns	O and LED
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[4]

1

4





Or any other correct alternative

- (b) NAND replacement of NOT x2 (1) 3 NAND replacement of AND x2 (1) NAND replacement of OR (1) Allow e.c.f. from part (a)
- (c) 2 correct redundancies one mark each 2

[6]

5. (a) (i) BCD 0101 0011 (1) Binary 110101 (1)

(b)

Display	Α	В	а	b	с	d	e	f	Ę
н	0	0	1	0	0	1	0	0	0
C	0	1	0	1	0	0	1	0	(
J	1	0	0	1	0	0	1	0	(
!-	1	1	0	1	1	0	0	0	1

		(ii)	NOR gate. Allow e.c.f. from (b)(i). Answer consistent with table.	1 [6]
6.	(a)	(i)	Resets (Q=0) when R is logic 1	1
		(ii)	Switch and resistor across power rails + correct orientation (1) Correct connection to R (1)	2
	(b)		When the D-type is reset the output Q will be at logic 0 and the LED will be \mathbf{ON} (Both answers needed for 1 mark)	1
	(c)		Q goes high on rising-edge of X (1) Q goes low on rising-edge of Reset (1) \overline{Q} opposite of Q (1)	3
				[7]

[7]

2

1

2

7. (a)

(i) 14/2+1 = +8
(ii) 14/8 = 1.75 V Allow e.c.f. from (i)

(b) (i)

(c)

V_{IN}/V	V_{OUT} / V
-3.0	-14.0
-2.0	-14.0
-1.0	-8.0
1.0	8.0
2.0	14.0
3.0	14.0

	Correct sign (1) Correct values. Allow e.c.f. from (a)(i) (1)					
(ii)	Positive gradient slope through origin (consistent with table) (1) Line passes through $(1.0, 8.0)$ (consistent with table) (1) Saturation at 14.0 V (penalise curve) (1)					
	Increase the input voltage (or value 2.47 V)					

8.	(a)	(i)	Resistor between input and inverting input (1) Feedback resistor between output and inverting input (1) Non-inverting input connected to 0 V (1)	3
		(ii)	R_F and R_{IN} in ratio 12:1 (1) Both resistors $\geq 1 \ k\Omega$ (1)	2
	(b)	(i)	$\pm 12 \ge 80 = \pm 960 \text{ mV}$	1
		(ii)	Inverted sine wave of same frequency as signal (1) Peaks at 960 mV (voltage marked on axis) (1) Allow e.c.f from (b)(i)	2
	(c)		3/12 = 0.25 MHz or 250 kHz or 250 000 (Hz)	1
	(d)		Inverted graph with slew-rate shape on <u>both</u> edges (1) saturates at -14 V (must be labelled) (1) correct starting points and gradients (1) (reaches -14 V saturation at 4.5 µs and 0 V at 11.5 µs)	3

[12]

1

1

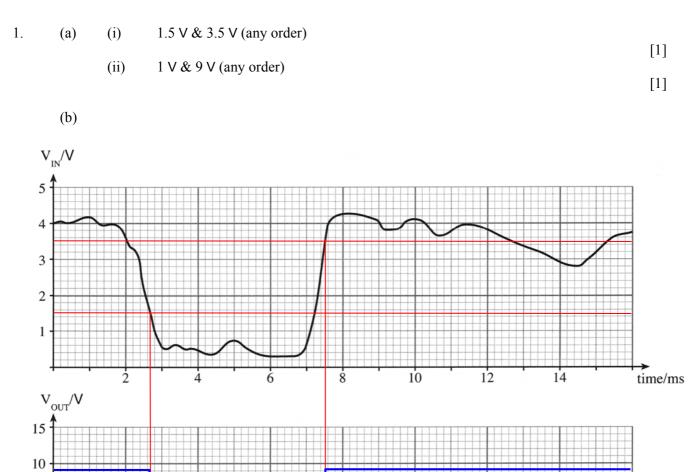
2

3

1

[8]

ET4



8

10

6

5

-5

-10

-15 -

ż

4

[3]

→ time/ms

Switching Thresholds (ecf a(i))	= 1 mark
Saturation values (ecf a(ii))	= 1 mark

12

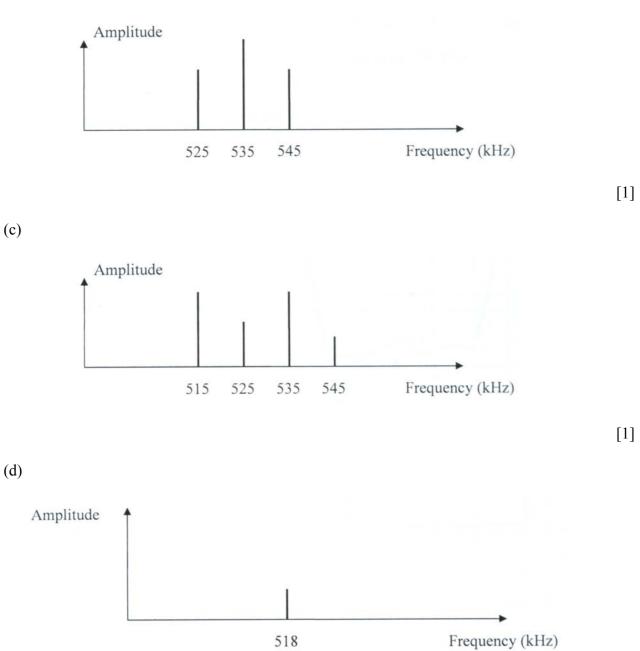
Non inverting action = 1 mark

14

Question Total = 5 marks

(b)

2.

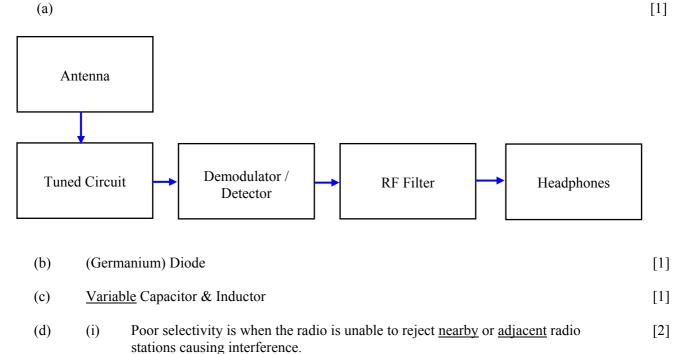


[1]

[1]

Question Total = 4 marks

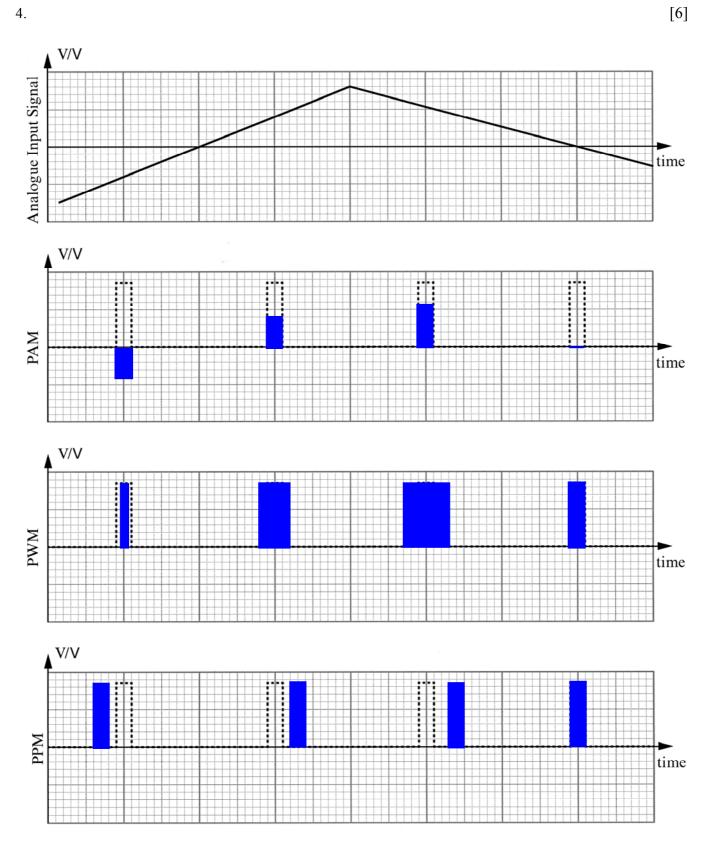
3.



- (ii) Poor sensitivity is when the radio is unable to pick up <u>weak</u> signals.
- (e) Any four from: [2] Tuned RF Amplifier / RF Amplifier Local Oscillator Mixer IF Filter IF Amplifier 3 correct blocks = 1 AF Amplifier 4 correct blocks = 2

Question Total = 7 marks

4.



Correct identification of modulation method = 3×1 mark Consistent application of method based on input signal = 3×1 mark

Question Total = 6 marks

5.

High Pass Filter. (a)

(b)
$$X_C = \frac{1}{2\pi fC} = \frac{1}{2\pi \times 10 \times 15 \times 10^{-9}} = 1.061032 \,\Omega \approx 1.06 \,\mathrm{M}\Omega$$

(1) (1) [2]

(d)
$$f_b = \frac{1}{2\pi RC}$$

 $f_b = \frac{1}{2\pi \times 3.3 \times 10^3 \times 15 \times 10^{-9}} = 3215 \text{ Hz} \approx 3.2 \text{ kHz}$

(e) [2]
Gain 1
 $f_b = \frac{1}{2\pi \times 3.3 \times 10^3 \times 15 \times 10^{-9}} = 3215 \text{ Hz} \approx 3.2 \text{ kHz}$

(c) [2]

Approx shape for HPF (e.c.f. (a)) = 1 mark Correct break frequency (at gain = 0.7) = 1 mark

Question Total = 8 marks

(c)

[1]

106 Ω (Accept ~100 Ω-110 Ω)

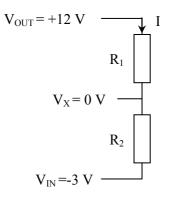
(d)

[2]

[1]

6. (a) V_{REF} is set at 0 V, therefore it does not matter whether V_{OUT} is at +12 V or -12 V, the voltage drop across R_1 is the same. [1]

(b)



$$I = \frac{12 - 0}{R_1} = \frac{12}{R_1}$$
 and $I = \frac{0 - (-3)}{R_2} = \frac{3}{R_2}$

The current I is the same so we can equate these equations.

$$\frac{12}{R_1} = \frac{3}{R_2}$$
$$\frac{12R_2}{3} = R_1$$
$$4R_2 = R_1$$

Or

$$V_{\mathbf{R}_1} : V_{\mathbf{R}_2}$$

$$12:3$$

$$4:1$$

$$\therefore \mathbf{R}_1: \mathbf{R}_2$$

$$\therefore 4:1$$

 $R_1 =40 k.....$

 $R_2 = \dots 10 k \dots$ [3]

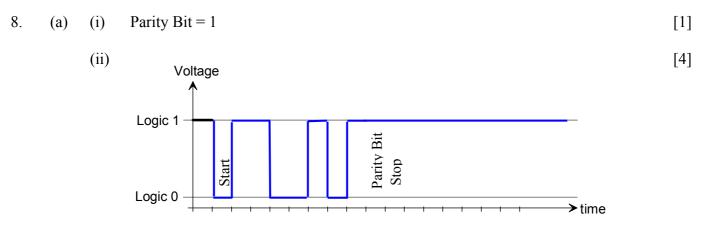
Calculation of ratio = 2 marks Correct resistors >1k = 1 mark

Question Total = 4 Marks

7.	(a)	(i)	Block X = Sampling Gate	[1]
		(ii)	Block Y = Analogue to Digital Converter	[1]
	(b)	(i)	$2^{12} = 4096$ levels	[1]
		(ii)	Period = 1 / frequency = $1/16000 = 0.0625$ ms or 62.5 µs.	[1]
		(iii)	60 bits must be transmitted in 62.5 μ s (1)	[3]
			1 bit = 62.5 μ s /60 = 1.04 μ s (1)	
			Min frequency = $\frac{1}{T} = \frac{1}{1.0416 \mu s} = 960061 \text{ Hz} \approx 960 \text{ kHz} (1)$	

Number of channels = $\frac{\text{sampling period}}{\text{No of bits} \times \text{PISO Period}}$ $5 = \frac{62.5\,\mu\text{s}}{12 \times \text{PISO Period}}$ $\text{PISO Period} = \frac{62.5 \times 10^{-6}}{5 \times 12}$ $\text{PISO Frequency} = \frac{5 \times 12}{62.5 \times 10^{-6}}$

Question Total = 7 marks



Correct graph = 2 marks / Data reversed = 1 mark 3 correct labels = 2 marks / 2 correct labels = 1 mark / 1 correct label = 0 mark

(b) (i) $P_4 = \dots 0 \dots P_3 = \dots 1 \dots P_2 = \dots 1 \dots P_1 = \dots 1 \dots P_0 = \dots 0 \dots [2]$ All 5 correct = 2 marks 4 correct = 1 mark

(ii)

D ₇	D_6	D_5	D_4	D ₃	D ₂	D_1	D_0	P ₄	P ₃	P ₂	P ₁	P ₀
1	1	0	1	1	0	0	1	1	1	0	1	0
												[1]

 P_1 , P_3 and P_4 fail, therefore the error is in D_6 as this is the only bit common to these three parity bits. [1]

Question Total = 9 marks

Paper Total = 50 marks



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