GCE MARKING SCHEME

ELECTRONICS
AS/Advanced

SUMMER 2014

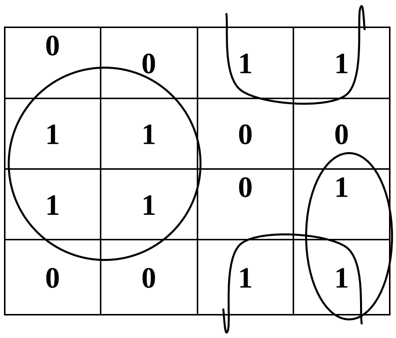
INTRODUCTION

The marking schemes which follow were those used by WJEC for the Summer 2014 examination in GCE ELECTRONICS. They were finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conferences were held shortly after the papers were taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conferences was to ensure that the marking schemes were interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conferences, teachers may have different views on certain matters of detail or interpretation.

WJEC regrets that it cannot enter into any discussion or correspondence about these marking schemes.

<table>
<tr><th colspan="3">Question</th><th>Marking details</th><th>Marks Available</th></tr>
<tr><td>1.</td><td>(a)</td><td>(i)</td><td>EXOR gate</td><td>1</td></tr>
<tr><td></td><td></td><td>(ii)</td><td>Columns Q_1 and Q_3 correct
<table>
<tr><th colspan="2">INPUTS</th><th colspan="3">OUTPUTS</th></tr>
<tr><th>B</th><th>A</th><th>Q_1</th><th>Q_2</th><th>Q_3</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
</table></td><td>2</td></tr>
<tr><td></td><td>(b)</td><td></td><td>$Q_1 = \overline{B}.\overline{A}$ or $\overline{B + A}$ (1)
$Q_2 = B \oplus A$ or $B.\overline{A} + \overline{B}.A$ (1)
$Q_3 = \overline{B.A}$ (or combinations from above) (1)</td><td>3</td></tr>
<tr><td></td><td>(c)</td><td></td><td>NAND gate ecf from (a) & (b)</td><td>1</td></tr>
<tr><td></td><td>(d)</td><td></td><td>Multiplexer connections correct.
D_3 to 0 V
D_0, D_1, D_2 to 5 V ecf from (a)</td><td>1</td></tr>
<tr><td></td><td></td><td></td><td></td><td>[8]</td></tr>
<tr><td>2.</td><td>(a)</td><td></td><td>Correctly drawn logic system using specified gates only
NOT A and NOT B to AND
B and A to AND
Both AND outputs to OR</td><td>1</td></tr>
<tr><td></td><td>(b)</td><td></td><td>Correct replacement NOT by NAND (both required) (1)
Correct replacement AND by NAND (both required) (1)
Correct replacement OR by NAND (1) ecf from (a)</td><td>3</td></tr>
<tr><td></td><td>(c)</td><td></td><td>Two correct redundancies clearly identified ecf from (b)</td><td>2</td></tr>
<tr><td></td><td></td><td></td><td></td><td>[6]</td></tr>
</table>

Question			Marking details	Marks Available
3.	*(a)*	(i)	$\overline{A}.1 = \overline{A}$	1
		(ii)	$B.\overline{B} + A.B + \overline{A}.\overline{B} + \overline{A}.A$ (1) correctly expanded brackets $A.B + \overline{A}.\overline{B}$ (1)	2
	(b)		 Three groups correctly identified (two 4's, one 2) (1) Any correct term from groups identified. (1) Simplest overall expression (1) **ecf** $\overline{C}.B + C.\overline{B} + (D.B.\overline{A}$ or $D.C.\overline{A})$	3
	(c)		Q = $\overline{\overline{A}.\overline{B}.A + \overline{A}.\overline{B}.\overline{B}}$ (1) OR $(\overline{\overline{A}}.\overline{\overline{B}}) + (\overline{A + \overline{B}})$ (1) Q= $\overline{\overline{A}}.\overline{\overline{B}}$ (1) either $A+B+\overline{A}.B$ or Q = A + B (1) $A + B(1 + \overline{A})$ (1) A + B (1) Note: 1 mark for correct answer, 2 independent marks for clearly shown correct working similar to above.	3
				[9]
4.	*(a)*	(i)	Reset when R is at logic 0 / active low	1
		(ii)	B and C outputs chosen (1) NAND gate used (1) Output of logic gate to reset (1)	3
	(b)	(i)	Display cycles/ changes rapidly (too rapidly to see individual numbers)	1
		(ii)	Display freezes/ stops changing **ecf** from *(b)(*i) (Display shows a single number)	1
	(c)		So that you cannot see individual numbers as it cycles, or equivalent	1
				[7]

<table>
<tr><th colspan="3">Question</th><th>Marking details</th><th>Marks Available</th></tr>
<tr><td>5.</td><td>(a)</td><td></td><td>
<table>
<tr><th>$\overline{S}$</th><th>$\overline{R}$</th><th>Q</th><th>$\overline{Q}$</th></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td></tr>
</table>
Setting/resetting correct (lines 2+4) (1)
Latching correct (lines 3+5) (1)
2nd mark can only be awarded if the 1st mark is awarded.</td><td>2</td></tr>
<tr><td></td><td>(b)</td><td></td><td>Resistor and switch in series across power rails with junction connected to $\overline{S}$ (1)
Correct orientation (1)</td><td>2</td></tr>
<tr><td></td><td>(c)</td><td></td><td>LED correct orientation (1)
Use of $\overline{Q}$ to sink current (1)</td><td>2</td></tr>
<tr><td></td><td></td><td></td><td></td><td>[6]</td></tr>
<tr><td>6.</td><td>(a)</td><td></td><td>$\overline{Q}$ connected to D ×3 (1)
then
Q to clock input on the next IC ×2 (1)
and then outputs A,B and C to Q (1)

OR
$\overline{Q}$ to clock input on the next IC ×2 (1)
and then $\overline{Q}$ to outputs A, B and C (1)</td><td>3</td></tr>
<tr><td></td><td>(b)</td><td></td><td>
<table>
<tr><th></th><th>OUTPUT C</th><th>OUTPUT B</th><th>OUTPUT A</th></tr>
<tr><td>Initial State</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>After ONE clock pulse</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>After SIX clock pulses</td><td>0</td><td>0</td><td>1</td></tr>
</table>
Correct outputs for after one clock pulse (1)
Correct output for after five clock pulses (1)</td><td>2</td></tr>
<tr><td></td><td></td><td></td><td></td><td>[5]</td></tr>
</table>

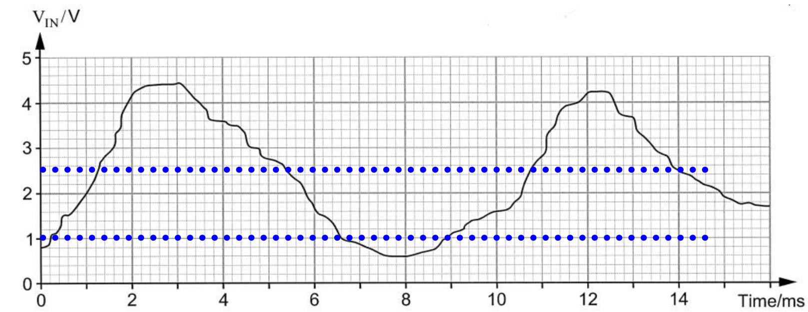
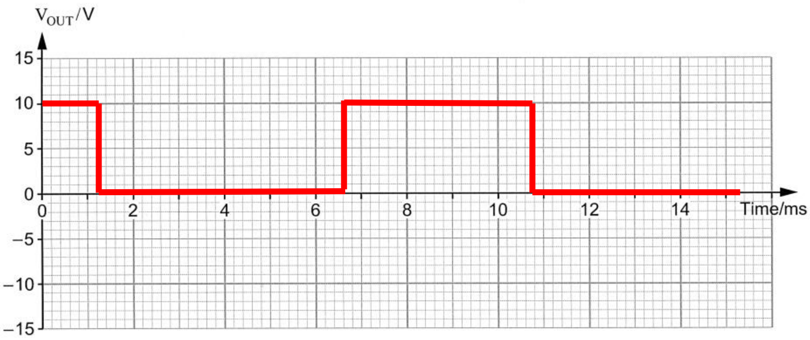
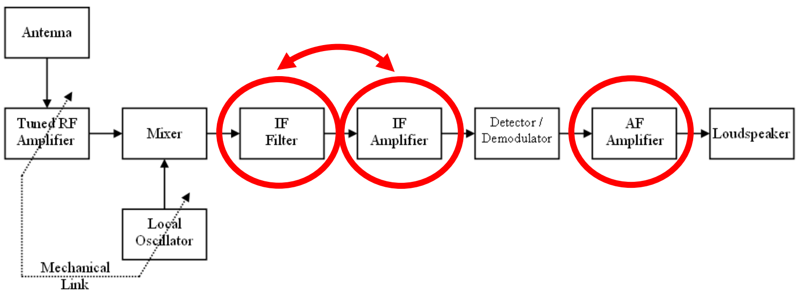
Question			Marking details	Marks Available
7.	*(a)*		68/1+ 1 = **69**	1
	(b)	(i)	135 ± 2 [kPa]	1
		(ii)	V_x = 74 ± 2 [mV] or implied by working (1) 74 × 69 = **5.11** ± **0.16** [V] or **5 106** ± **16** m[V] (1) (**ecf** *(a)* and V_x)	2
	(c)		8.0/69 = 0.1159 V or 115 mV (accept 116 mV) (1) (**ecf** from *(a)*) From graph 115 mV ≡ 172 ± 2 [kPa] (2) (116 mV ≡ 174 ± 2 [kPa])	3
				[7]
8.	*(a)*		Resistor connected between input and inverting input (1) **Variable** resistor connected between output and inverting input (1) Wire connecting non-inverting input and 0 V (1)	3
	(b)	(i)	Resistances in ratio 60:1 with R_F correctly identified (1) Both resistances ≥ 1 kΩ (1)	2
		(ii)	Value for R_{IN} from *(b)* (i) identified as input impedance	1
	(c)		-9/0.2 = - 45 **(minus sign needed)**	1
	(d)		$3.6 \times 10^6/30$ = 120 000 [Hz] **or** 120 k[Hz] **or** 0.12 M[Hz] (substitution 1 mark, answer with multiplier if appropriate 1 mark)	2
	(e)		Inverted graph with slew-rate shape on <u>both</u> edges (1) saturates at -12 V (correct position or labelled) (1) correct starting points and gradients (1) (reaches -12 V saturation at 4.5 μs and 0 V at 11.5 μs)	3
				[12]

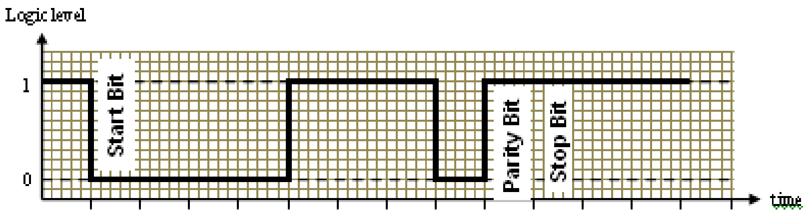
Question			Answers/Explanatory Notes	Marks Available
1.	*(a)*		6 V	1
	(b)		6 V **ecf** from *(a)*	1
	(c)		6 mA **ecf** from *(b)*	1
	(d)		2 kΩ **ecf** from *(a)* & *(c)*	1
	(e)		1 kΩ **ecf** from *(d)*	1
			correct use of Ohm's law this can be awarded from parts *(a), (c)* or *(d)* (shown by a tick in part *(e)*	1
				[6]
2.	*(a)*	(i)	6.75 V (1)	3
		(ii)	0.09 A [90 mA] (1)	
		(iii)	75 Ω (1) **ecf** from *(a)*(i) & (ii)	
	(b)	(i)	Equiv cct and load with **correct values** from part *(a)* (1)	3
		(ii)	voltage drop across R_O = 0.02 × 75 = 1.5 V (1) voltage drop across load = 6.75 – 1.5 = 5.25 V (1) [Accept any other method that makes use of equiv cct] [Apply **ecf** from *(a)* & *(b)*(i)]	
				[6]
3.	*(a)*	(i)	11.3 V (1)	3
		(ii)	[Unsmoothed] positive half cycle pulses (1) Accuracy of peak voltage (1) [Apply **ecf** from part (i)]	
	(b)	(i)	Capacitor in parallel with load (1)	2
		(ii)	Graph with 50 Hz ripple (1) **ecf** from *(a)*(ii)	
	(c)	(i)	10.6 V (1)	2
		(ii)	100 Hz (1)	
				[7]

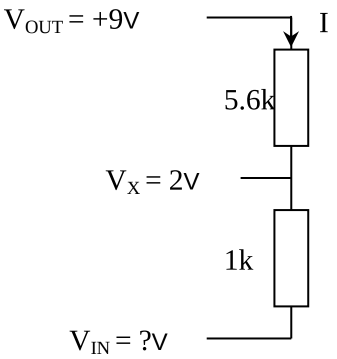
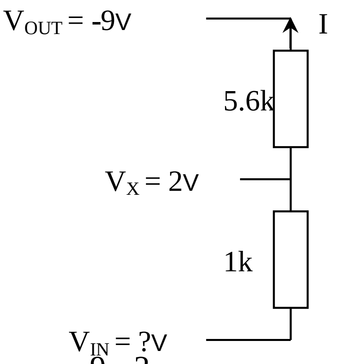
Question			Answers/Explanatory Notes	Marks Available
4.	*(a)*		Substitution/multipliers (1)	2
			Answer in range 32.43 to 32.58 s (1)	
	(b)		Substitution/multipliers (1)	2
			9.7 V (1)	
	(c)		Graph going high at 20 s (1)	2
			Graph going low at approx 53 s (1)	
			[Apply **ecf** from *(a)*]	
				[6]
5.	*(a)*		$V_{IN} = 5 \times 2.3/12.3 = 0.94$ V	1
	(b)	(i)	3.5 V for increasing output (1)	2
			1 V for decreasing output (1)	
			[Allow 1 mark if answers reversed]	
		(ii)	Switching threshold at 3 and 4.5 units on time axis 2 ×(1)	3
			Inverted o/p with amplitude of 5 V (1)	
			[Apply **ecf** from part (i)]	
	(c)		$3 = g_M \times 5$ (1)	2
			$g_M = 0.6$ S (1)	
				[8]

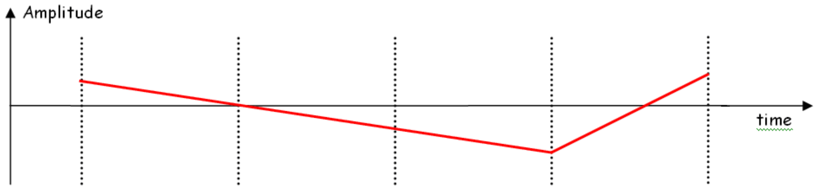
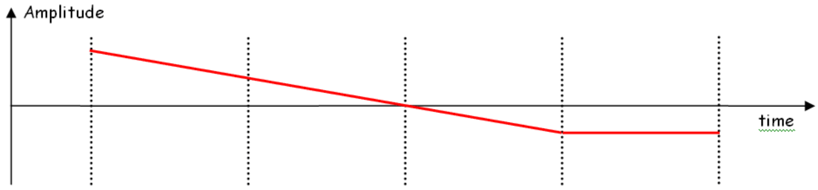
Question			Answers/Explanatory Notes	Marks Available
6.	*(a)*		Correct labels and shape (1) Correct M/S ratio (1)	2
	(b)		$R_B = 13\,k\Omega$ (1) Substitution/multipliers (1)	2
	(c)		$R_A = 26\,k\Omega$ (1) [Apply **ecf** from *(b)*]	1 **[5]**
7.	*(a)*		Voltage across R = 9 V (1) I = 258 mA (1) R = 9/258 mA = 34.88 Ω (1)	3
	(b)		Select 33 Ω to allow for 250 mA load current and 8 mA zener current	1
	(c)	(i)	3 V (1)	4
		(ii)	11.5 V (1)	
		(iii)	$P = 11.5^2/33$ (1) = 4 W (1) [Accept 3.79 W if calculation based on R = 34.88 Ω] [Apply **ecf** from previous parts]	**[8]**
8.	*(a)*	(i)	Both points plotted accurately within ± 1 square with graph linear between points (1)	2
		(ii)	$h_{FE} = 80 \pm 2$ [Apply **ecf** from an inaccurate graph] (1)	
	(b)	(i)	Accept answers in range 4.5 V to 4.6 V (1)	2
		(ii)	6 V ± 0.5 V (1)	
	(c)		V_{load} = 15 – (6 ± 0.5 V) = 9 V ± 0.5 V (1) IC = 9/120 = 0.075 A [75 mA] (1) P = 6 × 0.075 = 0.45W (1)	3 **[7]**

Question			Answers/Explanatory Notes	Marks Available
9.			Two resistors greater than 1 kΩ (1) Ratio resistors 1:3 (1) Larger resistor at top (1) Voltage divider with LDR connected to non inv i/p (1) LDR at bottom (1) Variable resistor (1) Correct transistor and lamp connections (1)	**[7]**
TOTAL				**60**

Question			Marking details	Marks Available
1.	*(a)*	(i)	Inverting	1
		(ii)	1.0 V **and** 2.5 V (any order)	1
	(b)		 	
			Action consistent with part *(a)*	1
			Correct switching thresholds	1
			Correct saturation	1
				[5]
2.	*(a)*		Antenna – Tuned Circuit – Detector/Demodulator – RF Filter - HP	1
	(b)	(i)	480 kHz / 0.48 MHz 3.28 MHz	1 1
		(ii)	480 kHz or 0.48 MHz	1
		(iii)		3
			IF Filter / Amp may be in either order	
				[7]

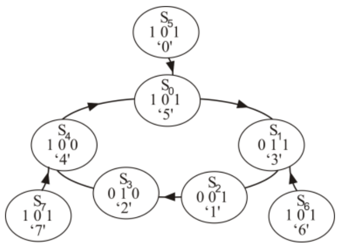
Question			Marking details	Marks Available
3.	*(a)*		 Correct data orientation **and** correct parity bit = 2 Completely reversed data orientation **and** correct parity bit = 1 Correct labels = 1	3
	(b)	(i)	P_4 & P_0 = 1, P_1, P_2 and P_3 = 0 5 correct = 2 / Complete inverse = 1	2
		(ii)	I. Only P_2 fails the parity test	1
			II. D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 | P_4 P_3 P_2 P_1 P_0 1 1 1 0 1 1 0 0 | 1 0 0 0 1	1
				[7]
4.	*(a)*		$\beta = \dfrac{\Delta f_c}{f_i} = \dfrac{60}{20} = 3$ Correct formula + substitution (1) Answer (1)	2
	(b)		$bandwidth = 2(\Delta f_c + f_i) = 2(60+20) = 160\text{kHz}$ *or* $bandwidth = 2(1+\beta)\, f_i = 2(1+3)\times 20 = 160\text{kHz}$ Correct formula + substitution (1) Answer (1) Allow **ecf** for β	2
				[4]

Question				Marking details	Marks Available
5.	*(a)*			$\frac{9-V_{IN}}{6.6}=\frac{9-2}{5.6}$ $9-V_{IN}=\frac{7\times 6.6}{5.6}$ $9-V_{IN}=8.25$ $V_{IN}=9-8.25=0.75\text{V}$ or  $I=\frac{9-2}{5.6\text{k}}=1.25\text{mA}$ $so\quad V_{1k}=1.25\text{mA}\times 1\text{k}=1.25\text{V}$ $\therefore V_{IN}=2-1.25=0.75\text{V}$ correct formula / substitution (1) correct answer (1)	2
	(b)			$\frac{-9-V_{IN}}{6.6}=\frac{-9-2}{5.6}$ $-9-V_{IN}=\frac{-11\times 6.6}{5.6}$ $-9-V_{IN}=-12.96$ $V_{IN}=-9+12.96=3.96\text{V}$ or  $I=\frac{-9-2}{5.6\text{k}}=1.96\text{mA}$ $so\quad V_{1k}=1.96\text{mA}\times 1\text{k}=1.96\text{V}$ $\therefore V_{IN}=2+1.96=3.96\text{V}$ correct formula / substitution (1) correct answer (1)	2 **[4]**

Question			Marking details	Marks Available
6.	*(a)*	i)	Pulse Amplitude Modulation	1
		ii)	 Consistency of Shape (1) Accuracy (1)	2
	(b)	i)	Pulse Width Modulation	1
		ii)	 Consistency of Shape (1) Accuracy (1)	2
				[6]
7.	*(a)*		Minimum frequency = 10 × 8 kHz = 80 kHz	1
			The PISO register must output 10 data bits before the next sample is taken.	1
	(b)		$resolution = \frac{6}{2^{10}} = \frac{6}{1024} = 5.86\,\text{mV}$ correct use of 2^{10} (1) answer (1)	2
	(c)		Schmitt trigger – SIPO – DAC – Low Pass Filter | SIPO Clock SIPO Clock – SIPO = 1 Schmitt – SIPO = 1 SIPO – DAC – LPF = 1	3
				[7]

Question			Marking details	Marks Available
8.	*(a)*	i)	472 kHz	1
		ii)	Use of 0.7 max to determine bandwidth – clearly marked on graph (1) bandwidth = 8 kHz (1)	2
	(b)		$Q = \frac{f_O}{B} = \frac{472}{8} = 59$	1
	(c)		$Q = \frac{2\pi f_0 L}{r_L}$ $L = \frac{Q \times r_L}{2\pi f_o} = \frac{59 \times 0.7}{2 \times \pi \times 472000} = 13.9 \times 10^{-6} = 13.9\mu H$ $L = 14.16\mu H (Q = 60)$ No mark if value of *Q* out of bounds Formula + rearrangement (1) answer (1)	2
	(d)		$C = \frac{1}{4\pi^2 f_o^2 L}$ $C = \frac{1}{4 \times \pi^2 \times 472000^2 \times 13.9 \times 10^{-6}}$ $C = 8.18 \times 10^{-9} = 8.2 nF$ $C = 8.02 nF (L = 14.16\mu H)$ No mark if *L* out of bounds answer	1
	(e)	i)	$R_D = \frac{L}{r_L C}$ $R_D = \frac{13.9 \times 10^{-6}}{0.7 \times 8.18 \times 10^{-9}} = 2427\Omega$ $R_D = 2427\Omega$ If $L = 14\mu H$ and $C = 8nF$ then R_D is 2500 Ω If $L = 14.16\mu H$ and $C = 8.02nF$ then R_D is 2522 Ω No mark if *L* or *C* out of bounds answer	1
		ii)	$I = \frac{8}{2427} = 3.3mA$ $R = \frac{2}{3.3 \times 10^{-3}} = 606\Omega$ or $R = \frac{2427}{4} = 606\Omega$ Substitution in formula (1) answer (1)	2 **[10]**

1. *(a)*



	Main sequence correct	1 mark
	Unused states identified correctly **ecf**	1 mark
	Unused states lead into main sequence (anywhere)	1 mark
(b)	$D_C = B . A$	1 mark
	$D_B = A + \overline{C}$	1 mark
	$D_A = C . B . \overline{A}$ (or equivalents)	1 mark

Total for Q1 **6**

2. *(a)*

	Current Outputs			Next Outputs		
State	**C**	**B**	**A**	**D_C**	**D_B**	**D_A**
0	0	0	0	1	0	1
1	1	0	1	1	0	0
2	1	0	0	1	1	0
3	1	1	0	0	1	0
4	0	1	0	0	0	0
5	0	0	1	1	1	1
6	0	1	1	0	1	0
7	1	1	1	0	0	0

	One mark for each correct data input	3 marks
	C B A correct for eight steps	
	(Main sequence only, and repeated: 1 mark only)	
	C B A correct for six or seven steps only - 1 mark	
	D_C D_B D_A /C, B, A structure correct	
(b)	Unused states – 0 0 1/ 0 1 1 / 1 1 1**(ecf)**	
	All	2 marks
	Any two - 1 mark	
(c)	No stuck states **(ecf)**	1 mark

Total for Q2 **6**

3. *(a)*

```
bsf      STATUS,RP0
movlw    b '11111'
movwf    TRISA
movlw    b 'XXXX0001'
movwf    TRISB
bcf      STATUS,RP0
```

	Correct binary number for TRISA	1 mark
	Correct binary number for TRISB ('X' = any value)	1 mark
(b) (i)	ISR is labelled 'alarm'	1 mark
(ii)	temp. sensor output connected to bit 6	1 mark
(iii)	Clears interrupt flag / allows further interrupts or equivalents	1 mark
	"Bit 1" instead of "…..flag": no marks	
(d) (iv)	LED pulses	1 mark
	Buzzer switches on continuously	1 mark
	until switch on PORT A0 is pressed.	1 mark

Total for Q3 **8**

4.	*(a)*	(i)	Load regulation – output voltage unaffected by load current / resistance	1 mark
		(ii)	Line regulation – output voltage unaffected by supply voltage	1 mark
	(b)	(i)	Non-inverting input voltage = 10.0 V	1 mark
		(ii)	Transistor symbol with base to output of op-amp	1 mark
			Correct connections for collector and emitter	1 mark
		(iii)	V_{OUT} = 12.0 V	1 mark
		(iv)	No change to output voltage	1 mark
			Voltage across 180 Ω resistor increases to 5.5 V (accept increases)	1 mark
			Total for Q4	**8**
5.	*(a)*	(i)	In Gray code, only 1 bit changes at a time. In binary, several bits can change.	1 mark
		(ii)	Binary can give false readings when optoswitches cross a segment boundary.	1 mark
			$G = Y$	1 mark
			$A = X \cdot \overline{Y}$	1 mark
			$R = \overline{X} \cdot \overline{Y}$ (or $\overline{X + Y}$)	1 mark
			Total for Q5	**5**
6.	*(a)*	(i)	Voltage at X falls	1 mark
		(ii)	Voltage at Y falls	1 mark
	(b)	(i)	Voltage at X falls	1 mark
		(ii)	Voltage at Y unchanged	1 mark
	(c)		Circuit must amplify the difference in voltage between X and Y, and ignore absolute size of each such as interference spikes.	1 mark
	(d)		V_{OUT} = +1.25 V	2 marks
			Wrong sign – subtract one mark	
			Total for Q6	**7**
7.	*(a)*	(i)	Diac – correct circuit symbol in series with gate terminal	1 mark
		(ii)	RC network connected correctly	1 mark
			with variable resistor	1 mark
	(b)	(i)	Phase angle = 18^0	1 mark
			Appropriate calculation	1 mark
		(ii)	The bigger the phase angle the dimmer the bulbs.	1 mark
	(c)		Correct shape during positive half-cycle – triggers at 25 V and on afterwards	1 mark
			Correct shape during negative half-cycle – switched off	1 mark
			Total for Q7	**8**
8.	*(a)*	(i)	Optimum voltage gain of P = 10	1 mark
			Gain of Q = 100 ÷ gain of P	1 mark
		(ii)	Correct bandwidth = 2×10^5	1 mark
			allow **ecf** from (i)	
		(iii)	Capacitors block any DC component in signal.	1 mark
	(b)	(i)	Voltage gain = 1	1 mark
		(ii)	Impedance matching between pre-amp and subsequent stage.	1 mark
			Total for Q8	**6**
9.	*(a)*		Correct shape for treble cut filter	1 mark
			Correct low frequency gain (= 20)	1 mark
			Correct break frequency (= 10 kHz)	1 mark
	(b)	(i)	Parallel RC network	1 mark
			RC network in feedback loop and rest of circuit correct	1 mark
			Correct low frequency gain	1 mark
		(ii)	Correct capacitor = 0.1 nF	1 mark
			Appropriate calculation **(ecf)**	1 mark
	(c)	(i)	V_{OUT} = -1.2 V	1 mark
		(ii)	Output 0.7 V smaller than V_{IN}	1 mark
			Horizontal section for V_{IN} between +0.7 V and -0.7 V	1 mark
			Total for Q9	**11**

10.	*(a)*		V_{OUT} = - 0.6 V (wrong sign: no marks)	1 mark
	(b)	(i)	Correct ratio of input resistors (R_B = 150 kΩ, R_A = 300 kΩ)	1 mark
			Feedback resistor = 30 kΩ	1 mark
		(ii)	Correct circuit for inverting amplifier, with input connected	1 mark
			Equal values for feedback and input resistors and both >1 kΩ	1 mark
			Total for Q10	**5**

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