$\frac{\text { WJEC }}{\text { CBAC }}$

## GCE MARKING SCHEME

## ELECTRONICS <br> AS/Advanced

JANUARY

## INTRODUCTION

The marking schemes which follow were those used by WJEC for the January 2013 examination in GCE ELECTRONICS. They were finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conferences were held shortly after the papers were taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conferences was to ensure that the marking schemes were interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conferences, teachers may have different views on certain matters of detail or interpretation.

WJEC regrets that it cannot enter into any discussion or correspondence about these marking schemes.
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ET1 - January 2013

| Question |  |  | Marking details |  |  |  | Marks Available |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1. | (a) <br> (b) | (i) <br> (ii) | One ma <br> EXNOR or ecf for Q <br> Correct symbol for EXN | A <br> 0 <br> 1 <br> 0 <br> 1 <br> or eac <br> ec <br>  <br> gate | S <br> $\mathbf{1}$ <br> $\mathbf{0}$ <br> $\mathbf{0}$ <br> $\mathbf{0}$ <br> allow | $Q$ <br> $\mathbf{1}$ <br> $\mathbf{0}$ <br> $\mathbf{1}$ <br> column <br> from (i) | 3 |
|  |  |  |  |  |  |  | [5] |
| 2. |  |  | $\mathrm{D}_{0}, \mathrm{D}_{3}, \mathrm{D}_{4}$ and $\mathrm{D}_{6}$ to 0 V $\mathrm{D}_{1}, \mathrm{D}_{2}, \mathrm{D}_{5}$ and $\mathrm{D}_{7}$ to 5 V Completely correct (awa Inversion of table (only | $\begin{aligned} & \mathrm{mar} \\ & \mathrm{ark}) \end{aligned}$ |  |  | 2 |
|  |  |  |  |  |  |  | [2] |
| 3. | (a) <br> (b) <br> (c) |  | $\overline{\mathrm{A}} .0=\mathbf{0}$ <br> Two correct groups of 4 Any correct term from gr Simplest overall expressi $$ | tifie s id <br> (1) <br> $\overline{\mathrm{A}} . \mathrm{A}$ | (1) tified $+\overline{\mathrm{B}} \cdot \mathrm{~A}$ | $0+\overline{\mathrm{B}} \cdot \mathrm{~A}=\overline{\mathrm{B}} \cdot \mathrm{~A}$ | $\begin{aligned} & 1 \\ & 3 \end{aligned}$ <br> 3 |
|  |  |  |  |  |  |  | [7] |
| 4. | (a) |  | Each mark for 4 correct Correct clock connection $\overline{\mathrm{Q}}$ to D (1) <br> Q to Resistor/LED (1) | $\overline{\text { necti }}$ |  |  | 3 |
|  | (b) |  | $\mathrm{Q}_{\mathrm{B}}$ and $\mathrm{Q}_{\mathrm{D}}$ connected to AND gate selected and Output of logic gate to $A$ | inpu R te | $\begin{aligned} & \text { logic } \\ & \text { to at } \\ & \text { ninals } \end{aligned}$ | $\begin{aligned} & (1) \\ & 1 \text { reset (1) } \end{aligned}$ | 3 |
|  | (c) | (i) | 6 |  |  |  | 1 |
|  |  | (ii) | 1001 |  |  |  | 1 |
|  |  |  |  |  |  |  | [8] |



| Question |  | Marking details | Marks Available |
| :---: | :---: | :---: | :---: |
| 6. | (a) <br> (b) <br> (c) | Switch and resistor correct orientation across power rails (1) <br> Correct connection to R (1) <br> When the D-type is reset the output Q will be at logic $\mathbf{0}$ and the LED will be ON <br> Both answers needed for the mark <br> Output Q <br> Rises 0 to 1 on first and fourth clock edge (1) <br> Falls 1 to 0 on third clock edge (1) <br> Falls 1 to 0 on edge of reset (1) <br> $\overline{\mathrm{Q}}$ is inverse of $\mathrm{Q}(1)$ | $2$ |
|  |  |  | [7] |
| 7. | (a) <br> (b) <br> (c) <br> (d) | Resistor between input terminal and inverting input (1) <br> Feedback resistor between output and inverting input (1) <br> Non-inverting input to ground (1) $\begin{aligned} & \mathrm{R}_{\mathrm{IN}}=10 \mathrm{k} \Omega(1) \\ & \mathrm{R}_{\mathrm{F}}=1.2 \mathrm{M} \Omega(1) \end{aligned}$ <br> Change $\mathrm{R}_{\mathrm{F}}$ in proportion to $\mathrm{R}_{\mathrm{IN}}$. Don't accept same amount. <br> $50 / \sqrt{2}=35.4$. Line across at 35 approx (1) <br> Bandwidth $=22.5[\mathrm{kHz}](\mathbf{1})$ (Accept $22-23 \mathrm{kHz}$ ) | 3 <br> 2 <br> 1 <br> 2 |
|  |  |  | [8] |


| Question |  |  | Marking details | Marks Available |
| :---: | :---: | :---: | :---: | :---: |
| 8. | (a) <br> (b) <br> (c) <br> (d) | (i) <br> (ii) <br> (iii) <br> (i) | $10 \mathrm{M} \Omega$ <br> Max gain $=100 / 2+1=51$ (1) <br> Min gain $=0 / 2+1=1$ (1) <br> Bandwidth $1.2 \times 10^{6} / 30(1)=40000(1)[\mathrm{Hz}]$ or $40 \mathrm{k}[\mathrm{Hz}]$ <br> or $0.04 \mathrm{M}[\mathrm{Hz}]$ <br> Sine wave with same frequency as original (1) (allow $\pm 1 / 2$ square division) <br> In phase with original (1) <br> Peaks at $12(\mathrm{~V}) 12000 \mathrm{~m}(\mathrm{~V})$ clearly marked on axis or peak (1) <br> $14 / 30=0.47(\mathrm{~V})$ or $467 \mathrm{~m}(\mathrm{~V})$ <br> Time $=14 / 5=2.8(1) \mu \mathrm{s}(1)$ | 2 <br> 2 <br> 3 <br> 1 <br> 2 |
|  |  | (ii) | Reduces distortion for high frequency signals OR Reduces distortion for signals with large voltage swings Or by implication. | 1 [12] |




| Question |  |  | Marking details | Marks Available |
| :---: | :---: | :---: | :---: | :---: |
| 3. | (a) <br> (b) <br> (c) | (i) <br> (ii) <br> (iii) | Antenna - Tuned Circuit - Detector/Demodulator - RF Filter - HP <br> Unable to detect weak stations - poor sensitivity (1) <br> Unable to reject nearby stations - poor selectivity (1) <br> $470 \mathrm{kHz} / 0.47 \mathrm{MHz}$ <br> 1.8 MHz <br> 2.27 MHz <br> $4.07 \mathrm{MHz} \quad 4$ correct $=2$ marks or 3 correct $=1$ mark <br> 470 kHz or 0.47 kHz | 1 <br> 2 <br> 2 <br> 1 <br> 4 <br> [10] |
| 4. | (a) <br> (b) <br> (c) |  | a, b, and d <br> The single parity system cannot distinguish when there are two errors in the data transferred. | 1 |

\begin{tabular}{|c|c|c|c|}
\hline \& stion \& Marking details \& Marks Available <br>
\hline 5. \& (a) \& $$
\begin{array}{lr}
\frac{10-V_{I N}}{10}=\frac{10-4}{7.5} & \\
10-V_{I N}=\frac{6 \times 10}{7.5} & \\
10-V_{I N}=8 & \\
V_{\text {IN }}=10-8 & \\
\mathrm{~V}_{\text {IN }}=2 \mathrm{~V} & \\
\frac{-10-V_{I N}}{10}=\frac{-10-4}{7.5} & \\
-10-V_{I N}=\frac{-14 \times 10}{7.5} & \\
-10-V_{I N}=-18.67 & \\
V_{\text {IN }}=-10+18.67 & \text { correct formula } / \text { substitution (1) } \\
\mathrm{V}_{\text {IN }}=8.67 \mathrm{~V} & \\
& \\
\text { correct answer (1) formula } / \text { substitution (1) } \\
\text { correct answer (1) }
\end{array}
$$ \& 2

2

[4] <br>

\hline 6. \& | (a) |
| :--- |
| (b) |
| (c) |
| (d) | \& | $\begin{aligned} f_{b} & =\frac{1}{2 \pi R C} \\ R & =\frac{1}{2 \times \pi \times 3800 \times 100 \times 10^{-9}} \end{aligned}$ $\mathrm{R}=418.8 \Omega \quad \text { correct formula (1) }$ substitution and multipliers (1) correct answer (1) $\text { Minimum frequency }=12 \times 8 \mathrm{kHz}=96 \mathrm{kHz}(1)$ |
| :--- |
| The PISO register must output 12 data bits before the next sample is taken. (1) $\text { resolution }=\frac{9}{2^{12}}=\frac{9}{4096}=2.197 \mathrm{mV}$ |
| correct use of $2^{12}(1)$ answer (1) |
| Schmitt trigger - SIPO - DAC - Low Pass Filter SIPO Clock |
| SIPO Clock - SIPO (1) |
| Schmitt - SIPO (1) |
| SIPO - DAC - LPF (1) | \& | 3 |
| :--- |
| 2 |
| 2 |
| 3 |
| [10] | <br>

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\end{tabular}

| Question |  |  | Marking details | Marks Available |
| :---: | :---: | :---: | :---: | :---: |
| 7. | (a) | i) | 448 kHz | 1 |
|  |  | ii) | Use of 0.7 max to determine bandwidth. (1) $\text { bandwidth }=10 \mathrm{kHz}(1)$ | 2 |
|  | (b) |  | $\boldsymbol{Q}=\frac{\boldsymbol{f}_{\boldsymbol{o}}}{\boldsymbol{B}}=\frac{448}{10}=44.8$ | 1 |
|  | (c) |  | $\begin{aligned} & \boldsymbol{Q}=\frac{2 \pi f_{0} \boldsymbol{L}}{\boldsymbol{r}_{L}} \\ & \boldsymbol{L}=\frac{\boldsymbol{Q} \times \boldsymbol{r}_{L}}{2 \pi f_{o}} \\ & \boldsymbol{L}=\frac{44.8 \times 0.8}{2 \times \pi \times 448000}=12.7 \times 10^{-6}=12.7 \mu \boldsymbol{H} \\ & \boldsymbol{L}=12.8 \mu \boldsymbol{H}(\boldsymbol{Q}=45) \end{aligned}$ | 1 |
|  | (d) |  | $\begin{aligned} & \boldsymbol{C}=\frac{1}{4 \pi^{2} \boldsymbol{f}_{o}^{2} \boldsymbol{L}} \\ & \boldsymbol{C}=\frac{1}{4 \times \pi^{2} \times 448000^{2} \times 12.7 \times 10^{-6}} \\ & \boldsymbol{C}=9.93 \times 10^{-9}=9.9 \boldsymbol{n} \boldsymbol{F} \\ & \boldsymbol{C}=9.85 n \boldsymbol{F}(\boldsymbol{L}=12.8 \mu \boldsymbol{H}) \end{aligned}$ |  |
|  |  |  | Multipliers (1) <br> Answer (1) | 2 |
|  | (e) | i) | $\begin{aligned} & R_{D}=\frac{L}{r_{L} C} \\ & R_{D}=\frac{12.7 \times 10^{-6}}{0.8 \times 9.9 \times 10^{-9}}=1600 \Omega \\ & R_{D}=1600 \Omega \end{aligned}$ <br> Accept $\mathrm{R}_{\mathrm{D}}(1585-1625 \Omega)$ | 1 |
|  |  | ii) | $\begin{aligned} & \boldsymbol{I}=\frac{10}{1600}=6.25 m \boldsymbol{A} \\ & \boldsymbol{R}=\frac{2}{6.25 \times 10^{-3}}=320 \Omega \\ & \begin{array}{r} \text { or } \end{array} \quad \boldsymbol{R}=\frac{1600}{5}=320 \Omega \\ & \begin{array}{r} \text { Accept } \mathrm{R} \text { in the range }(317-325 \Omega) \end{array} \\ & \begin{array}{r} \text { Substitution in formula (1) } \\ \text { Answer (1) } \end{array} \end{aligned}$ | 2 |
|  |  |  |  | [10] |

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