GCE MARKING SCHEME

ELECTRONICS
AS/Advanced

SUMMER 2013

INTRODUCTION

The marking schemes which follow were those used by WJEC for the Summer 2013 examination in GCE ELECTRONICS. They were finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conferences were held shortly after the papers were taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conferences was to ensure that the marking schemes were interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conferences, teachers may have different views on certain matters of detail or interpretation.

WJEC regrets that it cannot enter into any discussion or correspondence about these marking schemes.

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ET2	6
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ET5	16

GCE Electronics – ET1

Summer 2013

<table>
<tr><th colspan="3">Question</th><th>Marking details</th><th>Marks Available</th></tr>
<tr><td>1</td><td>(a)</td><td></td><td>
<table>
<tr><td>B</td><td>A</td><td>S</td><td>T</td><td>Z</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
</table>
One mark each correct column (allow ecf for Z)

(b) Logic gate EXOR (allow ecf from Z)
</td><td>3

1</td></tr>
<tr><td></td><td></td><td></td><td></td><td>[4]</td></tr>
<tr><td>2.</td><td>(a)</td><td>(i)
(ii)</td><td>NAND Gate

Q = $\overline{A.B}$ or Q = $\overline{A} + \overline{B}$ or allow 3 term answer</td><td>1

1</td></tr>
<tr><td></td><td>(b)</td><td>(i)
(ii)

(iii)</td><td>EX-NOR ; EXNOR ; XNOR

<table>
<tr><td>D</td><td>C</td><td>P</td></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
</table>
P = $\overline{D \oplus C}$ or P = $\overline{D}.\overline{C}$ + D.C allow ecf from (ii)</td><td>1

1

1</td></tr>
<tr><td></td><td></td><td></td><td></td><td>[5]</td></tr>
</table>

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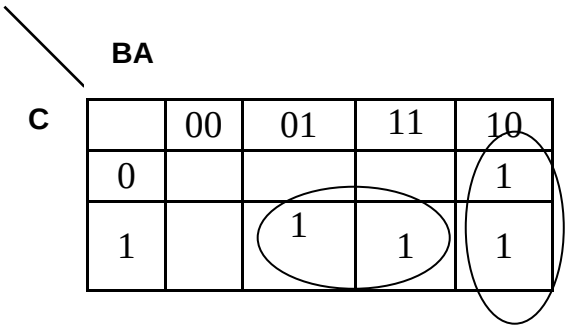
Question			Marking details	Marks Available
3	*(a)*			

C	B	A	**Q**
0	0	0	**0**
0	0	1	**0**
0	1	0	**1**
0	1	1	**0**
1	0	0	**0**
1	0	1	**1**
1	1	0	**1**
1	1	1	**1**

Column Q correct — 1

(b)



1

$Q = B.\overline{A} + C.A$ — 2

1 mark correct map and groups
1 mark each correct term allow **ecf** from map

Correct Boolean algebra solution = 3 marks
-1 mark if 3 terms present

(c)

method 1

$\overline{\overline{A} + \overline{B} + \overline{A}.B}$

$A.B + A + \overline{B}$

$A.(B + 1) + \overline{B}$

$A + \overline{B}$

or method 2

$\overline{\overline{A}.A.B + \overline{B}.A.B}$

$A + \overline{B}$

1 mark correct answer
2 marks for clearly shown correct working. — 3

[7]

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Question			Marking Details	Marks Available
4.	*(a)*	(i)	B to NOT gate (1) NOT gate to AND's with A and C (both correct) (1) AND's to OR gate to Q (1)	3
		(ii)	Correct replacement NOT by NAND (1) Correct replacement AND by NAND **(both required) (1)** Correct replacement OR by NAND (1) Allow **ecf** from (i)	3
		(iii)	Two correct redundancies ***clearly*** identified	2
	(b)		6 (NAND gates required)	1
				[9]
5.	*(a)*	(i)	Binary **(0) 1111011**	1
		(ii)	BCD **0001 0010 0011**	1
	(b)		Fewer <u>bits</u> required (for binary) or equivalent	1
				[3]

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<table>
<tr><th colspan="3">Question</th><th>Marking Details</th><th>Marks Available</th></tr>
<tr><td>6.</td><td>(a)</td><td></td><td>All clock pulse correct (1)
All Q's to output flags (1)
All $\overline{Q}$'s to D's (1)</td><td>3</td></tr>
<tr><td></td><td>(b)</td><td>(i)</td><td>A and D to inputs of AND P (1)
Output of P to R (1)</td><td>2</td></tr>
<tr><td></td><td></td><td>(ii)</td><td>3 (allow 6)</td><td>1</td></tr>
<tr><td></td><td></td><td>(iii)</td><td>
<table>
<tr><th>Clock Pulse</th><th>D</th><th>C</th><th>B</th><th>A</th><th>Q</th><th>W</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>3</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>4</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>5</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>6</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>7</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>8</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>9</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
</table>
One mark for each correct column Q and W (0-8) (2)
Line for clock pulse 9 correct (wrt answer in table) (1)</td><td>3</td></tr>
<tr><td></td><td></td><td>(iv)</td><td>ON for 3 seconds, OFF for 1 second, repeated
Completely correct 2 marks, One error 1 mark
Allow ecf from (iii)</td><td>2</td></tr>
<tr><td></td><td></td><td></td><td></td><td>[11]</td></tr>
</table>

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Question			Marking details	Marks Available
7.			B starts at logic 1 (1) B **falls** to logic zero at 50 ns (1) Q is 30 ns pulse/notch (1) Q positive pulse between 30 and 60 ns (1)	4
				[4]
8.	*(a)*		-60 (minus sign and value needed, ignore units)	1
	(b)	(i)	V_{OUT} inverted version of V_{IN} (1) Peaks at ± 10 V (1) Peaks, troughs and intercepts on time axis correct (1)	3
		(ii)	Inverted graph of input with same time axis intercepts (1) Clipping shown at ± 14 V (1)	2
				[6]
9.	*(a)*	(i)	Y faster slew rate (or equivalent) **Both needed**	1
		(ii)	$\frac{2.5x10^6}{500}$ = 5000 [Hz] or 5 k[Hz] or 0.005 M[Hz]	1
	(b)	(i)	Feedback resistor between output and inverting input (1) Resistor between inverting input and 0 V (1) Input terminal to non-inverting input (1)	3
		(ii)	Resistors in ratio **79:1** (1) Resistors correctly identified **and** both 1 kΩ or greater (less than 10 MΩ) (1)	2
	(c)		Horizontal line at gain = 80 for low frequency (1) Sloping line passing through point (24, 56) (1)	2
	(d)		Slew rate = $\frac{12}{4.8}$ = 2.5 (1) V μs^{-1} (1)	2
				[11]

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GCE Electronics: Unit ET2

Summer 2013

Question			Answers/Explanatory Notes	Marks Available
1	(a)	(i)	6 V (1)	3
		(ii)	3 mA (1)	
		(iii)	2.4 mA (1)	
	(b)		Voltage across resistors = 8.3 V (1) Voltage across each 1k Ω resistor = 4.15 V (1) V_{OUT} = 4.85 V (1)	3 **[6]**
2.	(a)	(i)	X low, Y high (1)	2
		(ii)	X high, Y low (1) [allow 1 mark if answers to (i) and (ii) are reversed]	
	(b)		Buzzer between 9 V supply and Y [**ecf** from (a)(ii)]	1
	(c)		To prevent false switching e.g. due to changes in ambient light	1 **[4]**
3.	(a)	(i)	R = 4 V /15 (1) R = 267 Ω (1)	
		(ii)	270 Ω (1)	3
	(b)	(i)	Diode across LED (1) and in inverse parallel (1)	
		(ii)	accept range 133 Ω to 135 Ω (1) [allow **ecf** from (a)]	3 **[6]**
4.	(a)		10 s	1
	(b)	(i)	Substitution/multipliers (1) 6.9 s (1)	2
		(ii)	Substitution/multipliers (1) 0.81 V (1)	2
		(iii)	50 s	1
	(c)	(i)	Appropriate scales (1) Quality/accuracy of curve (1)	
		(ii)	11 s [accept range 10 - 12 s] (1) [allow **ecf** from (b)]	3 **[9]**

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Question			Answers/Explanatory Notes	Marks Available
5.	(a)		4.24 V (1) 4.6 V (1)	2
	(b)	(i) (ii)	Graph with horizontal line just below peak (1) Voltage label showing peak at 4.6 V (1) [allow **ecf** from (a)]	2
	(c)		Graph showing large (1) Full wave output (1)	2
	(d)	(i) (ii)	Increases (1) 50Hz (1)	2 **[8]**
6.	(a)		Switch and resistor in trigger cct (1) Switch at bottom (1)	2
	(b)		Relay between pin 3 and 0 V rail (1) NO contact /connections in secondary cct (1) [accept relay connected to 15 V rail with NC contact]	2
	(c)		T = 300 s (1) substitution into formula/multipliers (1) 1.24 MΩ (1)	3 **[7]**
7.	(a)		Substitution/rearranging formula (1) g_M = 1.875 S (1)	2
	(b)		zero [accept answers less than 0.1 mA]	1
	(c)		gives low power consumption in the MOSFET	1 **[4]**

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Question			Answers/Explanatory Notes	Marks Available
8.	(a)	(i)	I_c = 1 A	1
		(ii)	I_B = 1/250 = 0.004 = 4 mA	1
		(iii)	Voltage across base resistor = 4 V (1) R_B= 4 V/4 mA = 1 kΩ (1)	2
	(b)		Thermistor and variable resistor in input cct (1) Thermistor at bottom (1)	2
	(c)		When I_B = 4 mA, voltage across 700 Ω resistance = 700 x 4 mA = 2.8 V (1) V_B = 7.2 - 2.8 = 4.4 V (1) This shows that when the base current is 4 mA the input voltage is insufficient to saturate the transistor (1) [allow **ecf** from (a)]	3 **[9]**
9.	(a)	(i)	12 – 5.1 = 6.9 V (1) 6.9/15 = 0.46 A = 460 mA (1)	2
		(ii)	5.1 x 0.46 (1) = 2.3 W (1) **ecf** from (i)	2
	(b)		460 – 10 = 450 mA [allow **ecf** from (a)]	1
	(c)	(i)	9.2 V (1)	
		(ii)	5.1 V (1)	2 **[7]**
TOTAL				**60**

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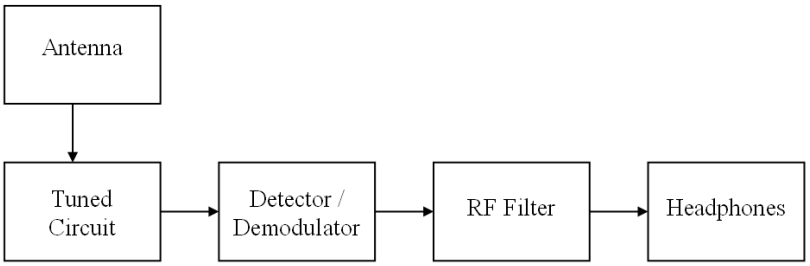
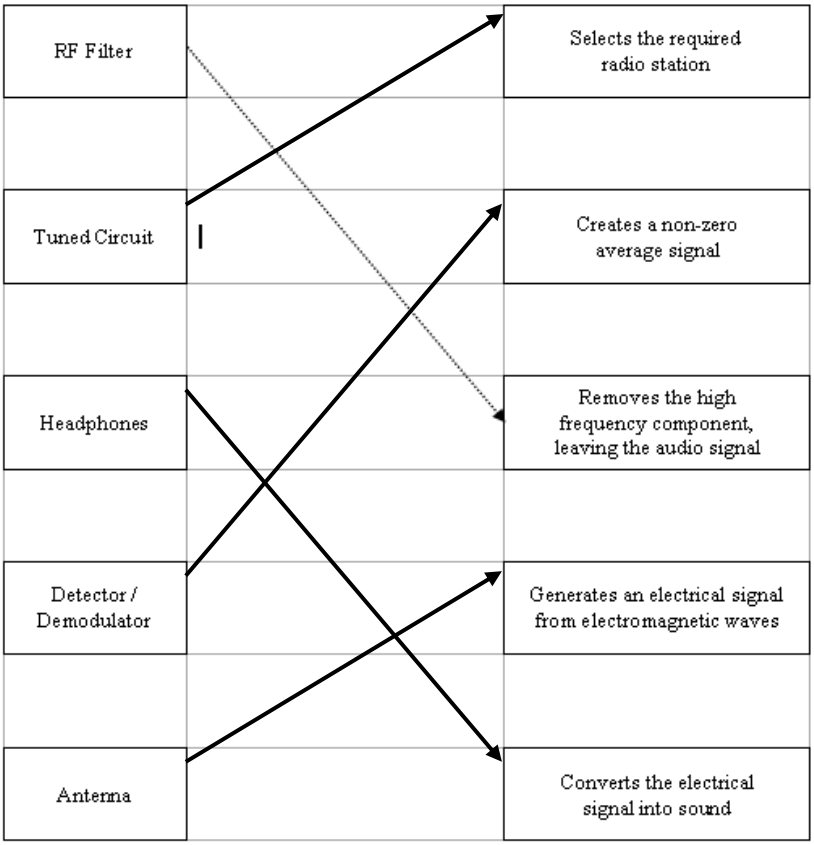
GCE Electronics – ET4

Summer 2013

Question			Marking details	Marks Available
1.	*(a)*			1
	(b)		 4 Correct links – 2 marks or Any two correct links – 1 mark	2 **[3]**

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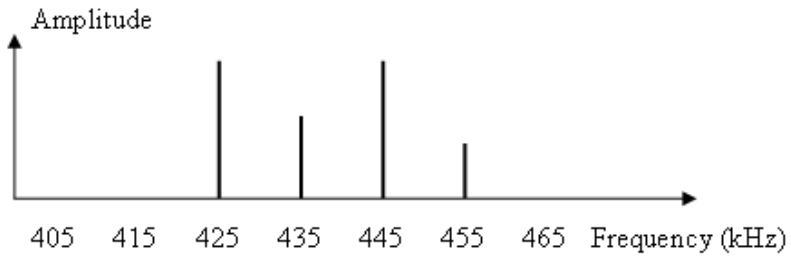
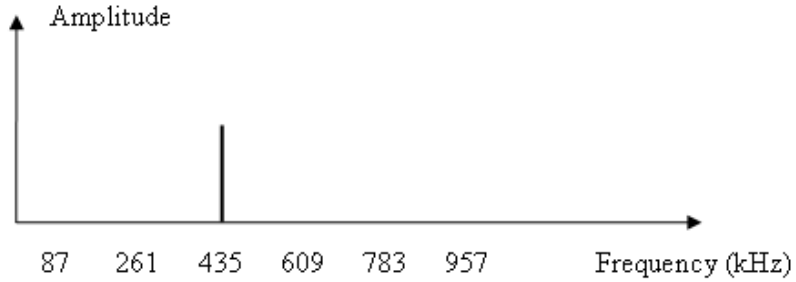
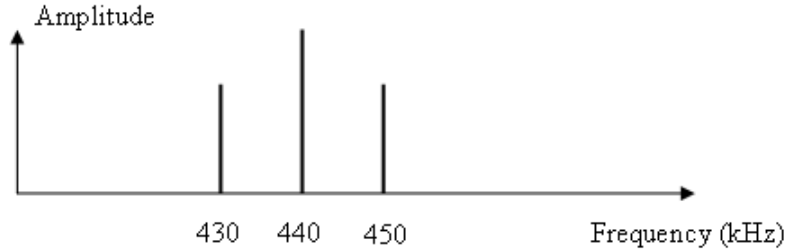
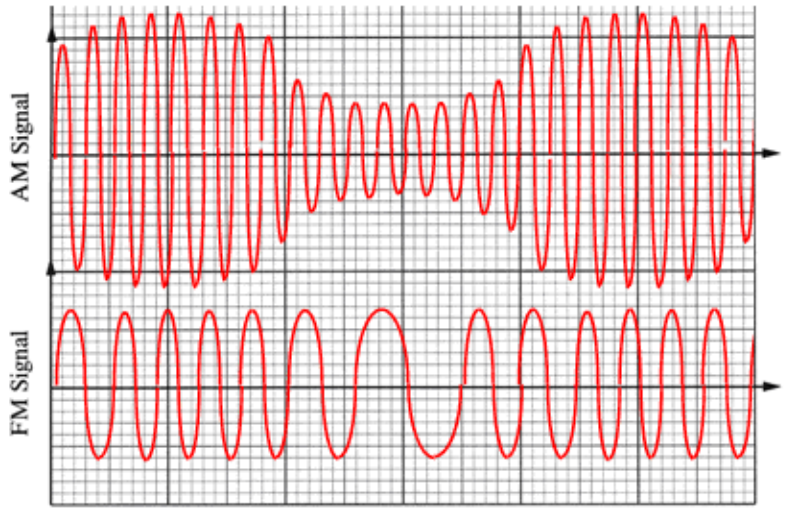
Question			Marking details	Marks Available
2.	*(a)*		Band Pass Filter	1
	(b)			1
	(c)			1
	(d)			1 **[4]**
3.	*(a)*		 For AM – indication of varying amplitude with an attempt at constant frequency required. For FM – indication of constant amplitude and varying frequency.	1 1

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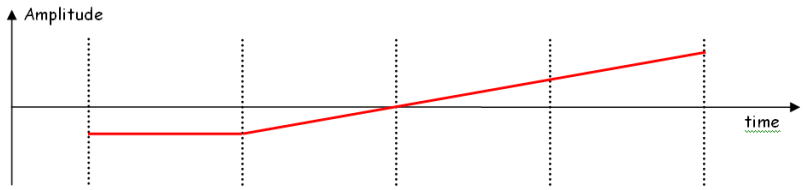
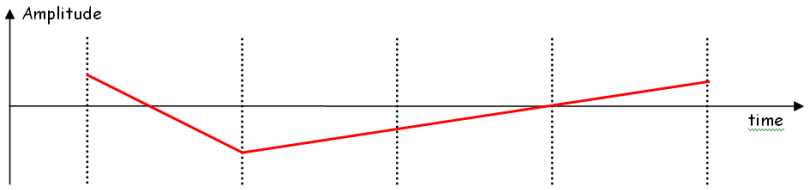
Question			Marking details	Marks Available
3.	*(b)*	(i)	$\beta = \frac{\Delta f_c}{f_i} = \frac{100}{20} = 5$	1
		(ii)	$Bandwidth = 2(1+\beta) f_i$ $= 2(1+5)20kHz$ $= 240kHz$ or $Bandwidth = 2(\Delta f_c + f_i)$ $= 2(100+20)$ $= 240kHz$	1 1 or 1 1 **[5]**
4.	*(a)*	(i)	Pulse Width Modulation (1)	
		(ii)	 Consistency of Shape (1) Accuracy (1)	3
	(b)	(i)	Pulse Amplitude Modulation (1)	
		(ii)	 Consistency of Shape (1) Accuracy (1)	3 **[6]**

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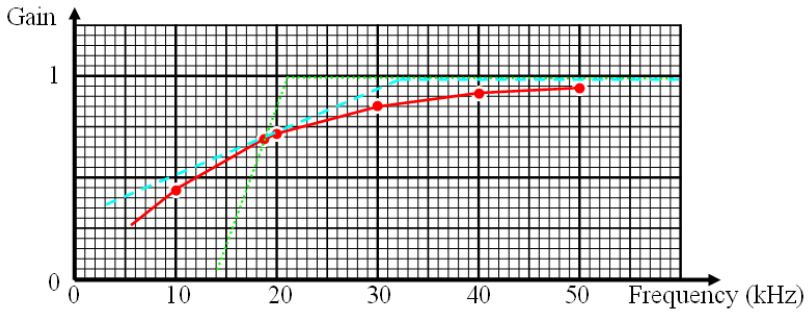
Question			Marking details	Marks Available
5.	*(a)*		High Pass Filter	1
	(b)		$X_C = \frac{1}{2\pi fC}$ $= \frac{1}{2\pi \times 1000 \times 47 \times 10^{-9}}$ $= 3386\Omega$ substitution **and** multipliers = 1 correct answer = 1	2
	(c)		33.86 Ω or (b) ÷ 100.	1
	(d)		$f_b = \frac{1}{2\pi RC}$ $f_b = \frac{1}{2 \times \pi \times 180 \times 47 \times 10^{-9}}$ $f_b = 18.812kHz$ substitution **and** multipliers = 1 correct answer = 1	2
	(e)		 Shape consistent with (a)(1) Break frequency consistent at 70% point with (d) (18.8 kHz)(1) {Red line gives true response – accept 2 line approx. between limits shown but must pass through 70% value}	2
				[8]

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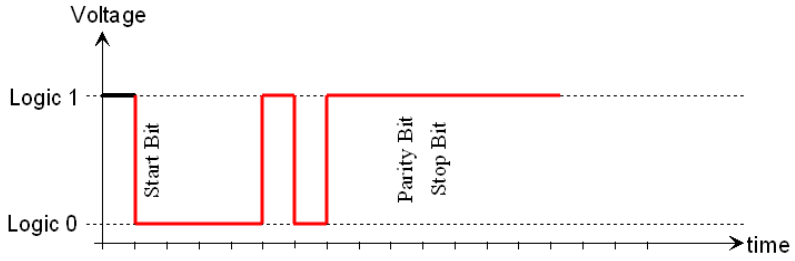
Question			Marking details	Marks Available
6.	*(a)*	(i)	Parity bit = 1	1
		(ii)	 Data reversed and correct = 2 marks or Data correct but not reversed = 1 mark All three labels correct = 2 marks or Any two labels correct = 1 mark	4
	(b)	(i)	<table><tr><td>D_7</td><td>D_6</td><td>D_5</td><td>D_4</td><td>D_3</td><td>D_2</td><td>D_1</td><td>D_0</td><td>P_4</td><td>P_3</td><td>P_2</td><td>P_1</td><td>P_0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr></table> All five correct = 2 marks Four correct = 1 mark	2
		(ii)	<table><tr><td>D_7</td><td>D_6</td><td>D_5</td><td>D_4</td><td>D_3</td><td>D_2</td><td>D_1</td><td>D_0</td><td>P_4</td><td>P_3</td><td>P_2</td><td>P_1</td><td>P_0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr></table>	1
			The only parity bits to fail are P_1 and P_4, the only bit affected by an error in these two parity bits is D_7, so this is where the error is located.	1
				[9]

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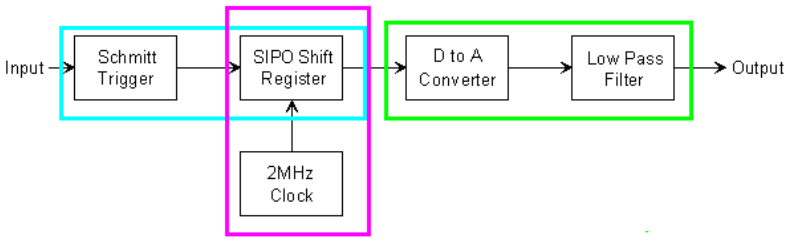
Question			Marking details	Marks Available
7.	*(a)*	i)	Block X = Sampling Gate	1
		ii)	Block Y = PISO Shift Register	1
		iii)	Block Z = PISO Clock, 800 kHz Clock, High Frequency Clock (Do not accept just Clock)	1
	(b)	i)	$2^{16} = 65\ 536$	1
		ii)	The highest frequency present at the input is 20 kHz (Audio Signal). Nyquist's sampling theorem states that sampling frequency must be at least 2x highest input frequency, = 36 kHz, therefore 50 kHz	1
	(c)		 All 3 Correct = 2 marks 2 Correct = 1 mark	2
	(d)	i)	 -1 for each error Minimum of 0 marks Maximum of 2	2
		ii)	I. Low pass filter (1) II. Digital to analogue converter (1)	2
				[11]

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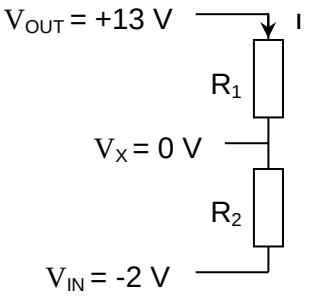
Question			Marking details	Marks Available
8.	*(a)*		V_{REF} is set at 0 V, (therefore it does not matter whether V_{OUT} is at +13 V or -13 V, the voltage drop across R_1 is the same)	1
	(b)		 $I = \frac{13-0}{R_1} = \frac{13}{R_1}$ *and* $I = \frac{0-(-2)}{R_2} = \frac{2}{R_2}$ The current I is the same so we can equate these equations. $\frac{13}{R_1} = \frac{2}{R_2}$ $\frac{13R_2}{2} = R_1$ $6.5R_2 = R_1$ e.g. R_1 = 6.5k, R_2 = 1k R_1 = 13k, R_2 = 2k etc OR $V_{R_1} : V_{R_2}$ $13 : 2$ $6.5 : 1$ $\therefore R_1 : R_2$ $\therefore 6.5 : 1$ R_1 = ...65k..... R_2 = ...10k..... Calculation of ratio = 2 marks Correct resistors >1k = 1 mark	3 **[4]**

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GCE Electronics – ET5

Summer 2013

1. *(a)* Three states in the main sequence 1

(b) (i) Unused states - do not form part of the main sequence 1

(ii) Stuck state – one that never progresses into the main sequence 1

(c) (i) One of S_5 / S_6 / S_7. 1

(ii) Two stuck states – S_3 and S_4 (both needed to get mark.) 1

(iii) Stuck states can be a problem on power-up or system reset. 1

Total for Q1 [6]

2. *(a)*

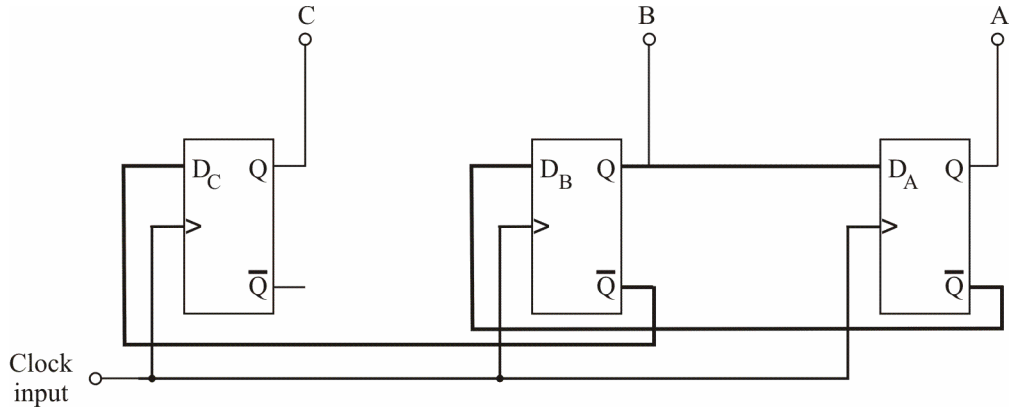
	Current Outputs			Next Outputs		
State	**C**	**B**	**A**	**D_C**	**D_B**	**D_A**
0	1	0	0	1	1	0
1	1	1	0	0	1	1
2	0	1	1	0	0	1
3	0	0	1	1	0	0
4	0	0	0	1	1	0
5	0	1	0	0	1	1
6	1	0	1	1	0	0
7	1	1	1	0	0	1

Main sequence identified (1)
Unused states identified (1)
Correct progression for main sequence (1)
Correct progression for unused states (1) 4

(b)

$D_C = \underline{B}$ or **ecf** from table (1)
$D_B = \overline{A}$ or **ecf** from table (1)
$D_A = B$ or **ecf** from table (1) 3

(c)



Correct clock connections (1)
D_C correct or **ecf** from part (b) (1)
D_B correct or **ecf** from part (b) (1)
D_A correct or **ecf** from part (b) (1)
Use of Q bar instead of NOT gates (1) 5

Total for Q2 [12]

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3. *(a)* PORT A: bit 2 is an input; all others are outputs (1) 2
PORT B: all bits are inputs (1)

(b) movlw b '1 X X 1X X X X' (X = 'don't care') 1

(c)

```
101   alarm   movwf   Wtemp,1
102           bcf     INTCON,1
103           bsf     PORTA,4
104           bsf     PORTA,3
105           call    fivesec
106           clrf    PORTA
107           movf    Wtemp,0
108           retfie
```

All seven commands complete / correct 4 marks 4
Any five ..... 3 marks only
Any three ..... 2 marks only
Any one ..... 1 mark only

(d) Working register may be used, and hence contents changed, in ISR 1

Total for Q3 [8]

4. *(a)* (i) Voltage at X = 0.75 V 1
(ii) Y indicates whether the analogue input voltage exceeds the input voltage range. 1

(b) (i) Resolution = 0.25 V 1
(ii) Reference voltage = 2 V 1
(iii) Resistor chain will contain 8 resistors 1

(iv)

Inputs							Outputs		
P	**Q**	**R**	**S**	**T**	**U**	**V**	**C**	**B**	**A**
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	1	1
1	1	1	1	0	0	0	1	0	0
1	1	1	1	1	0	0	1	0	1
1	1	1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1	1	1

Comparator outputs P to V correct (2)
Pattern reversed, or use of saturation voltages, subtract one mark
Binary outputs CBA correct (1) 3

Total for Q4 [8]

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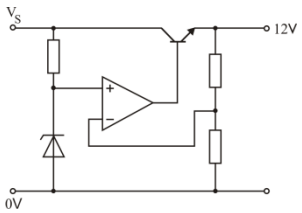
5. *(a)* One strain gauge is under different strain from the other. 1

(b) (i) Voltage at P = 5.42 V 1
(ii) Voltage at Q = 5.45 V 1
(iii) Voltage gain of difference amplifier = 41 1
(iv) V_{OUT} = -1.23 V 2
Incorrect sign – subtract one mark

(c) Both strain gauges are exposed to same temperature, and so output of bridge is unaffected by temperature variation 1

(d)



Zener diode + resistor, with correct symbols and orientation (1)
Emitter follower, with correct symbols and orientation (1)
Correct connections to op-amp (1) 3

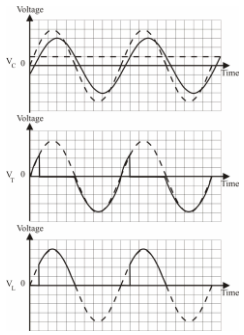
Total for Q5 [10]

6. *(a)* Gate – must receive a sufficient positive pulse of current, or equivalent 1

(b) Holding current – minimum anode/cathode current needed to maintain latching 1

(c) (i) Diac – correct circuit symbol in series with gate terminal 1
(ii) Phase shift = $\tan^{-1}(R/X_C)$
Evidence of correct interpretation of multipliers and/or X_C (1) 2
$= 25.2^0$ (1)

(iii)



For V_C – sinusoidal with phase lag (1) 5
– correct alignment to firing voltage (1)
For V_T – correct shape (1)
For V_L – correct shape (1)
$V_T + V_L = V_S$ (1)

Total for Q6 [10]

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7. *(a)* Filter = bass cut 1

(b) Break frequency = 260.5 Hz
Use of 13 kΩ resistor (1) 3
Evidence of correct interpretation of multipliers (1)
Correct answer (1)

(c) Correct shape, allowing **ecf** from *(a)*(1) 3
Correct break frequency, allowing **ecf** from *(b)*(1)
Correct gain on horizontal portion (= 30) (1)

Total for Q7 [7]

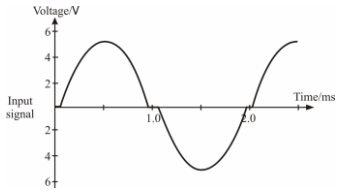
8. *(a)* Link Z only 1

(b) $R_1 = R_2$ 1

(c) (i) Max power dissipation = 9 W 1

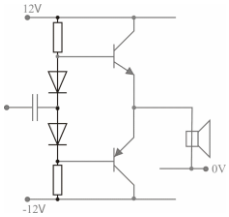
(ii) Zero, or reduced, power dissipation when signal = 0 1

(iii)



Amplitude = 5.3 V (1) 3
Evidence of crossover distortion (1)
Correct crossover distortion - horizontal curve between -0.7 and +0.7 V (1)

(iv)



Four components as shown (1) 2
Correct orientation (1)

Total for Q8 [9]

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