Surname	Centre Number	Candidate Number
Other Names		2

GCE AS/A level

1141/01

ELECTRONICS – ET1

A.M. TUESDAY, 14 May 2013

1¼ hours

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**4**	
2.	**5**	
3.	**7**	
4.	**9**	
5.	**3**	
6.	**11**	
7.	**4**	
8.	**6**	
9.	**11**	
Total	**60**	

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ADDITIONAL MATERIALS

In addition to this examination paper, you will need a calculator.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The total number of marks available for this paper is 60.

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

You are reminded to show all working. Credit is given for correct working even when the final answer given is incorrect.

INFORMATION FOR THE USE OF CANDIDATES IN ET1

Preferred Values for resistors

The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

Standard Multipliers

Prefix	Multiplier
T	$\times 10^{12}$
G	$\times 10^{9}$
M	$\times 10^{6}$
k	$\times 10^{3}$

Prefix	Multiplier
m	$\times 10^{-3}$
μ	$\times 10^{-6}$
n	$\times 10^{-9}$
p	$\times 10^{-12}$

Operational amplifier

$$G = -\frac{R_F}{R_{IN}}$$

$$G = 1 + \frac{R_F}{R_1}$$

$$\text{Slew Rate} = \frac{\Delta V_{OUT}}{\Delta t}$$

Boolean identities

$$A + \overline{A}.B = A + B$$

$$A.B + A = A.(B+1) = A$$

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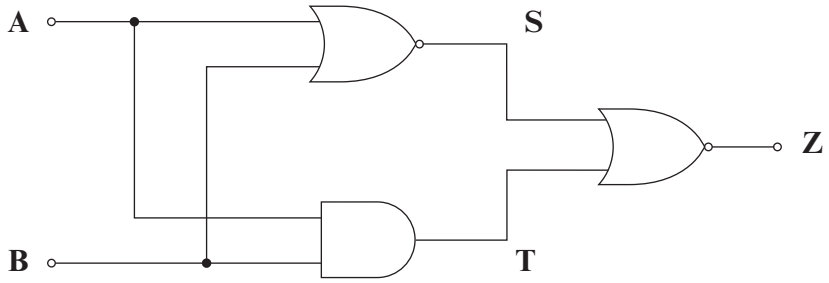
1. The system below uses three logic gates.



(a) Complete the truth table for this system. [3]

B	A	S	T	Z
0	0			
0	1			
1	0			
1	1			

(b) Name the single gate that would produce output Z. [1]

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2. *(a)* The truth table for a logic gate is shown below.

B	A	Q
0	0	1
0	1	1
1	0	1
1	1	0

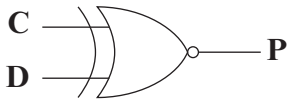
(i) What logic gate produces this truth table?

.....

(ii) Write down the Boolean expression for the output Q in terms of A and B. [2]

Q = ...

(b) The logic gate shown here has inputs C and D and output P.



(i) State the name of this gate.

.....

(ii) Complete the truth table for this gate.

D	C	P
0	0	
0	1	
1	0	
1	1	

(iii) Write down the Boolean expression for the output P in terms of C and D. [3]

P = ...

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3. A logic system behaves according to this Boolean expression.

$$Q = C.\overline{B}.A + C.B + \overline{C}.B.\overline{A}$$

(a) Complete the truth table for this system. [1]

C	B	A	Q
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

(b) Use a Karnaugh map or Boolean algebra to simplify the expression for Q. [3]

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C \ BA	00	01	11	10
0				
1				

(c) Apply DeMorgan's theorem to the following expression **and** simplify the result. [3]

$$Q = \overline{(\overline{A} + \overline{B}).(\overline{A}.B)}$$

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4. *(a)* (i) Without simplification draw the circuit diagram for the following expression. Use only AND, OR and NOT gates. [3]

$$Q = C.\overline{B} + \overline{B}.A$$

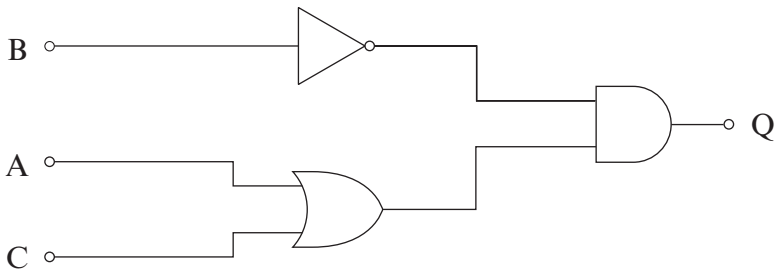
(ii) Draw the NAND gate equivalent circuit. [3]

(iii) Cross out **all** redundant gates. [2]

(b) The original equation can be rewritten as:

$$Q = \overline{B} .(C + A)$$

with the corresponding circuit diagram drawn below:



What is the least number of NAND gates needed to build this version of the circuit? (Hint: Drawing the circuit diagram may help you to work out your answer.) [1]

Least number of gates required = ...

5. *(a)* Convert the number 123 into:

(i) Binary .....

(ii) BCD ..... [2]

(b) In counting systems that do not require the number to be displayed why would using binary counters be an advantage compared to using BCD counters? [1]

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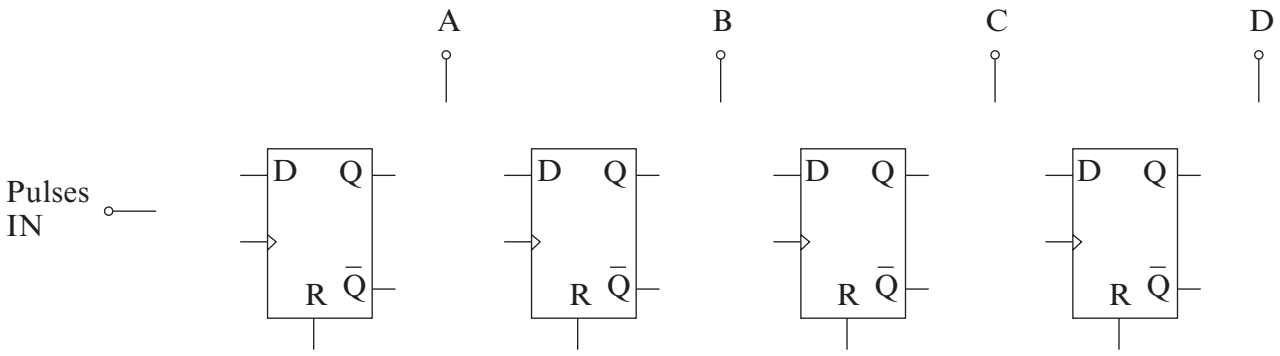
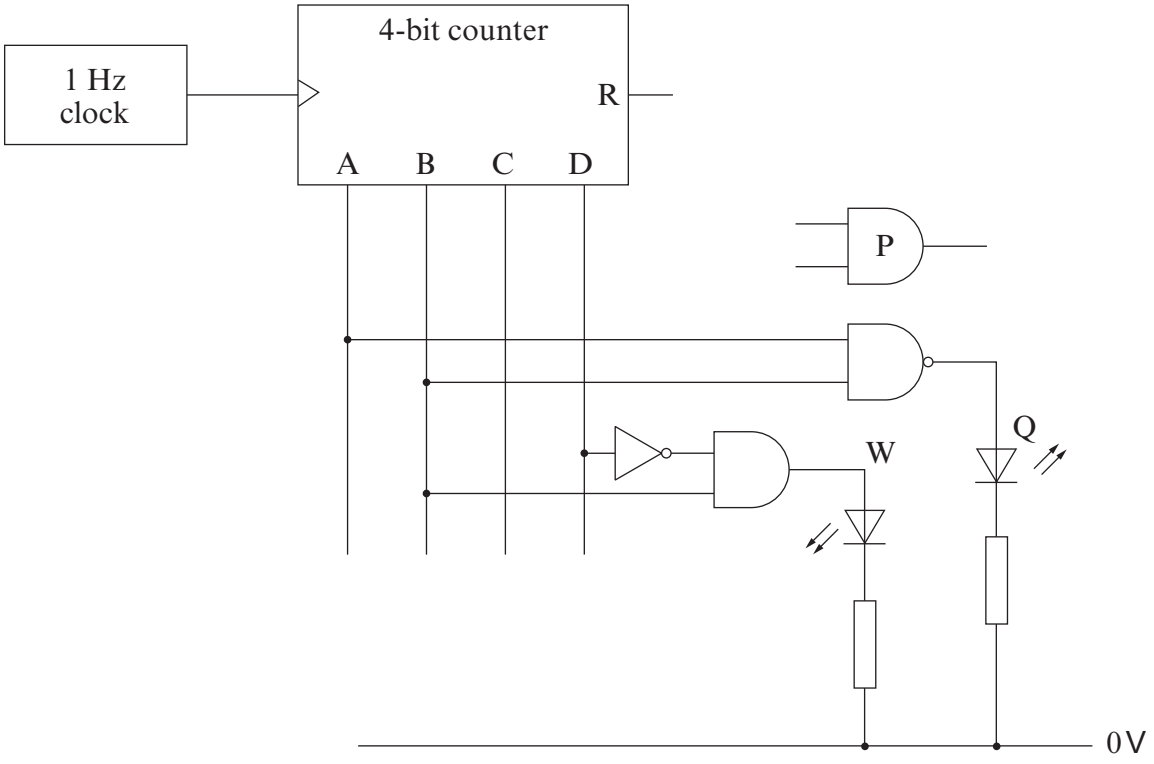
6. *(a)* Complete the diagram to make a 4 bit up-counter where A is the least significant bit. [3]



(b) A student designs a light sequencer using the 4-bit counter. The diagram below shows a 1 Hz clock feeding pulses into the counter.

(i) Complete the diagram to make a counter that resets on the 9th pulse (modulo-9) using logic gate P. [2]



(ii) How many times does counter output A change in the first 6 seconds? [1]

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(iii) Complete the truth table for the light sequencer. [3]

Clock Pulse	D	C	B	A	Q	W
0	0	0	0	0		
1	0	0	0	1		
2	0	0	1	0		
3	0	0	1	1		
4	0	1	0	0		
5	0	1	0	1		
6	0	1	1	0		
7	0	1	1	1		
8	1	0	0	0		
9						

(iv) Describe what happens to LED Q over a period of 8 seconds. [2]

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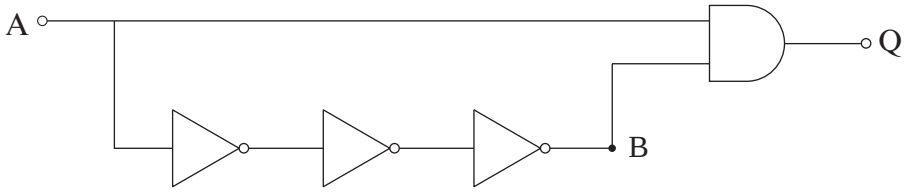
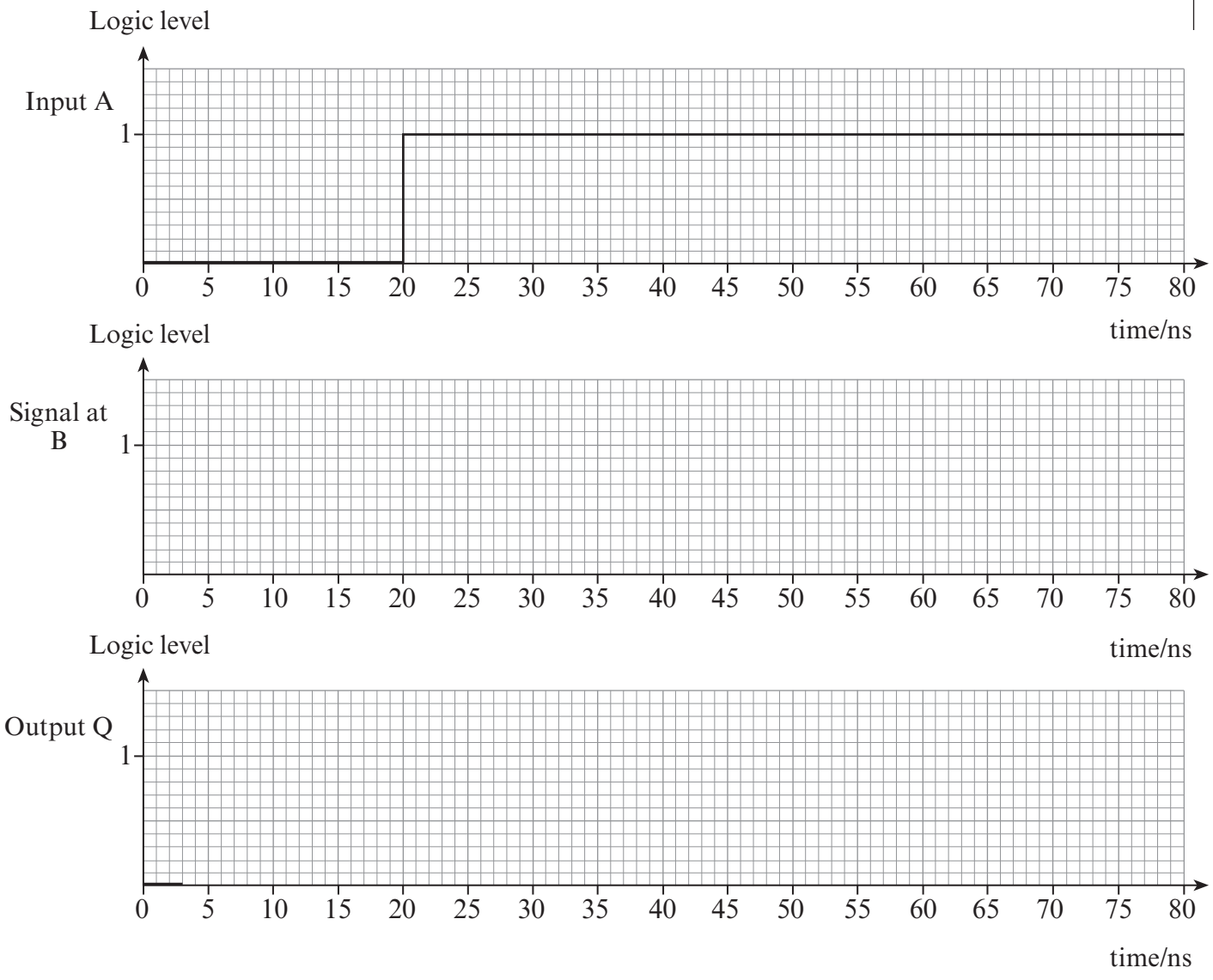
7. The following diagram shows the circuit for a *transition gate*.
Each logic gate has a propagation delay of 10 ns.



Complete the following diagram to show how the signal at B and output Q change when the pulse shown is applied to input A.
Initially, output Q is at logic 0. [4]



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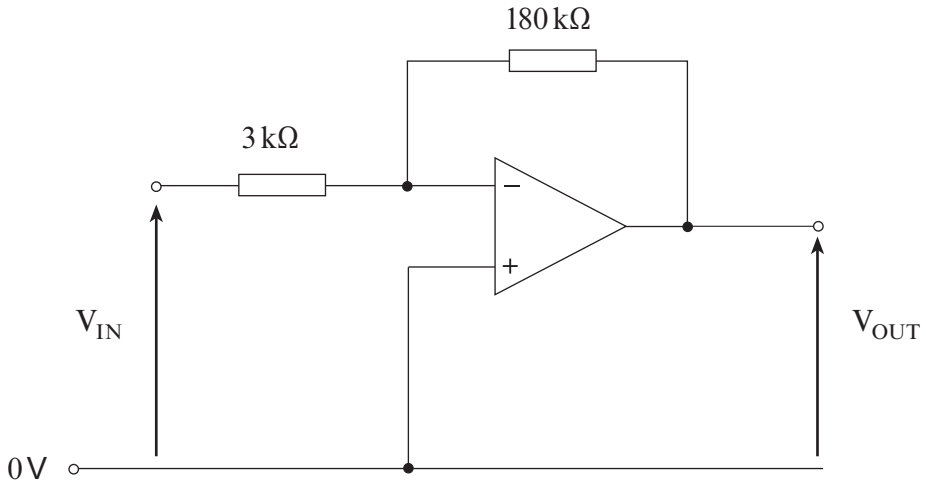
8. The following diagram shows an op-amp used as a voltage amplifier.



(a) Calculate the voltage gain of the amplifier. [1]

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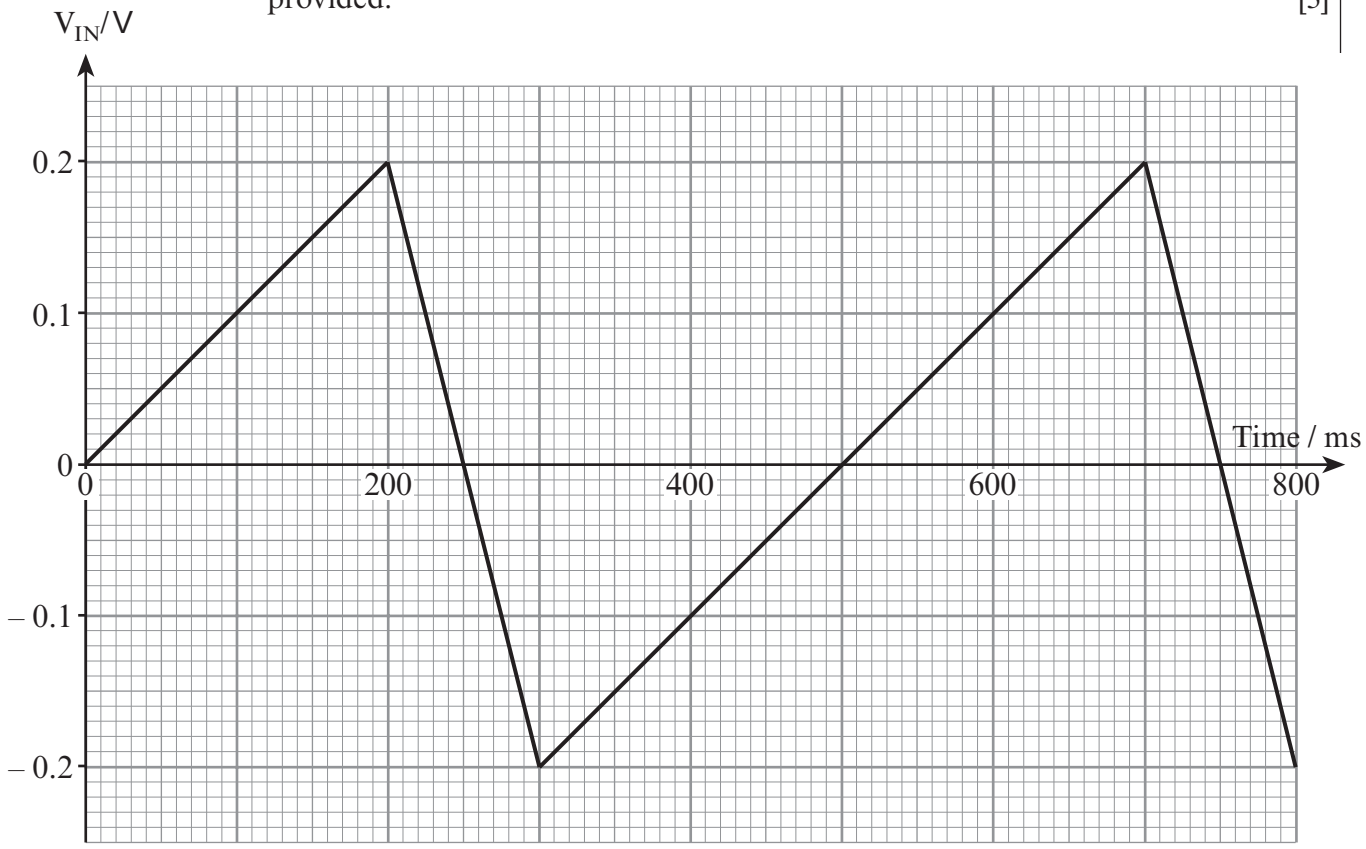
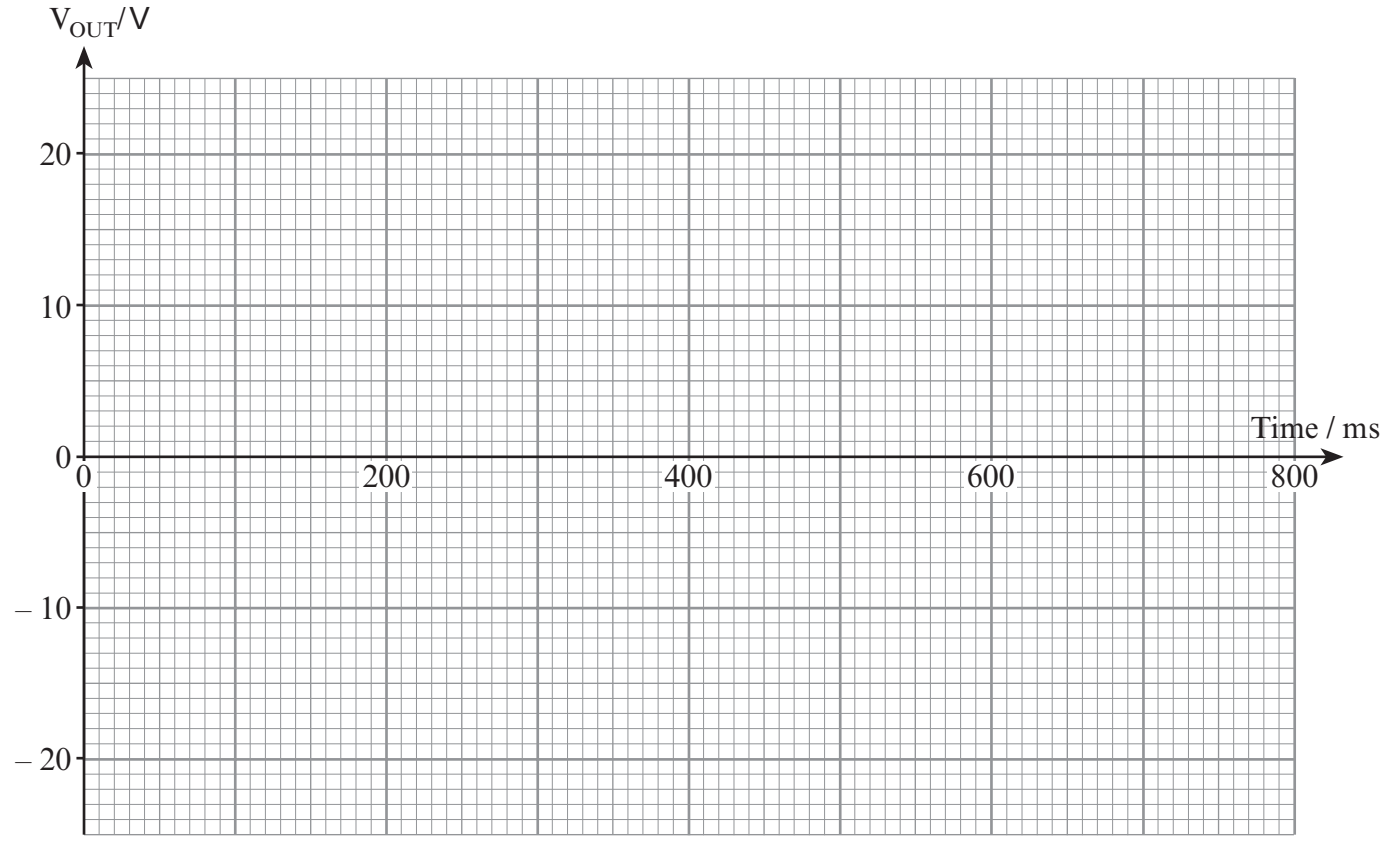
Examiner only

(b) A similar amplifier of gain –50 is powered from a ±15 V power supply and saturation occurs at ±14 V.

(i) The signal V_{IN} is applied to the input. Draw the output voltage V_{OUT} on the axes provided. [3]





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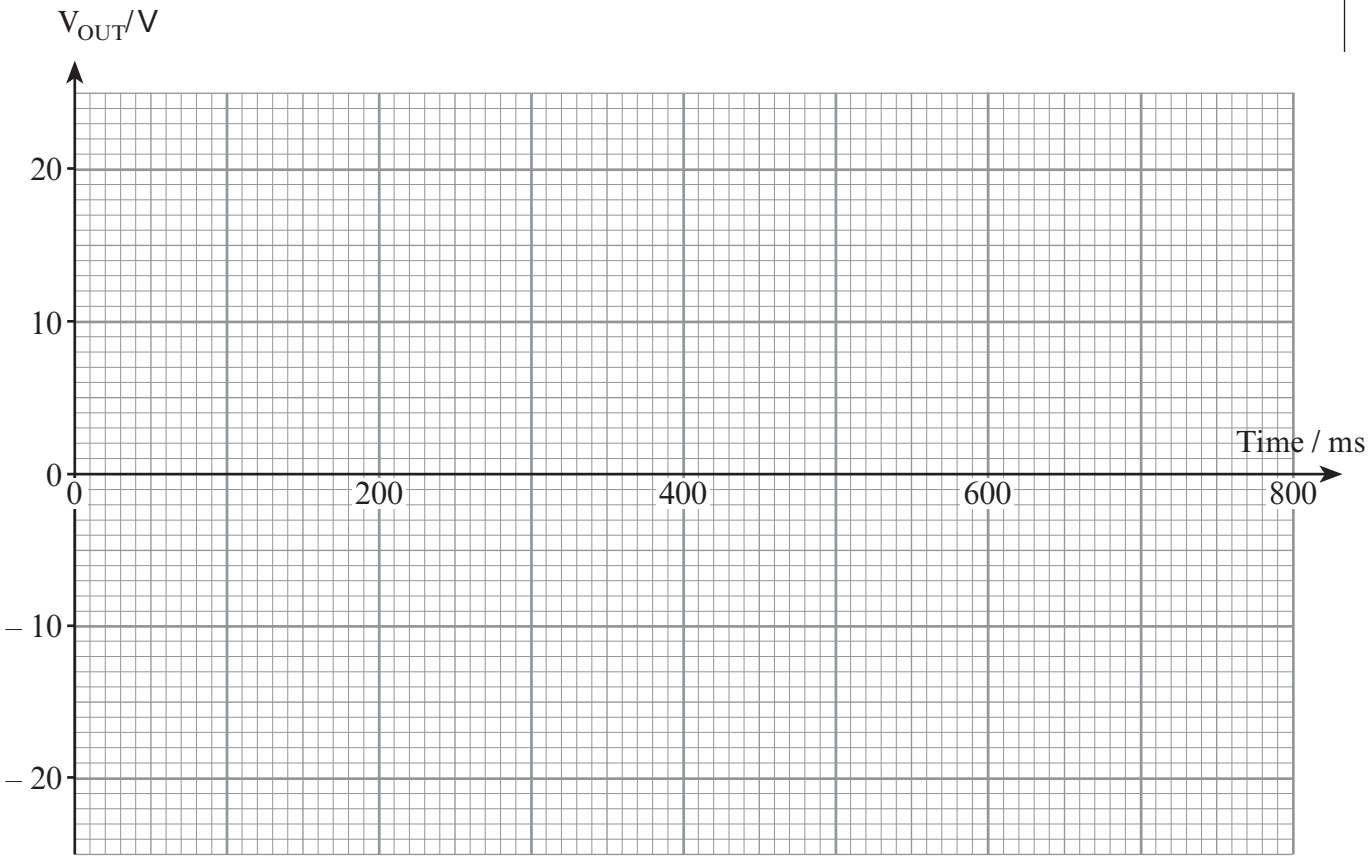
(ii) A different input signal of same shape and frequency but amplitude ± 400 mV is now applied to the input. Use the axes provided to sketch the resulting output signal. [2]



Turn over.

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9. The table shows some properties for two op-amps, X and Y.

Property	**X**	**Y**
Input Impedance / Ω	5×10^8	4×10^9
Open loop gain	6×10^5	1×10^6
Maximum output current / mA	5	20
Gain bandwidth product / MHz	4	2.5
Slew rate / V μs^{-1}	1.5	2.0
Maximum output voltage / V	18	18

(a) (i) Which amplifier is capable of reaching its maximum output voltage in the **shortest** time when a large step input signal is applied?

Op-amp .....

Reason: .....

(ii) What is the bandwidth of amplifier Y when it is configured to have a gain of 500?

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.....

.....

[2]

Examiner only

(b) (i) A third op-amp is configured to be a non-inverting voltage amplifier with a gain of 80. Draw the circuit diagram for this amplifier. Label R_1 and R_F. [3]

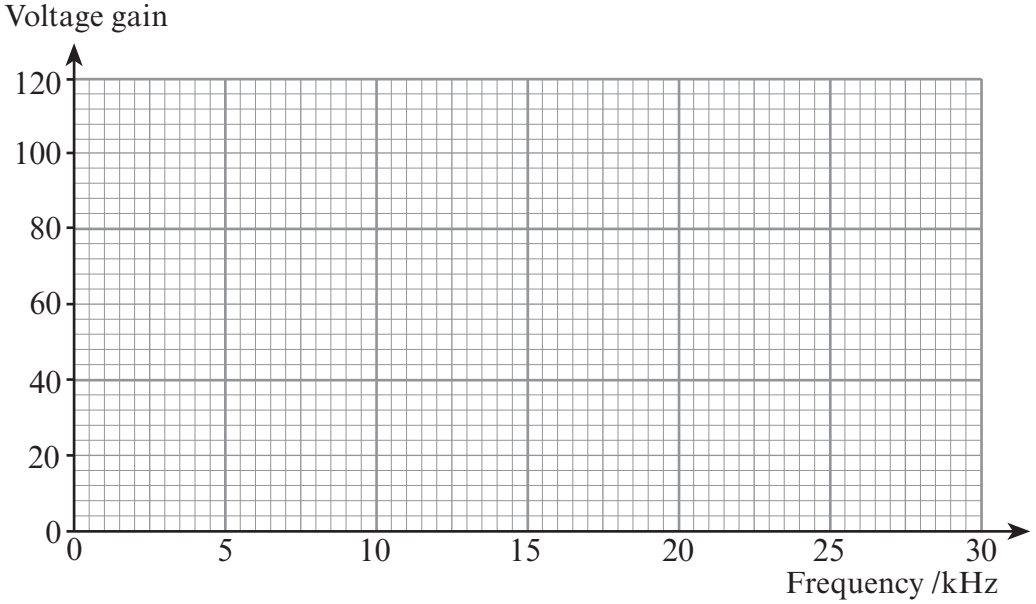
0 V

(ii) Select suitable resistors to give a voltage gain of 80.

R_1 .....

R_F ..... [2]

(c) This amplifier (gain 80) has a bandwidth of 24 kHz. Sketch the frequency response of the amplifier on the axes below. Clearly show the point at which the bandwidth is measured. [2]



TURN OVER FOR THE REST OF THE QUESTION.

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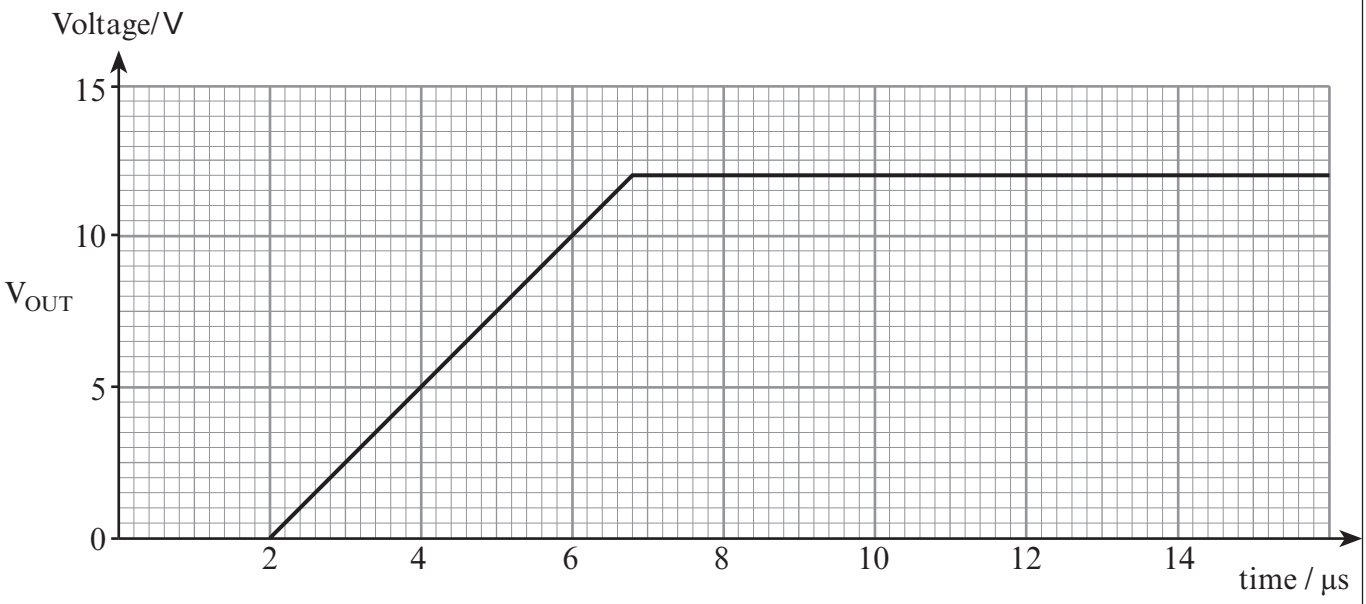
(d) The graph shows how the output voltage of the amplifier responds to a **large** step input voltage.



Calculate the slew rate of this amplifier and give an appropriate unit. [2]

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END OF PAPER