Surname

Centre Number Candidate Number

Other Names



GCE A level

1144/01

ELECTRONICS ET4

P.M. TUESDAY, 29 May 2012

l hour

For Examiner's use only			
Question	Maximum Mark	Mark Awarded	
1.	4		
2.	5		
3.	4		
4.	5		
5.	15		
6.	6		
7.	11		
Total	50		

ADDITIONAL MATERIALS

In addition to this examination paper, you will need a calculator.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer all questions.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The total number of marks available for this paper is 50.

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

You are reminded to show all working. Credit is given for correct working even when the final answer given is incorrect.

INFORMATION FOR THE USE OF CANDIDATES

Preferred Values for resistors

The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

Standard Multipliers:

Prefix	Multiplier	Prefix	Multiplier
Т	× 10 ¹²	m	× 10 ⁻³
G	× 10 ⁹	μ	× 10 ⁻⁶
М	× 10 ⁶	n	× 10 ⁻⁹
k	× 10 ³	р	× 10 ⁻¹²

Filters	$f_b = \frac{1}{2\pi RC}$	Break frequency for high pass and low pass filters
	$X_{\rm C} = \frac{1}{2\pi f \rm C}$	Capacitive reactance
	$X_L = 2\pi f L$	Inductive reactance
	$Z = \sqrt{R^2 + X_C^2}$	For a series RC circuit
	$f_0 = \frac{1}{2\pi\sqrt{LC}}$	Resonant frequency
	$R_{\rm D} = \frac{L}{r_{\rm L}C}$	Dynamic resistance
	$Q = \frac{2\pi f_0 L}{r_L}$	
	$Q = \frac{f_0}{B}$	
Modulation	$m = \frac{(V_{max} - V_{min})}{(V_{max} + V_{min})} \times 100\%$	Depth of modulation
	$\beta = \frac{\Delta f_c}{f_i}$	Modulation index
	resolution = $\frac{i/p \text{ voltage range}}{2^n}$	РСМ
	Bandwidth = $2(\Delta f_c + f_i)$	Transmitted FM Bandwidth
	Bandwidth = $2(1 + \beta)f_i$	
Radio receivers	$C = \frac{1}{4\pi^2 f_0^2 L}$	

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Use f	$B \xrightarrow{f}_{\overline{z}} C$	Headphones
Uset	ne letters A–E to answer the following questions.	
(a)	Which component modifies the RF signal to give a non-zero average signal?	
(<i>b</i>)	Which component separates the audio signal from the RF carrier?	
(c)	Which component carries more than one RF signal at all times?	
(<i>d</i>)	Which components select the required RF signal?	

3

1. The circuit diagram for a simple radio receiver is shown below.

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Turn over.

[4]

Amplitude

- [3]
- (b) The 15 kHz sinusoidal wave is now replaced with an audio signal containing frequencies in the range 250 Hz 15 kHz. The carrier signal frequency is still 200 kHz.
 - (i) On the axes below, draw the frequency spectrum of the transmitted wave. Label **all** significant frequencies.





(ii) What is the broadcast bandwidth of the signal?

[1]

[1]

- 3. Frequency modulation (FM) is a very popular way of transmitting good quality radio signals.
 - (a) The test signal below is used to frequency modulate the carrier. Use the axis provided to draw the FM Signal.



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4.

Calculate the value of V_{IN} which causes V_{OUT} to change from -9 V to +9 V. (ii) [2] A digital signal degrades as it travels along a transmission line. A Schmitt trigger can be used to restore the signal to its original state. Name two causes of signal degradation that are restored by the Schmitt trigger. 1. 2. [1]

(b)



(b) An engineer is designing an I.F. filter for a Superhet receiver.

The following circuit diagram shows the IF filter connected to a signal generator with the peak value of V_{IN} set to 12 V. The inductor has a resistance r_L of 2.6 Ω . V_{IN} is kept at 12 V and the frequency increased to give the maximum value of V_{OUT} .



(i) Calculate the frequency at which V_{OUT} is a maximum.

[2]

(ii)	Calculate the Dynamic Resistance R _D of the filter.	Examiner only
(iii)	[2] Use your answer to part (ii) to determine the maximum value of the voltage $V_{\rm OUT}$ with $V_{\rm IN}$ set to 12 V.	
(iv)	[2] Determine the 'Q factor' of this circuit.	
(v)	[2] Determine the bandwidth of this filter.	1144
······	[1]	

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Sketch the frequency response of the filter using the axes below. (vi)

Label, with numerical values:

- Peak Output Voltage. Resonant frequency. i.
- ii.
- Bandwidth. iii.





[3]

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6. The ASCII code is an internationally agreed method of coding alphanumeric characters in computer systems.

Character	ASCII Code
V	1010110
W	1010111
Х	1011000
Y	1011001
Z	1011010

The following table gives the ASCII code for a number of different characters.

- (a) A computer system uses **even** parity. Start, stop and parity bits have to be added before the signal can be transmitted.
 - (i) What is the purpose of the parity bit?
 - (ii) What is the value of the parity bit when character, 'X' is transmitted?

[1]

[1]

(b) The graph below shows the signal for a character, received at the end of the transmission link.



(c) The **same** character was transmitted again, and the information received is shown in the graph below.



Given that an attempt was made to transmit the same character, as in part (b), explain why the receiving equipment would not have rejected the data as being incorrect.



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<i>(b)</i>	The	The signal from the low pass filter contains frequencies in the range 50 Hz - 18 kHz.			
	(i)	What is the relationship between the input signal frequency range and the minimum sampling frequency required to allow the signal from the low pass filter to be reconstructed at the receiver?			
		[1]			
	(ii)	Hence, what is the minimum frequency that can be used for Clock A in this transmitter?			
		[1]			
(c)	Cloc Expl	ek B must operate at a higher frequency than Clock A for the system to work properly. lain why this is the case.			
•••••					
•••••					
		[1]			
	The	[1]			
(a)	The	16-bit Analogue to Digital Converter (ADC) has an input voltage range of 0 to 12 v.			
	Wha	at is the resolution of the system?			
•••••					
•••••					
		[2]			

PART (e) OF THIS QUESTION IS ON THE NEXT PAGE

A PCM receiver requires a serial-in-parallel-out shift register (SIPO) which can be (e) constructed using D-Type flip-flops.



On the diagram above

Clock

draw the connections needed to make the first 4-bits of a SIPO shift register; [2] (i)

(ii)	label the signal input;	[1]
(iii)	label the signal outputs.	[1]

THERE ARE NO MORE QUESTIONS IN THE EXAMINATION.

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