Candidate Name	Centre Number	Candidate Number
		2

GCE AS/A level

1141/01

ELECTRONICS

ET1

P.M. WEDNESDAY, 12 January 2011

1¼ hours

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**11**	
2.	**7**	
3.	**6**	
4.	**4**	
5.	**12**	
6.	**11**	
7.	**9**	
Total	**60**	

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ADDITIONAL MATERIALS

In addition to this examination paper, you will need a calculator.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The total number of marks available for this paper is 60.

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

You are reminded to show all working. Credit is given for correct working even when the final answer given is incorrect.

INFORMATION FOR THE USE OF CANDIDATES

Preferred Values for resistors

The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

Standard Multipliers

Prefix	Multiplier
T	$\times 10^{12}$
G	$\times 10^{9}$
M	$\times 10^{6}$
k	$\times 10^{3}$

Prefix	Multiplier
m	$\times 10^{-3}$
μ	$\times 10^{-6}$
n	$\times 10^{-9}$
p	$\times 10^{-12}$

Boolean Identities

$A + \overline{A}.B = A + B$

$A.B + A = A.(B + 1) = A$

Operational amplifier

$$G = -\frac{R_F}{R_{IN}}$$

$$G = 1 + \frac{R_F}{R_1}$$

$$\text{Slew Rate} = \frac{\Delta V_{OUT}}{\Delta t}$$

1. *(a)* Here is the truth table for a two-input logic gate.

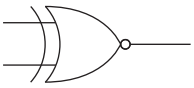
A	B	Q
0	0	1
1	0	0
0	1	0
1	1	0

Identify the logic gate and draw the correct symbol for it.

Logic Gate: ..... [1]

Symbol: [1]

(b) Complete the truth table for the two-input EXNOR gate shown below.



A	B	Q
0	0	
1	0	
0	1	
1	1	

[1]

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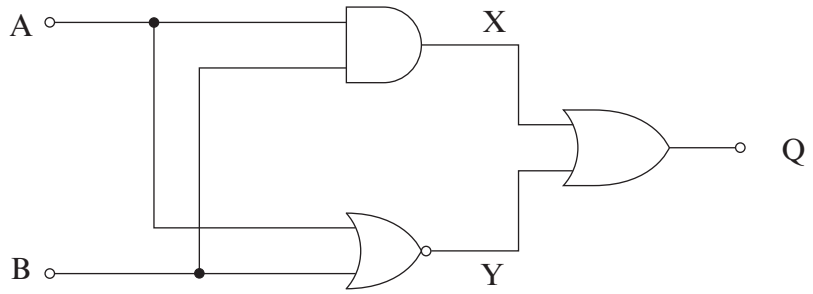
(c) An EXNOR gate can be built from other logic gates. Complete the truth table to show that the following circuit produces the same output as an EXNOR gate.



A	B	X	Y	Q
0	**0**			
1	**0**			
0	**1**			
1	**1**			

[2]

(d) A student attempts to build this circuit but mistakenly uses a NOR gate in place of the OR gate. What effect would this mistake have on output Q? [1]

.....

.....

(e) In the space below, draw the same logic system as the one shown in part *(c)*, but with the logic gates replaced by their NAND gate equivalent.

[3]

(f) Draw lines through all redundant gates. [2]

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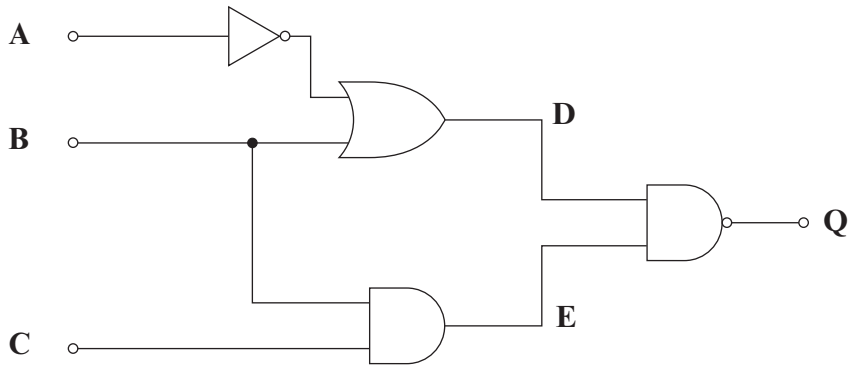
2. The following diagram shows a logic system.



(a) Write down the Boolean expressions for D, E and Q in terms of inputs A, B and C:

D = ...

E = ...

Q = ...

[3]

(b) The Boolean expression for another 3 input logic system is $Q = \overline{(A.\overline{C})} + \overline{(B + A)}$

Apply DeMorgans theorem to this expression and simplify it to show that input B is not needed. [4]

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3. *(a)* Simplify the following expressions, showing appropriate working.

(i) $\overline{A}.1 =$ ..... [1]

(ii) $A + \overline{A}.B =$ ..... [1]

(b) Either using a Karnaugh map or the rules of Boolean algebra, simplify the following expression as much as possible.

$$Q = \overline{D}.\overline{C}.\overline{B}.\overline{A} + \overline{D}.B.\overline{A} + D.C.B + \overline{D}.C.B.A + \overline{D}.C.\overline{A}$$

.....

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.....

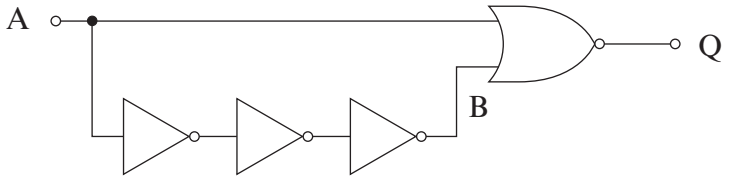
.....

.....

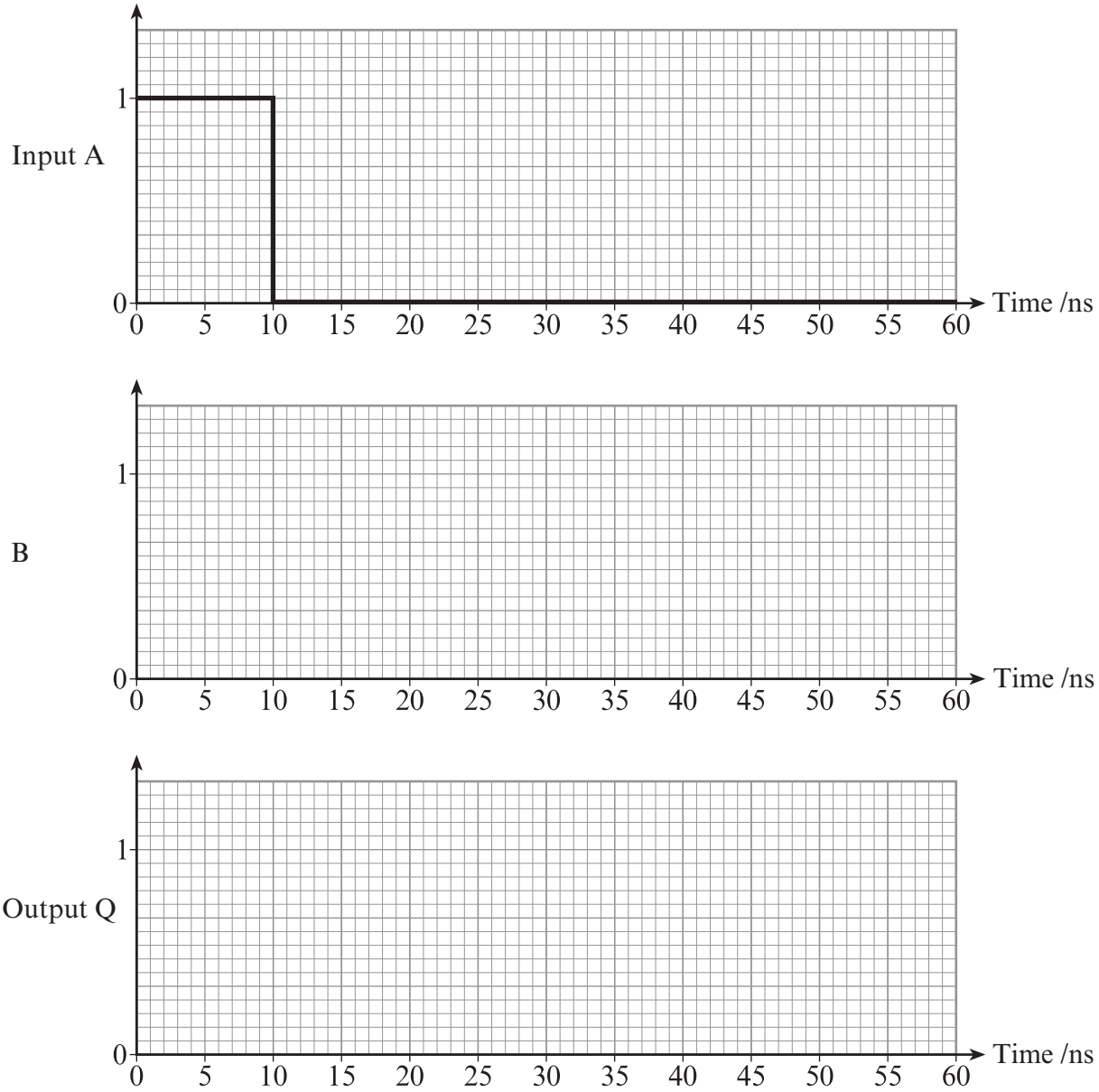
DC \ BA	00	01	11	10
00				
01				
11				
10				

[4]

4. The following transition gate is used to provide edge-triggering.
Each gate has a propagation delay of 10 ns.



Complete the following diagram to show how the signal at **B** and the output **Q** change when the pulse shown is applied to input **A**
Initially B and Q are both at logic 0.



[4]

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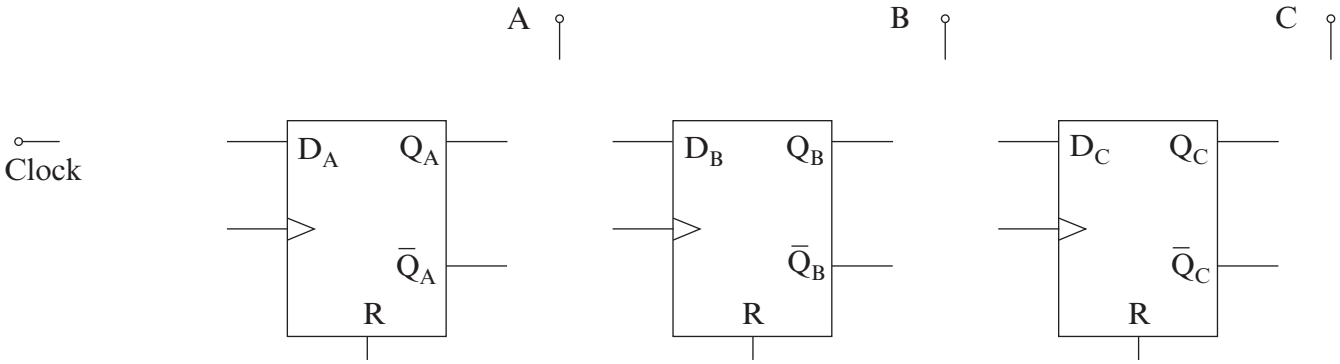
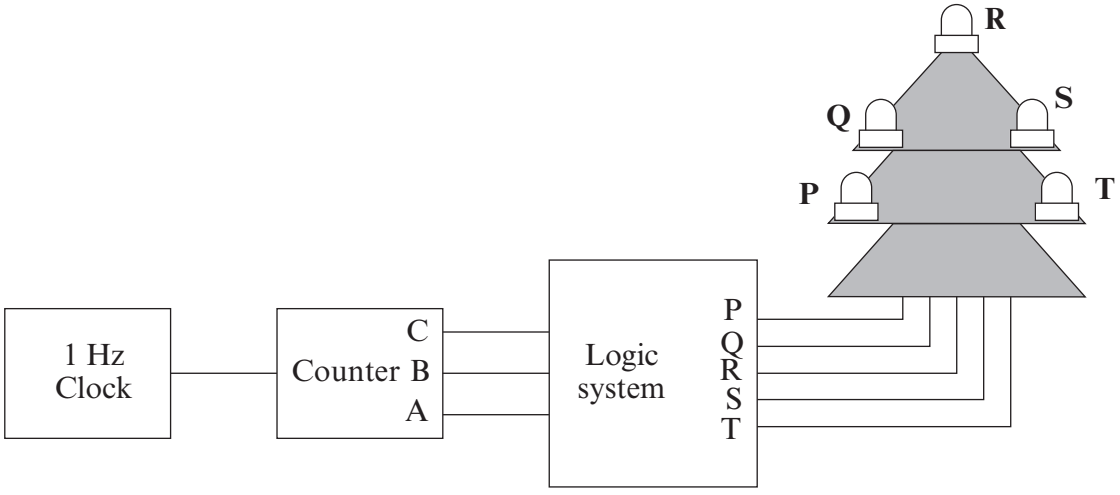
5. The diagram shows 3 D-type flip-flops, which form part of a binary up-counter. Outputs A, B and C are used to indicate the binary output.
C is the most significant bit.

(a) (i) Complete the diagram to make a three bit binary up-counter. [3]



(ii) On the circuit diagram above add a logic gate and the connections necessary to make the counter reset on the fifth clock pulse. [3]

(b) A student uses the counter to make a Christmas decoration.



An LED is on when the corresponding output is high.

The LEDs flash in the sequence specified by the following Boolean expressions:

$$P = T = \overline{B \oplus A}$$

$$Q = S = A + C$$

$$R = B.\overline{A} + C$$

Complete the truth table to show the sequence of outputs produced. [3]

Clock pulse	C	B	A	P	Q	R	S	T
0	0	0	0					
1	0	0	1					
2	0	1	0					
3	0	1	1					
4	1	0	0					
5	Counter resets here							

(c) Draw the logic circuit for the system.

[3]

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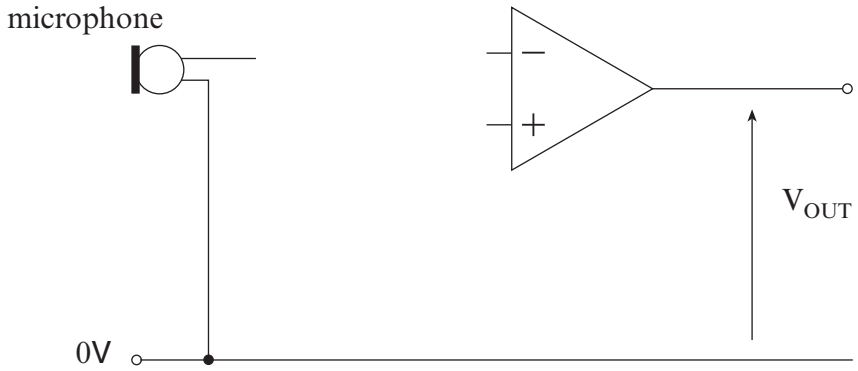
6. An incomplete circuit diagram for a non-inverting voltage amplifier is shown below. It is to be used to amplify the signal from a microphone with peak output voltage ± 100 mV.

(a) Complete the diagram to show this amplifier.



[3]

The saturation voltage of the amplifier output is ± 12 V.

(b) (i) Calculate the maximum voltage gain for the amplifier that avoids clipping distortion. [1]

.....

.....

(ii) Choose suitable resistor values to give the amplifier this voltage gain. Label the circuit diagram with these values. [2]

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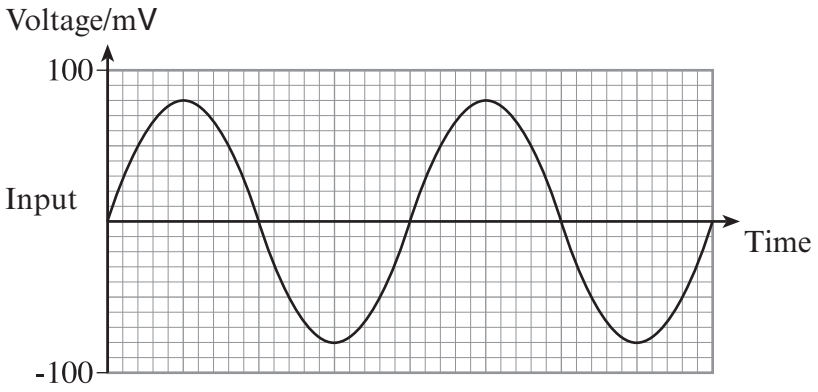
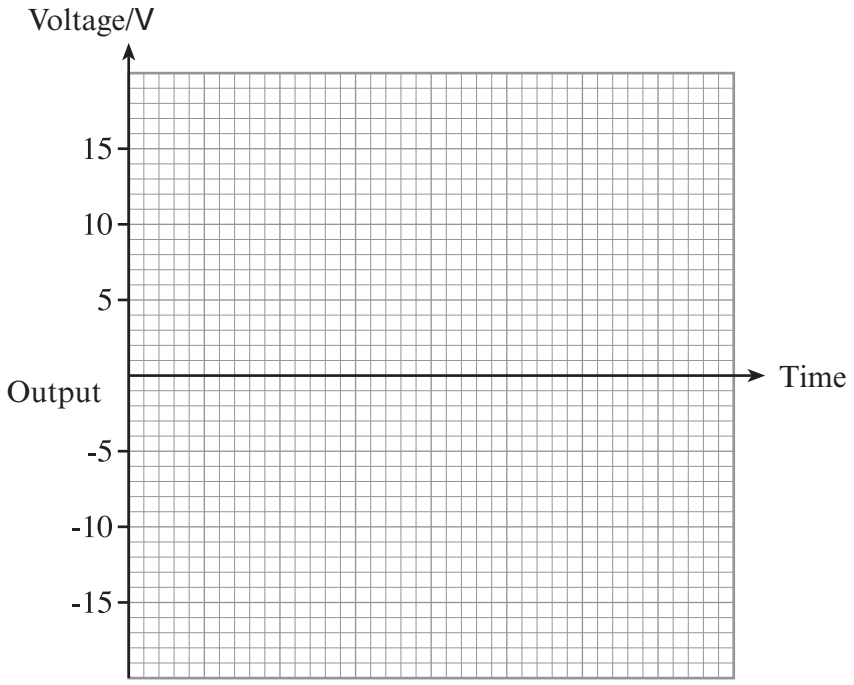
(c) (i) A different non-inverting amplifier has a voltage gain of 140.
The saturation voltage is ± 12V. The following signal is applied to the input. Draw the output voltage and label important voltage values on the lower grid.





[3]

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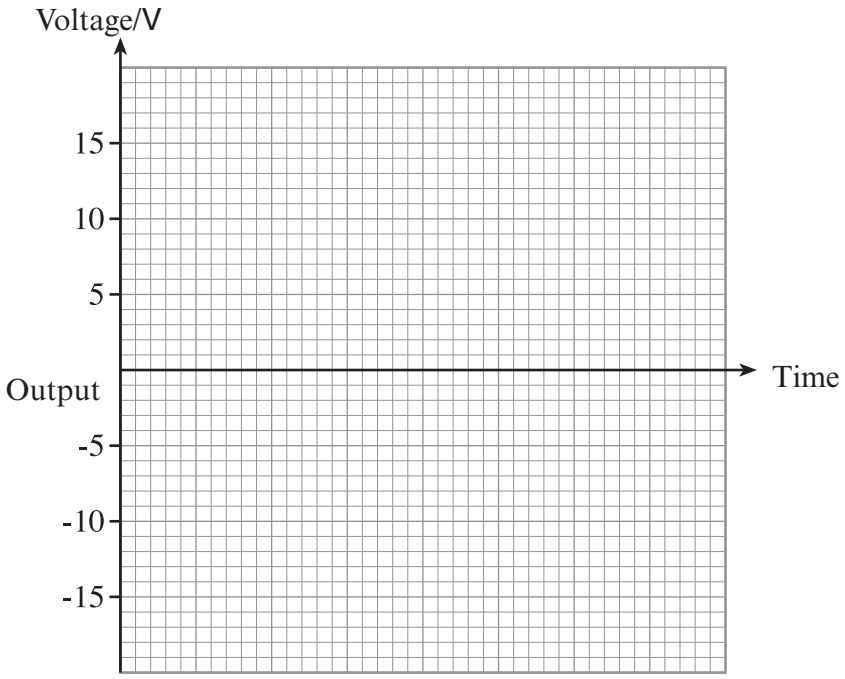
(ii) The amplitude of the input signal is increased to ± 100mV. Sketch the output voltage on the axes provided.



[2]

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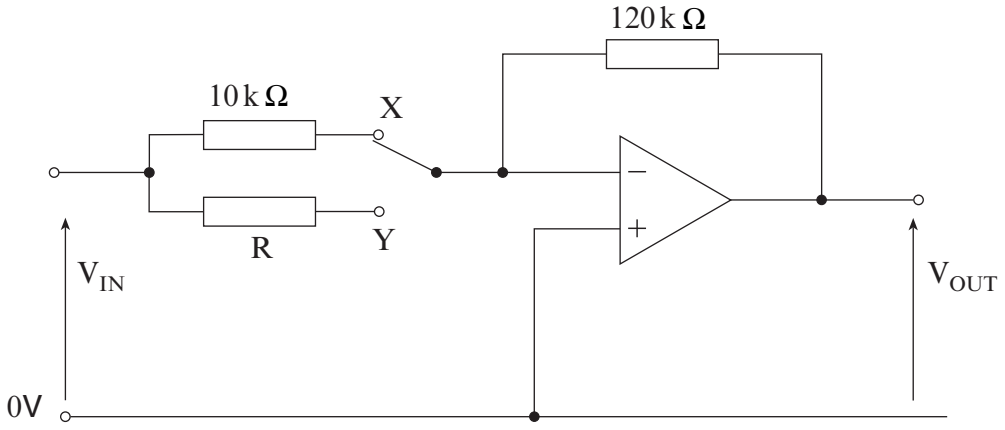
7. An extract from the data sheet of an op-amp is shown in the following table.

Parameter	Value
Input Impedance	10 MΩ
Output Impedance	100 Ω
Open Loop Gain	10^5
Gain Bandwidth Product	1.5 MHz
Slew Rate	6 $V\mu s^{-1}$

The circuit diagram below shows an op-amp set up as a voltage amplifier. The switch allows the user to change the gain of the amplifier.



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The op-amp is powered from a ±15 V supply and saturation occurs at ±14 V.

An input voltage of 0.9 V is applied to V_{IN}.

(a) The switch is initially connected to position **X**.

(i) Determine the input impedance of the amplifier.

.....

(ii) Calculate the voltage gain of the amplifier.

.....

.....

(iii) Calculate the output voltage when V_{IN} = 0.9 V.

.....

(iv) Calculate the bandwidth of the amplifier.

.....

.....

[6]

(b) The switch is moved to position **Y**. This doubles the gain of the amplifier.

Calculate:

(i) the value of resistor R;

.....

.....

(ii) the output voltage for V_{IN} = 0.9 V.

.....

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[2]

(c) State what change, **if any**, has occurred to the bandwidth after the switch is moved from position **X** to **Y**.

.....

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[1]

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FOR USE ONLY IF YOU HAVE MADE SUBSTANTIAL DELETIONS IN PARTS OF YOUR ANSWERS OR NEED MORE SPACE TO COMPLETE THEM. BE SURE TO INDICATE THE QUESTIONS CONCERNED.