Candidate Name	Centre Number	Candidate Number

WJEC CBAC

GCE AS/A level

1141/01

ELECTRONICS

ET1

P.M. TUESDAY, 17 May 2011

1¼ hours

For Examiner's Use Only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**7**	
2.	**9**	
3.	**10**	
4.	**7**	
5.	**9**	
6.	**10**	
7.	**8**	
Total	**60**	

1141 010001

ADDITIONAL MATERIALS

In addition to this examination paper, you will need a calculator.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The total number of marks available for this paper is 60.

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

You are reminded to show all working. Credit is given for correct working even when the final answer given is incorrect.

INFORMATION FOR THE USE OF CANDIDATES

Preferred Values for resistors

The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

Standard Multipliers

Prefix	Multiplier
T	$\times 10^{12}$
G	$\times 10^{9}$
M	$\times 10^{6}$
k	$\times 10^{3}$

Prefix	Multiplier
m	$\times 10^{-3}$
μ	$\times 10^{-6}$
n	$\times 10^{-9}$
p	$\times 10^{-12}$

Boolean Identities

$A + \overline{A}.B = A + B$

$A.B + A = A.(B + 1) = A$

Operational amplifier

$$G = -\frac{R_F}{R_{IN}}$$

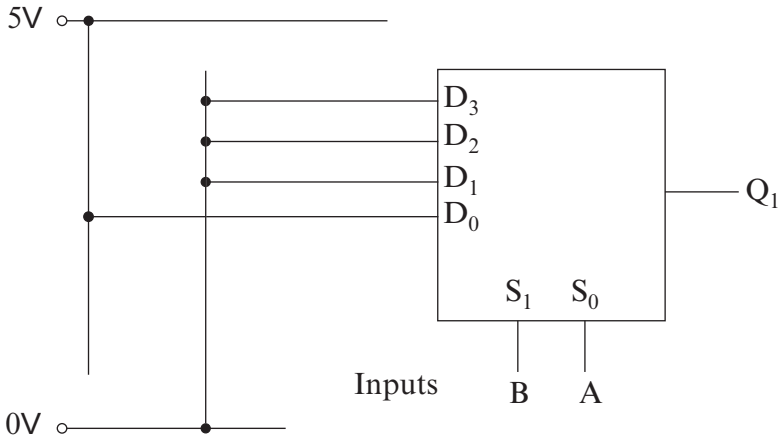
$$G = 1 + \frac{R_F}{R_1}$$

$$\text{Slew Rate} = \frac{\Delta V_{OUT}}{\Delta t}$$

Questions begin on page 4

Examiner only

1. *(a)* A multiplexer can be used as a programmable logic gate or system. Complete the truth table for the multiplexer shown in the diagram and, hence, identify the logic gate.



B	A	Q_1
0	0	
0	1	
1	0	
1	1	

[1]

Logic Gate ..... [1]

(b) (i) A logic system must generate the output Q_2 where

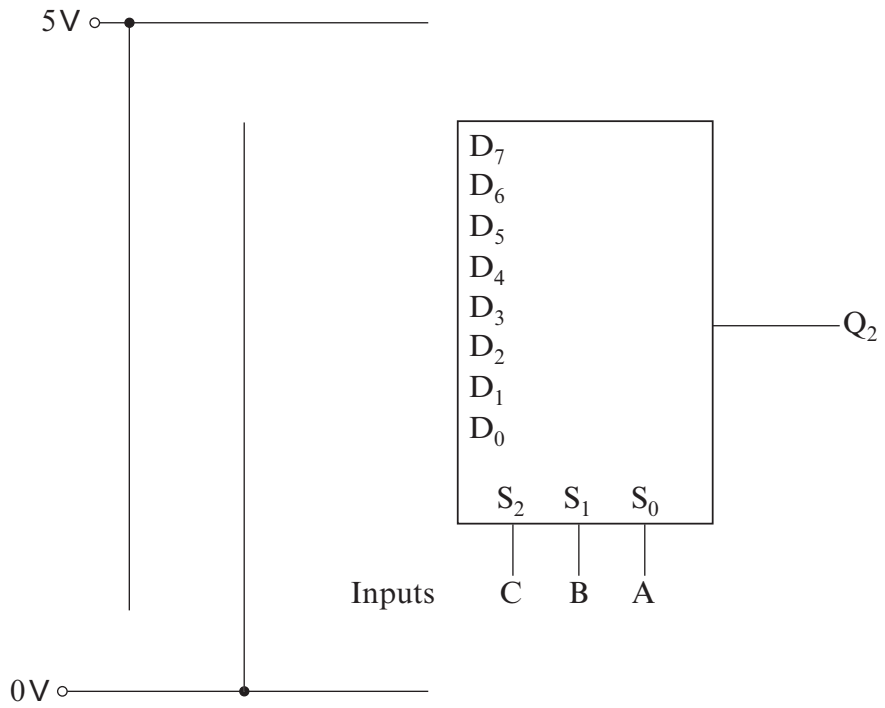
$$Q_2 = C.B.\overline{A} + \overline{C}.\overline{A}$$

Complete the truth table for this system.

C	B	A	Q_2
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

[2]

(ii) Complete the following diagram to show how the data inputs of an 8:1 multiplexer should be connected to perform the function in (i). The input S_2 is the **most significant** select input.



[2]

(c) Give one advantage of using a multiplexer in place of logic gates to perform logic functions.

.....

[1]

Examiner only

2. The output Q of an electronic warning system in a car illuminates an LED when the ignition key is turned on in either of the following circumstances;

1. the driver's door is open
2. the driver's seatbelt is not fastened.

- microswitch, A, on the door outputs a logic 1 if the door is open.
- microswitch,B, on the seatbelt outputs a logic 1 when the belt is fastened.
- sensor, C, outputs a logic 1 when the ignition key is turned.
- the LED is ON when Q is logic 1.

(a) Complete the truth table for the logic system.

Door switch A	Seatbelt switch B	Key sensor C	Q
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

[1]

(b) (i) Use the table to write down the unsimplified Boolean expression for Q in terms of C, B and A.

Q = ...

[2]

(ii) Simplify the expression using either a Karnaugh map or the rules of Boolean algebra.

.....

.....

.....

.....

.....

C \ BA	00	01	11	10
0				
1				

[3]

(c) Show on the following diagram how the same output, Q, can be generated using logic gates. Credit will be given for solutions using the least number of logic gates.

[3]

Examiner only

3. *(a)* Simplify the following expressions showing working where appropriate.

(i) B + 1 = ...

[1]

(ii) $(\overline{B} + \overline{A}).(B + A)$ = ...

.....

[2]

(b) A logic system produced the Karnaugh map shown below.

DC \ BA	00	01	11	10
00	1	1	0	0
01	1	0	1	1
11	0	0	1	1
10	1	1	0	0

Give the simplest Boolean expression for the output of this logic system.
Show any groups that you create on the map.

.....

.....

.....

[4]

(c) Apply DeMorgan's theorem to the following expression **and** simplify the result.

$$Q = \overline{\overline{(A + B)} + A}$$

.....

.....

.....

.....

.....

[3]

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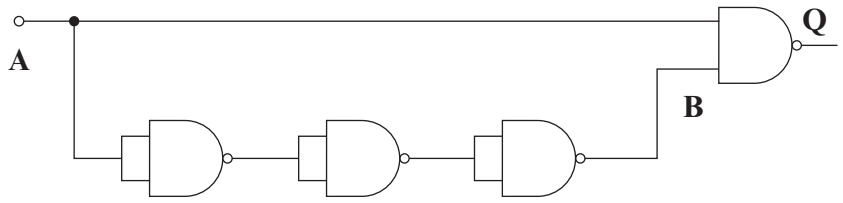
Examiner only

4. A transition gate, made from NAND gates, is shown below. Each NAND gate has a propagation delay of 10 ns.



(a) What is meant by *propagation delay*?

.....

.....

[1]

(b) What job does a transition gate perform within a D-type flip-flop?

.....

.....

[1]

(c) Why is it **not** appropriate to use the process of NAND redundancy in a transition gate?

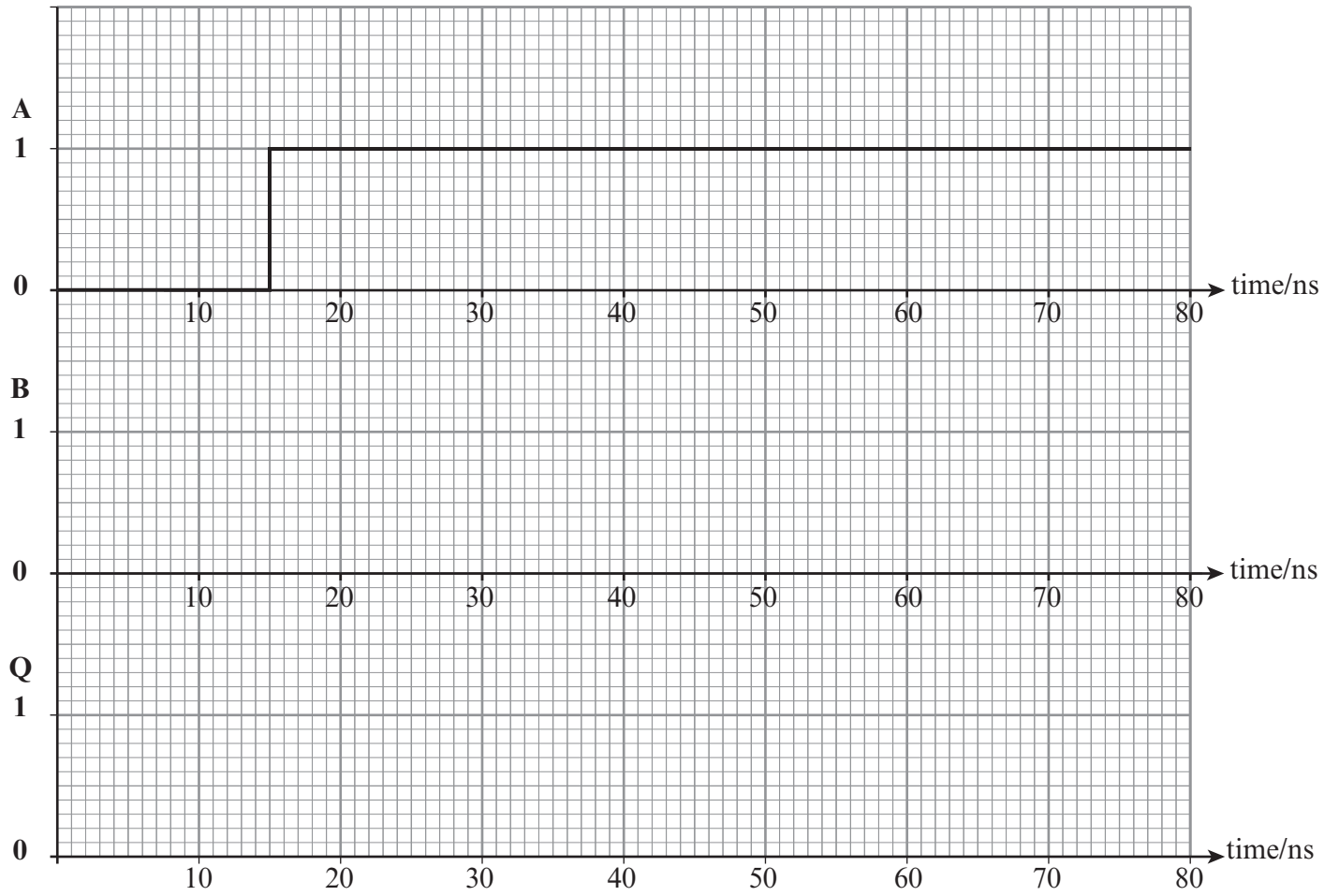
.....

.....

[1]

Examiner only

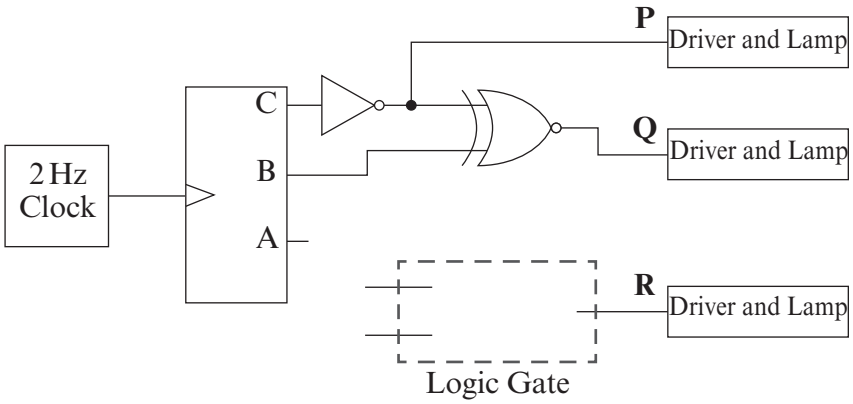
(d) The signal, shown on the graph is applied to input A.
Show on the diagram how the logic levels at **B** and **Q** change over the course of 80ns.



[4]

Examiner only

5. The diagram shows the control system for a lighting display that uses a 3-bit counter. A lamp is on when a logic 1 is applied to the driver. All the lamps are initially off.



(a) (i) Complete the truth table for columns P and Q.

[2]

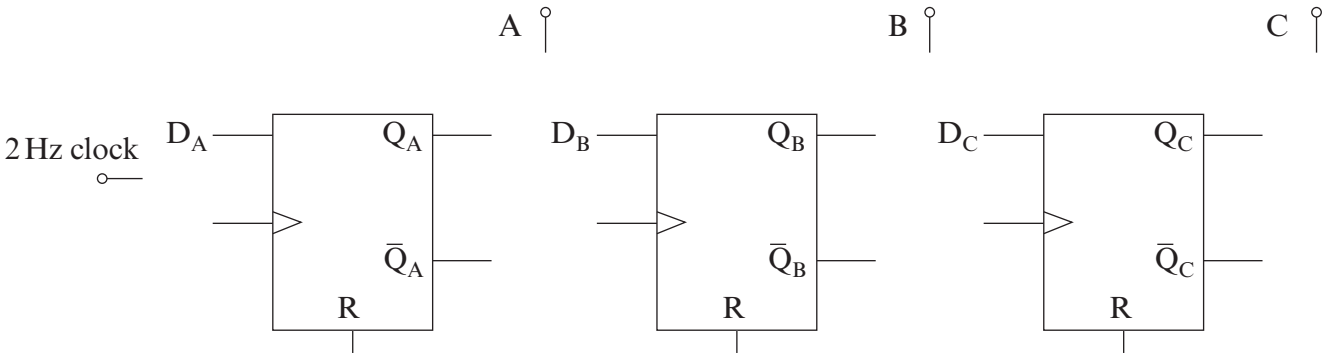
C	B	A	P	Q	R
0	0	0			1
0	0	1			1
0	1	0			1
0	1	1			0
1	0	0			1
1	0	1			1
1	1	0			1
1	1	1			0

(ii) In the dotted box above draw the 2-input logic gate that will produce output R and show how to connect it to the counter.

[2]

Examiner only

(b) Complete the diagram to show how three rising-edge-triggered D-type flip-flops can be connected to make a 3-bit up-counter.



[3]

(c) (i) How many pulses does the 2 Hz clock produce in 20 seconds?

.....

[1]

(ii) How many times does output B of the counter change in 20 seconds?

.....

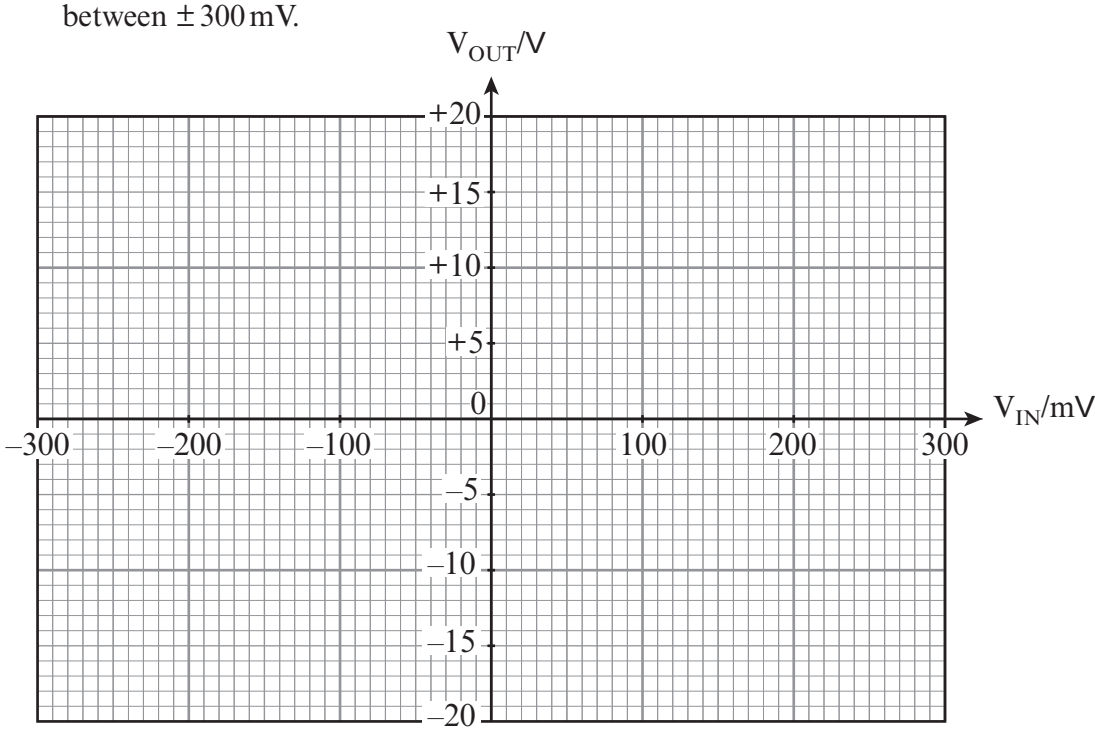
[1]

Examiner only

6. A voltage amplifier, built from an op-amp, is designed to fulfil the following specification:

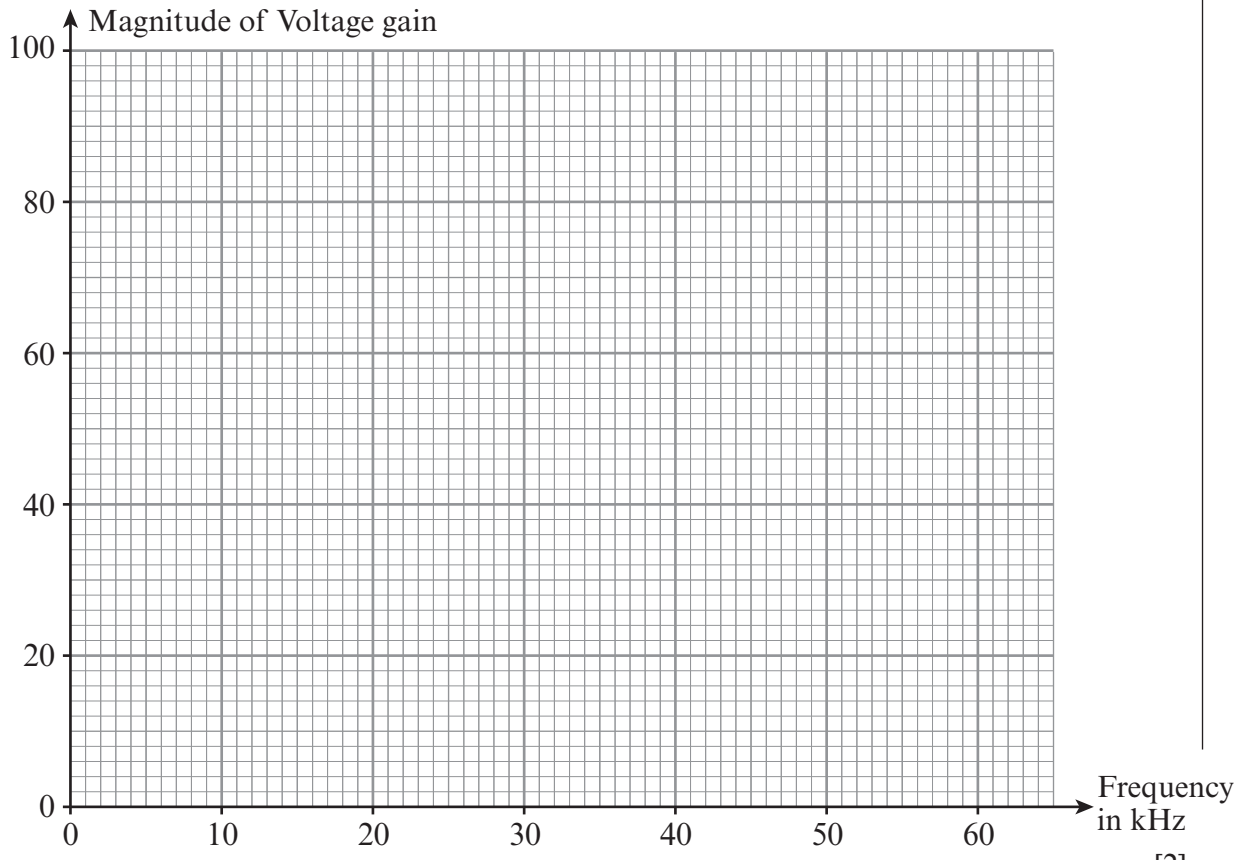
- Maximum output voltage at saturation ± 16 V
- Voltage gain – 80
- Gain bandwidth product 3.2 MHz
- Input impedance 2 kΩ

(a) Draw the voltage transfer characteristic of this voltage amplifier for input voltages between ± 300 mV.



[3]

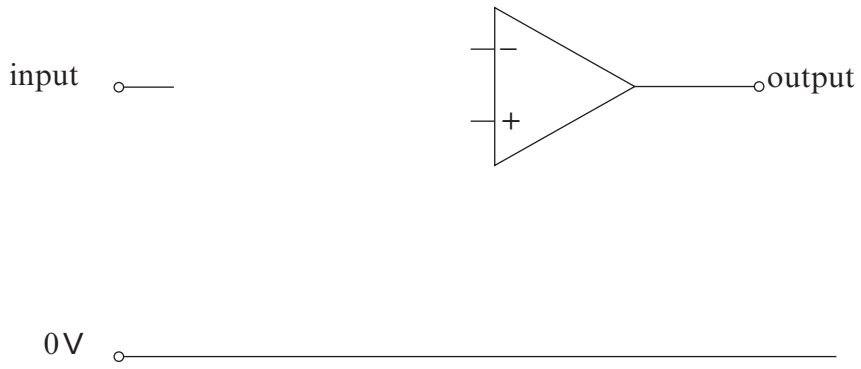
(b) Use the axes provided to draw the frequency response of this amplifier.



[2]

Examiner only

(c) (i) Complete the circuit diagram for this voltage amplifier.



[3]

(ii) Choose suitable resistor values to give the amplifier an input impedance of 4 kΩ and a voltage gain of −80. **Label the circuit diagram with these values**.

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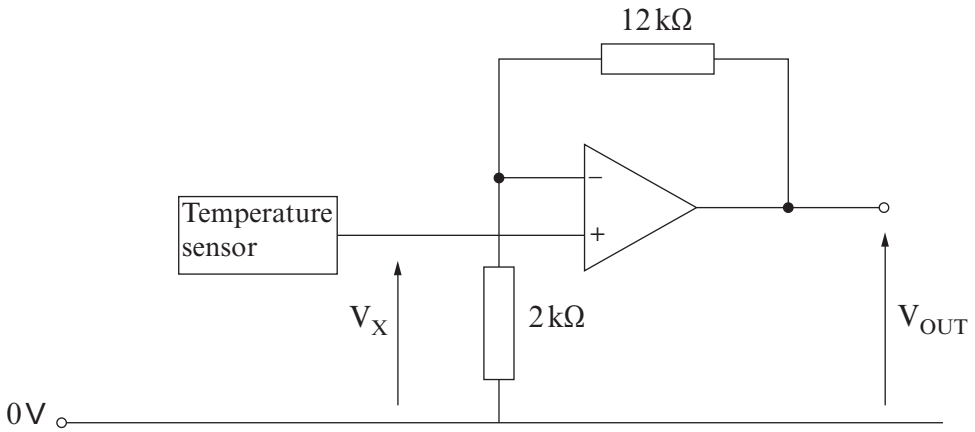
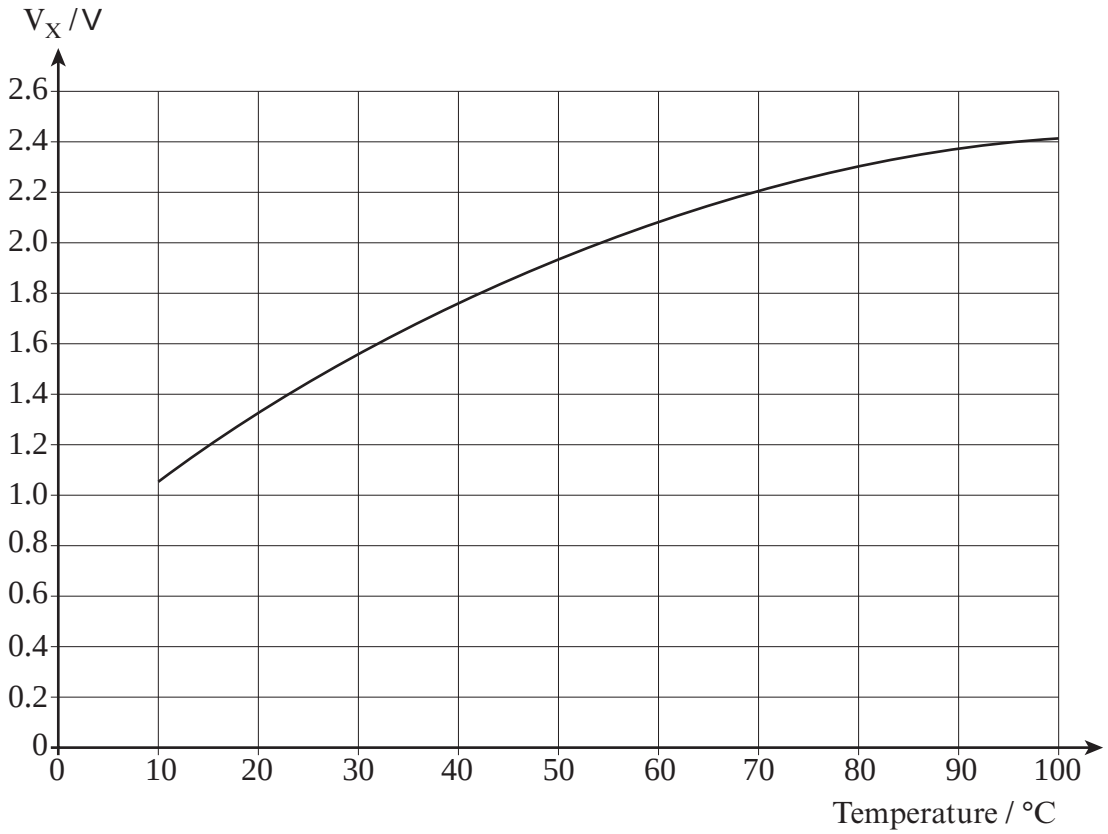
[2]

Examiner only

7. The circuit diagram shows part of a temperature control system. The output voltage of the temperature sensor changes in a non-linear way. This is shown in the calibration graph below. A voltage amplifier based on an op amp is used to amplify this voltage.





Examiner only

(a) Use the calibration graph to deduce the following:

(i) the temperature when $V_X = 1.6\,V$.

.....

[1]

(ii) the value of V_X when the temperature is 45 °C.

.....

[1]

(b) (i) What is the voltage gain of the amplifier?

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[2]

(ii) Calculate the output voltage, V_{OUT}, of the amplifier at 45 °C.

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[1]

(c) The operational amplifier saturates at $\pm 14\,V$.
Determine the maximum temperature that this system can reliably measure.

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[3]

Examiner only