Candidate Name	Centre Number	Candidate Number
		2

General Certificate of Education
Advanced Subsidiary/Advanced

381/01

ELECTRONICS
ET1

P.M. TUESDAY, 15 January 2008
(1½ hours)

ADDITIONAL MATERIALS

In addition to this examination paper, you will need a calculator.

INSTRUCTIONS TO CANDIDATES

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

For Examiner's use only.	
1	
2	
3	
4	
5	
6	
7	
8	
Total	

No certificate will be awarded to a candidate detected in any unfair practice during the examination.

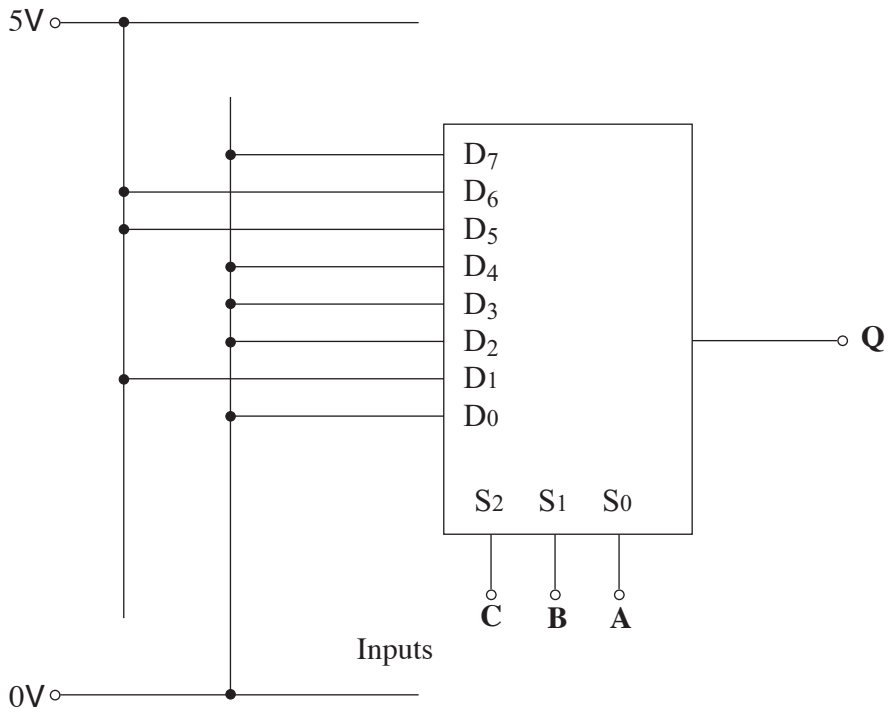
INFORMATION FOR THE USE OF CANDIDATES

Preferred Values for resistors
The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

RC networks	$V_C = V_O\,(1 - e^{-t/RC})$	for a charging capacitor
	$V_C = V_O\,e^{-t/RC}$	for a discharging capacitor
	$t = -RC\ 1n\left(1 - \frac{V_C}{V_O}\right)$	for a charging capacitor
	$t = -RC\ 1n\left(\frac{V_C}{V_O}\right)$	for a discharging capacitor
Alternating Voltages	$V_O = V_{rms}\sqrt{2}$	
Silicon Diode	$V_F \approx 0{\cdot}7\,V$	
Bipolar Transistor	$h_{FE} = \frac{I_C}{I_B}$	Current gain
	$V_{BE} \approx 0{\cdot}7\,V$	in the on state
MOSFETs	$I_D = g_M V_{GS}$	
Operational amplifier	$G = -\frac{R_F}{R_{IN}}$	Inverting amplifier
	$G = 1 + \frac{R_F}{R_1}$	Non-inverting amplifier
	$V_{OUT} = -R_F\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$	Summing amplifier
	$\text{Slew Rate} = \frac{\Delta V_{OUT}}{\Delta t}$	Slew rate
555 Monostable	$T = 1{\cdot}1\ RC$	
555 Astable	$t_H = 0{\cdot}7\,(R_A + R_B)C$	
	$t_L = 0{\cdot}7\ R_B C$	
	$f = \frac{1 \cdot 44}{(R_A + 2R_B)C}$	
Schmitt Astable	$f \approx \frac{1}{RC}$	

1. The diagram shows a multiplexer, used as a programmable logic system. The input S_2 is the **most significant** select input.



(a) Complete the following truth table for this system.

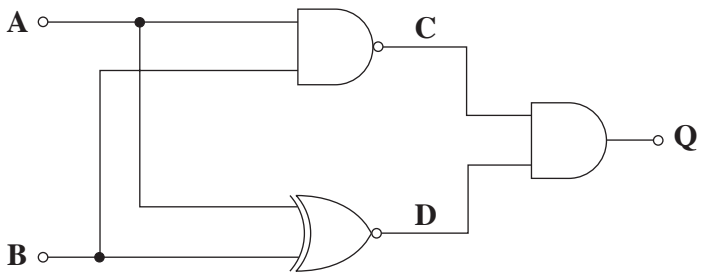
C	B	A	Q
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

[2]

(b) Write down the Boolean expression for **Q** in terms of **A**, **B** and **C**. Do **not** simplify the Boolean expression.

Q = ... [2]

2. *(a)* A logic system is shown below.



(i) Complete the truth table for this system.

B	A	C	D	Q
0	0			
0	1			
1	0			
1	1			

[3]

(ii) Write down the Boolean expressions for **C**, **D** and **Q** in terms of **A** and **B**.

C = ...

D = ...

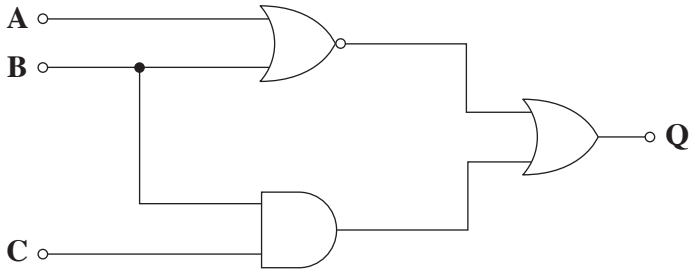
Q = ...

[3]

(iii) Name the single 2-input logic gate that could produce the same function as the **Q** output.

Logic Gate ..... [1]

(b) Here is another logic system.



(i) In the space below, draw the same logic system, but with the logic gates replaced by their NAND gate equivalents.

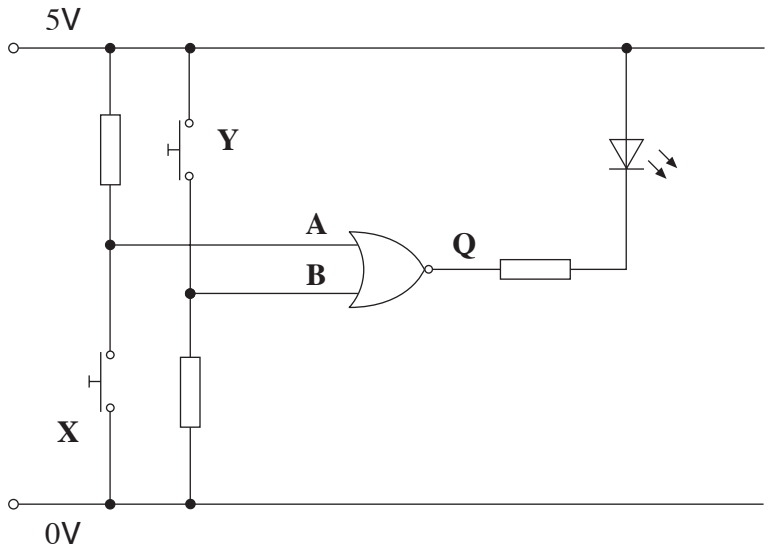
[3]

(ii) Each NAND integrated circuit contains four dual-input gates. What is the minimum number of ICs needed to construct this equivalent circuit?

.....

[1]

3. The circuit below contains both a pull-up and pull-down resistor.



The table below shows the four possible logic states of switches **X** and **Y**. Complete the table by adding:

- the correct logic level for points **A**, **B** and **Q**;
- the word **'OFF'** or **'ON'** to indicate the state of the LED in each case.

Switch **X**	Switch **Y**	Input **A**	Input **B**	Output **Q**	State of LED
Open	Open				
Open	Closed				
Closed	Open				
Closed	Closed				

[4]

Examiner only

4. *(a)* Simplify the following expressions, showing appropriate working.

(i) $B.\overline{0}$ = ... [1]

(ii) $B.A + B.\overline{A}$ = ...

..... [1]

(b) Either using a Karnaugh map or the rules of Boolean algebra, simplify the following expression as much as possible.

$$Q = D.C.B.A + C.\overline{B}.A + \overline{D}.\overline{C}.\overline{B} + D.C.A + D.\overline{C}.\overline{B}$$

.....

.....

.....

.....

.....

D.C \ B.A	0.0	0.1	1.1	1.0
0.0				
0.1				
1.1				
1.0				

[4]

(c) Apply DeMorgan's theorem to the following expression **and** simplify the result.

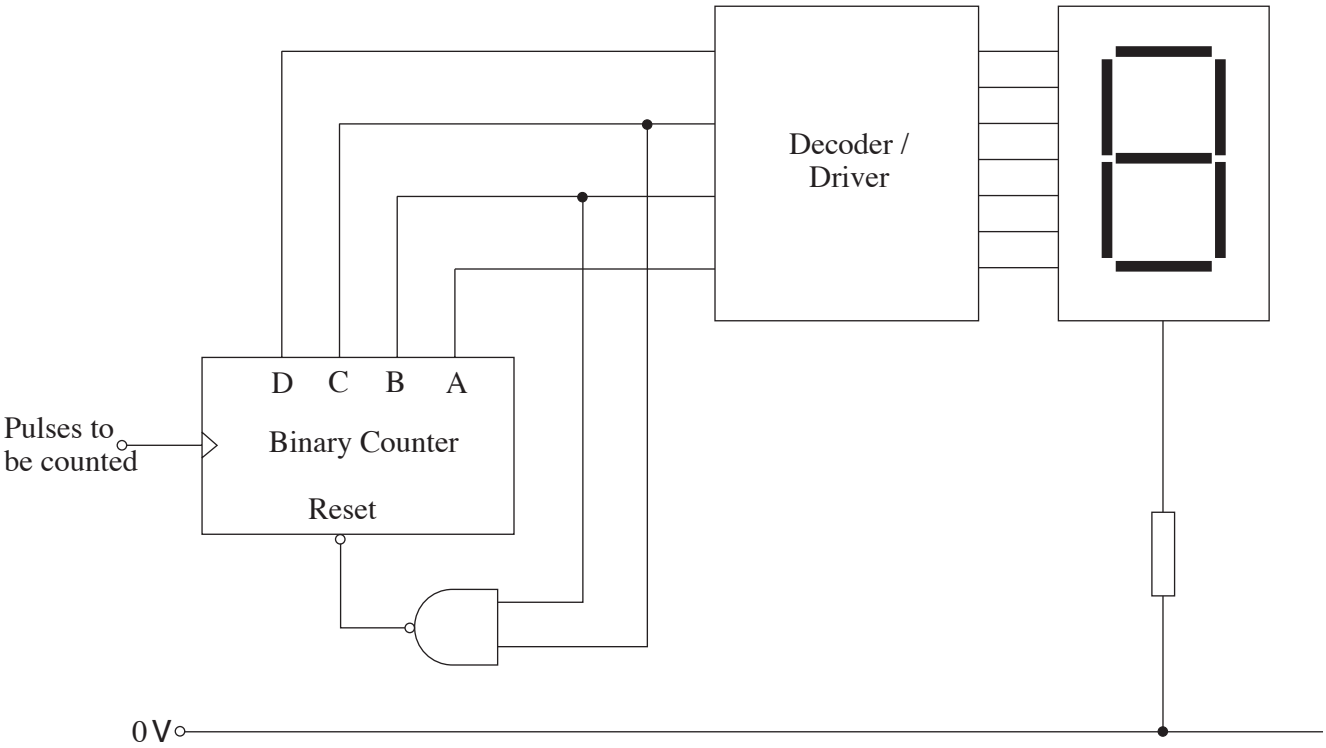
$$Q = \overline{(\overline{A + B}).\overline{A}}$$

.....

.....

..... [3]

5. The diagram below shows a counting system that uses a binary counter and 7-segment display.



(a) Describe the two functions of the decoder/driver.

1. .....

.....

2. .....

.....

[2]

Examiner only

(b) (i) What would be the last number displayed **before** the counter resets?

.....

[1]

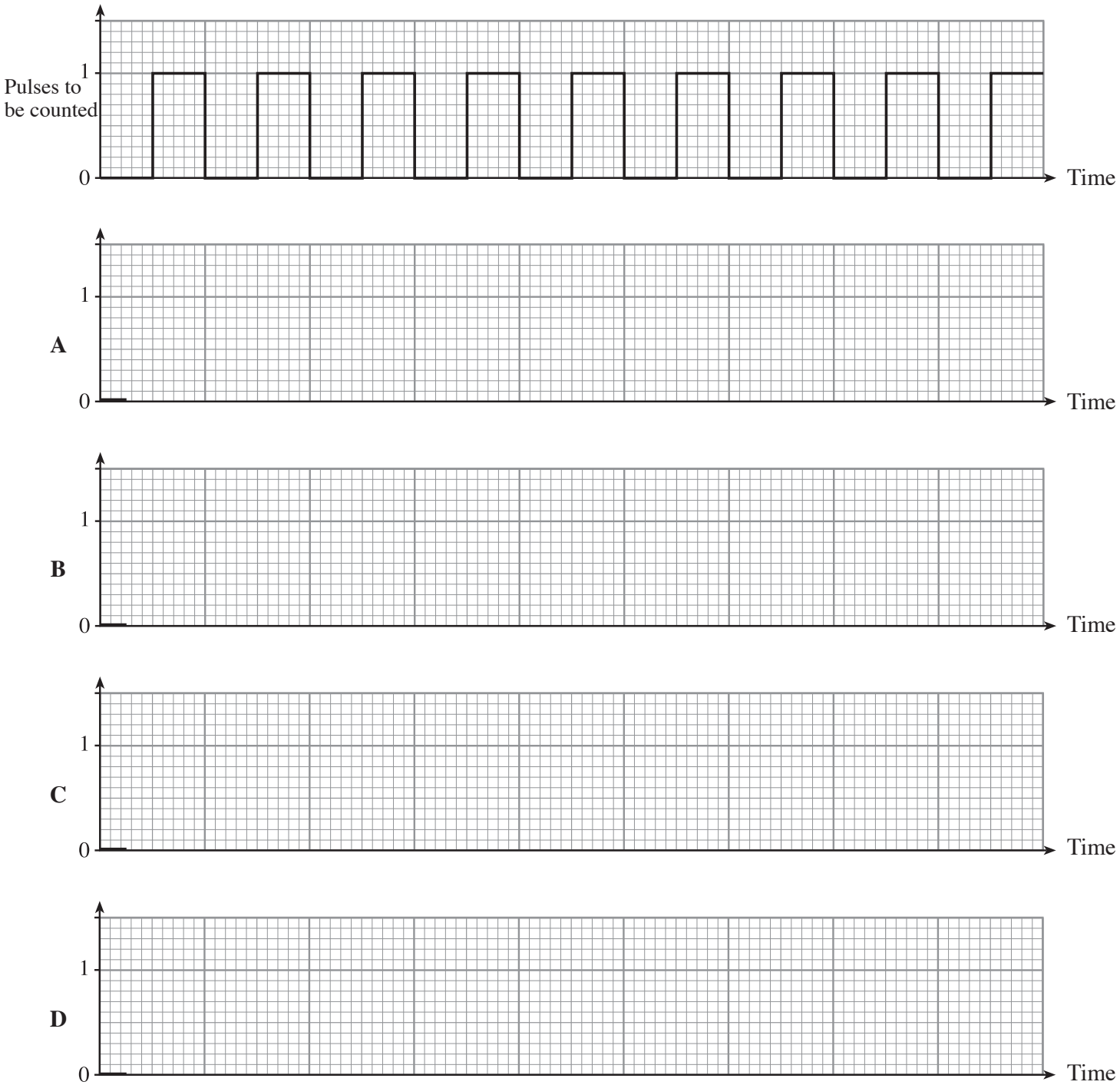
(ii) The counter shown is *rising-edge triggered*. What is meant by *rising-edge triggered*?

.....

.....

[1]

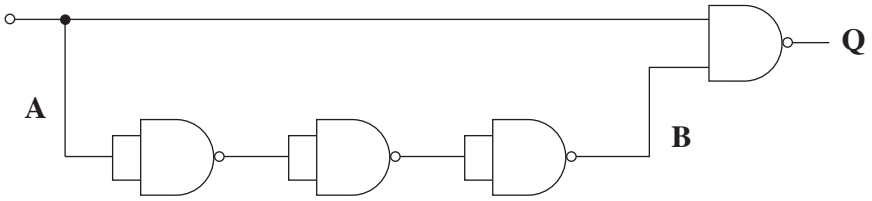
(c) The timing diagram shows pulses to be counted by the system. Use your answers to part *(b)* to complete the diagram to show the signals at outputs **A**, **B**, **C** and **D**.
Initially the counter is reset.



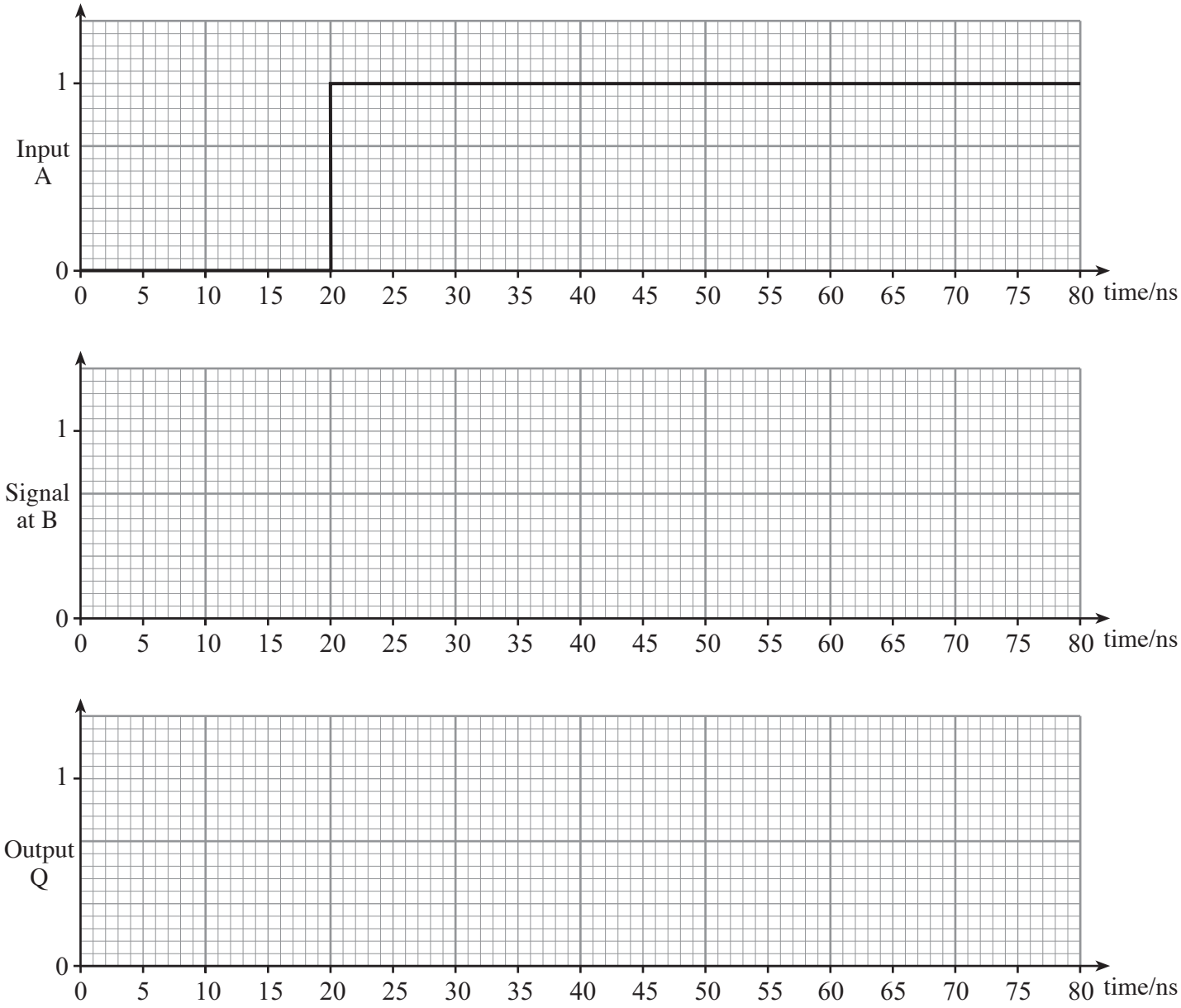
[4]

Examiner only

6. The following diagram shows the circuit for a *transition gate* constructed from NAND gates. Each logic gate has a propagation delay of 5 ns.



(a) Complete the following diagram to show how the signal at **B** and output **Q** change when the signal shown is applied to input **A**.
Initially, output Q is at logic 0.



[5]

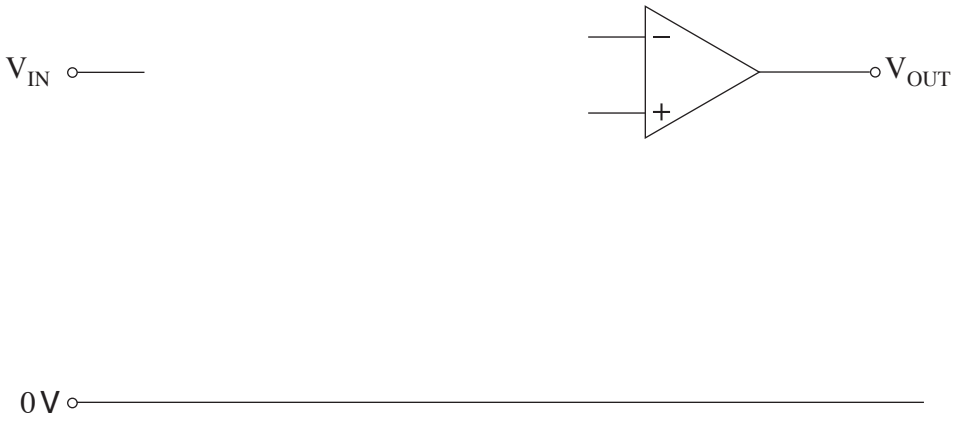
(b) What job does the transition gate perform within a D-type flip-flop?

.....

.....

[1]

7. *(a)* (i) Draw the circuit for an inverting amplifier based on an op-amp. [3]



(ii) Select suitable resistors to give a voltage gain of –24.

R_{IN} = ...

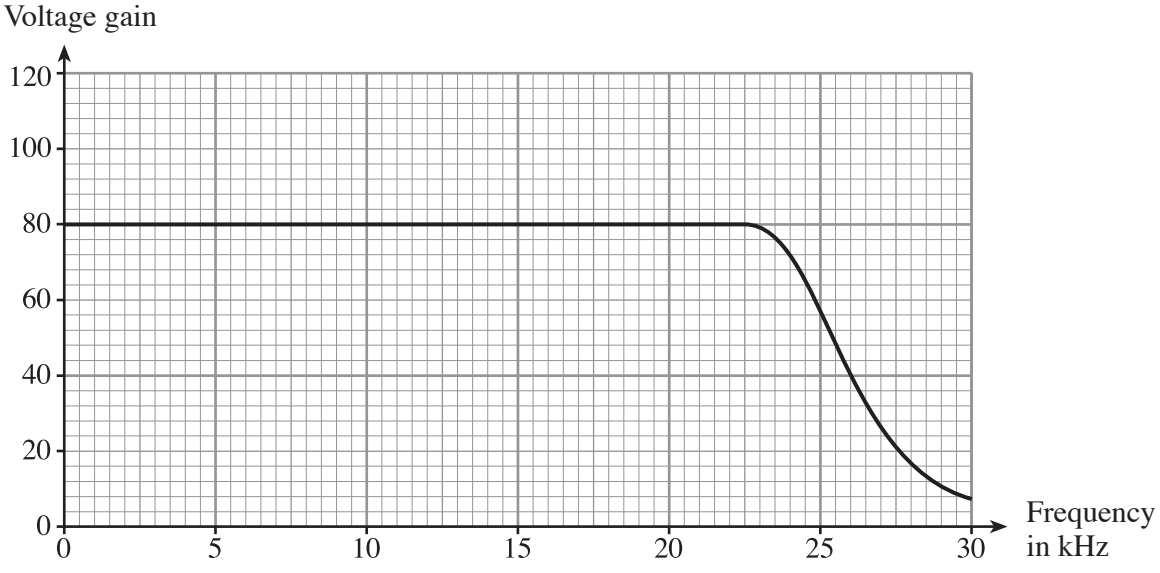
R_F = ... [2]

(iii) The voltage gain of the amplifier is now doubled without changing its input impedance. Select suitable resistors for this.

R_{IN} = ...

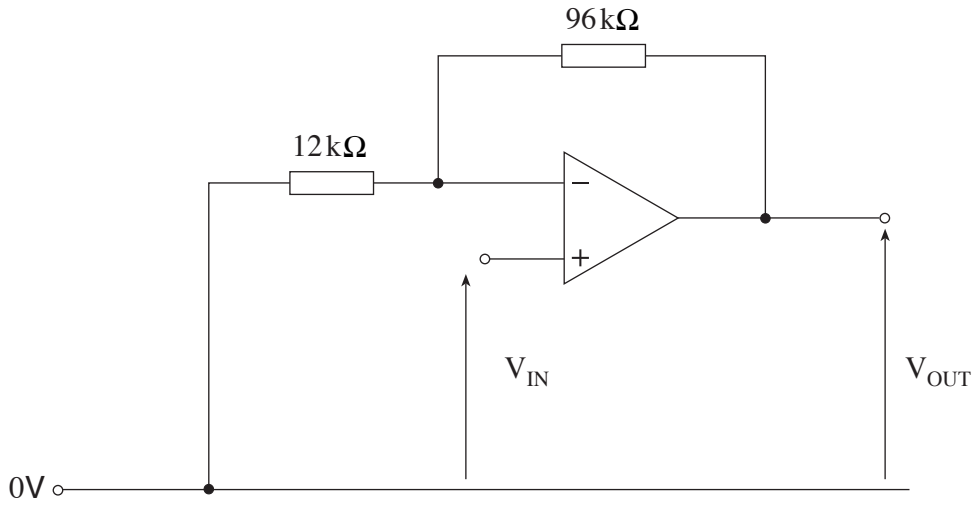
R_F = ... [1]

(b) Another amplifier has the frequency response shown below.
Use the graph to estimate the bandwidth of this amplifier.
Show **on the graph** how you obtained your result.



Bandwidth = ... kHz [2]

8. The following diagram shows an op-amp set up as a voltage amplifier.



An extract from the data sheet for the op-amp is given below.
The op-amp is powered from a ±15V supply.

Parameter	Value
Open-loop gain	$3{\cdot}0 \times 10^5$
Input Impedance	$2{\cdot}0 \times 10^{12}\Omega$
Saturation voltage	±13·5 V
Slew Rate	$10\,V\mu s^{-1}$
Gain-bandwidth product	5 MHz

(a) Calculate the voltage gain of this amplifier.

.....

.....

[1]

(b) What is the input impedance of this voltage amplifier?

.....

[1]

(c) A test signal of amplitude 40 mV is applied to the input.

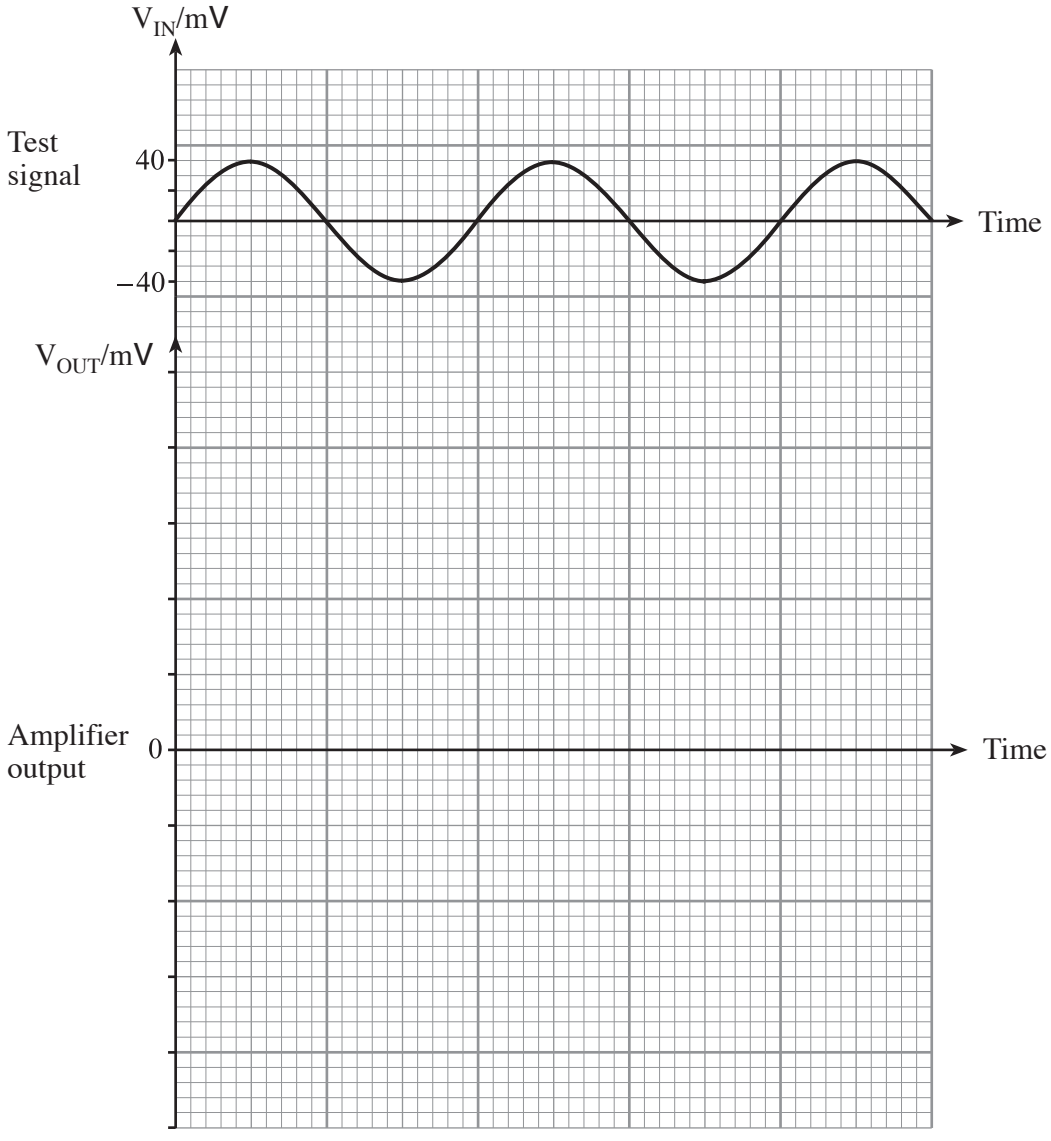
(i) Calculate the amplitude of the output voltage.

.....

.....

[1]

(ii) Complete the graph to show the output voltage.
Label any significant voltages.



[2]

(d) What is the maximum amplitude of input voltage, which does not produce clipping distortion?

.....

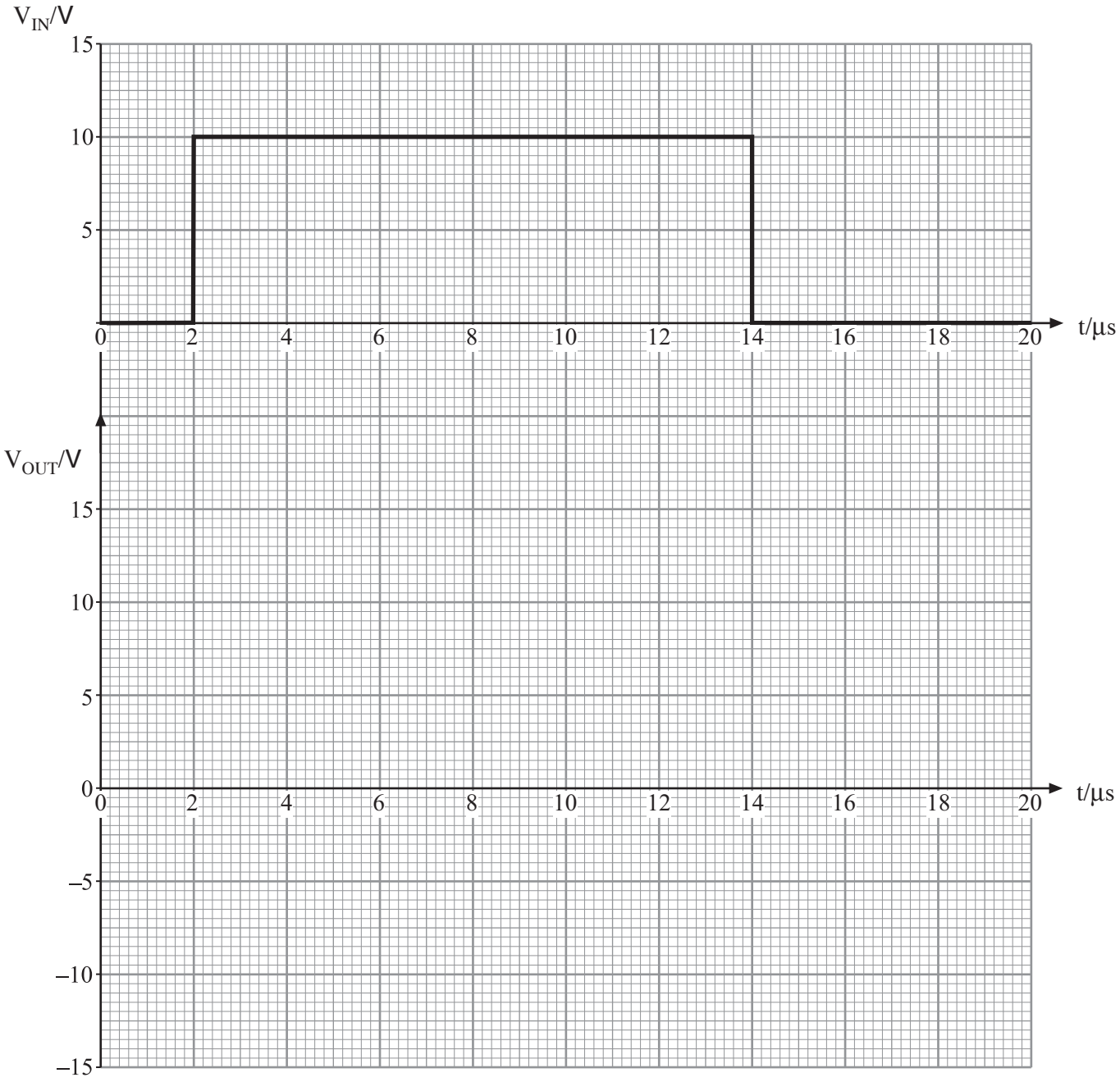
.....

[1]

THIS QUESTION CONTINUES ON THE NEXT PAGE

Examiner only

(e) The following signal is applied to the input to illustrate the effect of slew-rate on the output of the voltage amplifier.
Draw the output voltage on the axes below.
V_{OUT} is initially at 0 V.



[4]

Examiner only

FOR USE ONLY IF YOU HAVE MADE SUBSTANTIAL DELETIONS IN PARTS OF YOUR ANSWERS OR NEED MORE SPACE TO COMPLETE THEM. BE SURE TO INDICATE THE QUESTIONS CONCERNED.