| Candidate Name | Centre Number | Candidate Number |
|---|---|---|
| | | |

**WELSH JOINT EDUCATION COMMITTEE**
**General Certificate of Education**
**Advanced Subsidiary/Advanced**

WJEC CBAC

**CYD-BWYLLGOR ADDYSG CYMRU**
**Tystysgrif Addysg Gyffredinol**
**Uwch Gyfrannol/Uwch**

381/01

# ELECTRONICS

## ET1

P.M. MONDAY, 16 January 2006

(1½ hours)

## ADDITIONAL MATERIALS

In addition to this examination paper, you will need a calculator.

## INSTRUCTIONS TO CANDIDATES

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

## INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

| For Examiner's use only. | |
|---|---|
| **1** | |
| **2** | |
| **3** | |
| **4** | |
| **5** | |
| **6** | |
| **7** | |
| **8** | |
| **Total** | |

No certificate will be awarded to a candidate detected in any unfair practice during the examination.

## INFORMATION FOR THE USE OF CANDIDATES

**Preferred Values for resistors**
The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

**RC networks**

$V_C = V_O (1 - e^{-t/RC})$ for a charging capacitor

$V_C = V_O e^{-t/RC}$ for a discharging capacitor

$$t = -RC \ln\left(1 - \frac{V_c}{V_o}\right)$$ For a charging capacitor

$$t = -RC \ln\left(\frac{V_c}{V_o}\right)$$ For a discharging capacitor

**Alternating Voltages** $V_o = V_{rms}\sqrt{2}$

**Silicon Diode** $V_F \approx 0{\cdot}7V$

**Bipolar Transistor**

$$h_{FE} = \frac{I_C}{I_B}$$ Current gain

$V_{BE} \approx 0{\cdot}7V$ in the on state

**MOSFETs** $I_D = g_M V_{GS}$

**Operational amplifier**

$$G = -\frac{R_F}{R_{IN}}$$ Inverting amplifier

$$G = 1 + \frac{R_F}{R_1}$$ Non-inverting amplifier

$$V_{OUT} = -R_F\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$$ Summing amplifier

$$\text{Slew Rate} = \frac{\Delta V_{OUT}}{\Delta t}$$ Slew rate

**555 Monostable** $T = 1{\cdot}1\ RC$

**555 Astable**

$t_H = 0{\cdot}7\ (R_A + R_B)C$

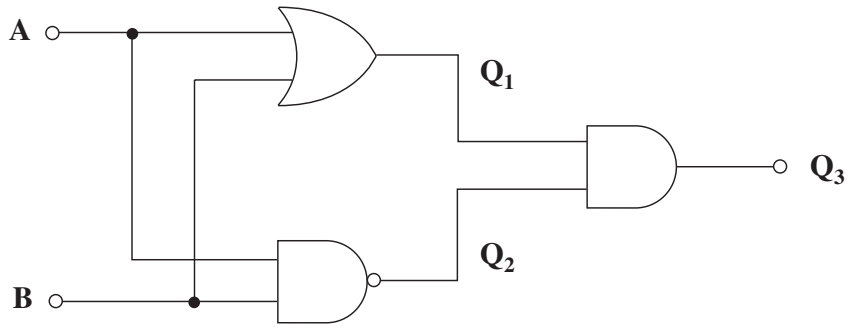
$t_L = 0{\cdot}7\ R_B C$

$$f = \frac{1 \cdot 44}{(R_A + 2R_B)C}$$

**Schmitt Astable**

$$f \approx \frac{1}{RC}$$

**1.** Here is a logic system.




*(a)* Write down the Boolean expression for $\mathbf{Q_1}$, $\mathbf{Q_2}$ and $\mathbf{Q_3}$ in terms of **A** and **B**. [3]

$\mathbf{Q_1}$ = .....

$\mathbf{Q_2}$ = .....

$\mathbf{Q_3}$ = .....

*(b)* Complete the truth table for the system. [2]

| **INPUTS** | | **OUTPUTS** | | |
|---|---|---|---|---|
| B | A | $Q_1$ | $Q_2$ | $Q_3$ |
| 0 | 0 | | | |
| 0 | 1 | | | |
| 1 | 0 | | | |
| 1 | 1 | | | |

*(c)* Name the single, 2-input logic gate that would produce the same function as the system shown in part *(a)*. [1]

Name of gate .....

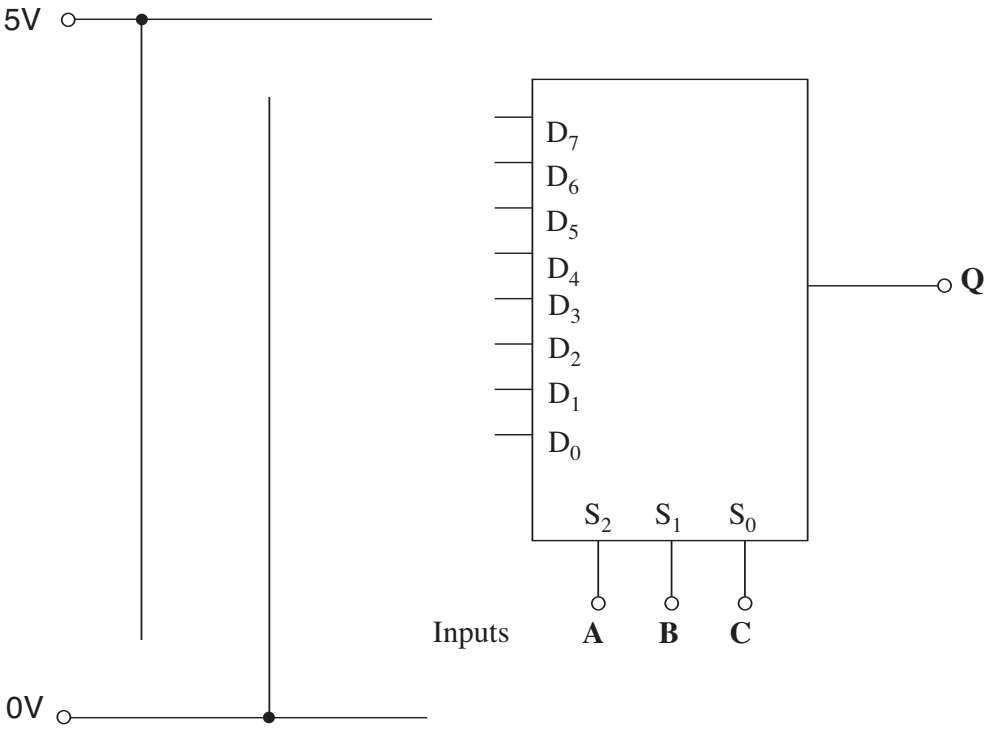
**2.** A logic system must generate the output Q where

$$Q = \overline{C} \,.\, \overline{B} \,.\, A + \overline{B} \,.\, \overline{A}$$

*(a)* Complete the truth table for this system. [1]

| C | B | A | Q |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

*(b)* Complete the following diagram to show how the data inputs of an 8:1 multiplexer should be connected to perform this function. The input $S_2$ is the **most significant** select input. [2]




*(c)* Give **one** advantage of using a multiplexer in place of logic gates to perform logic functions.

[1]

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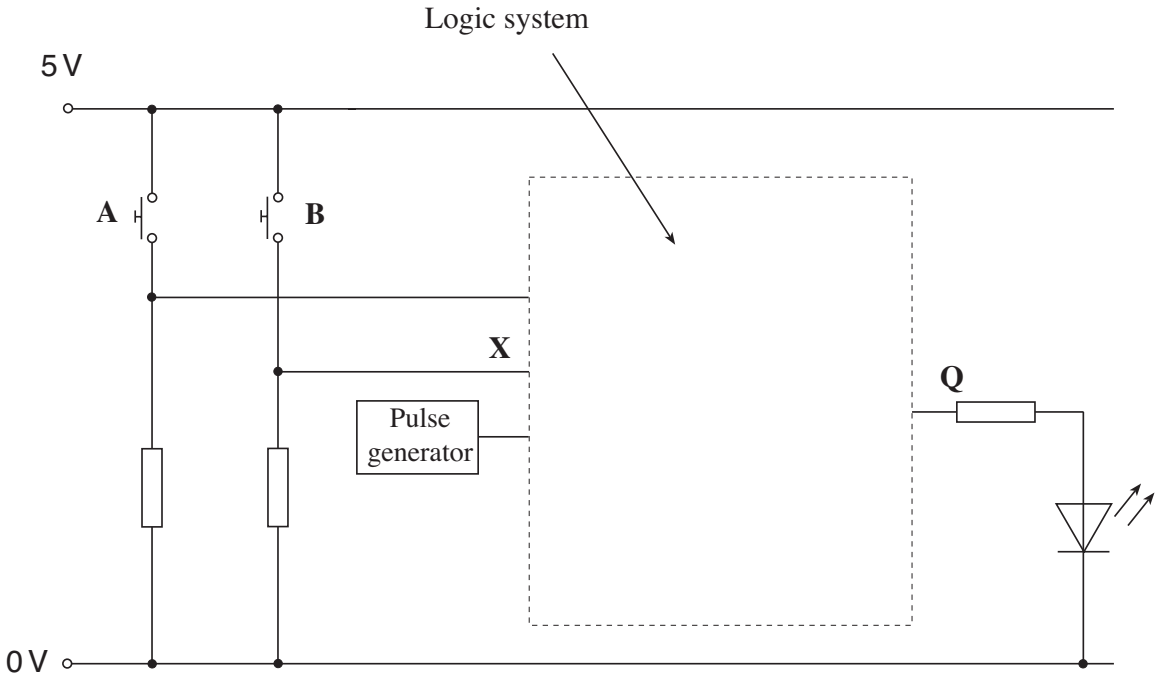
**3.** The diagram shows part of an alarm system used to protect DVD players in a shop. When the DVD player is in place pressure switches **A** and **B** are closed.




*(a)* What is the logic level at point **X** when the switch B is open (OFF)? [1]

Logic level at **X** .....

*(b)* What logic level at **Q** causes the LED to light? [1]

Logic level at **Q** .....

*(c)* Design a logic system, using **two 2-input** logic gates, such that the LED will flash only if the DVD player is lifted off **both** pressure switches. Draw your design in the box above showing the two logic gates and appropriate connections. [3]

**4.** ***(a)*** Simplify the following expressions. [2]

(i) A.0 = .....

(iii) $A + \overline{A}.B$ = .....

.....

| B \ A | 0 | 1 |
|---|---|---|
| 0 | | |
| 1 | | |

*(b)* (i) Complete the Karnaugh map for the following expression. [1]

$$Q = \overline{D}.\overline{C}.\overline{B}.\overline{A} + C.B.A + D.C.\overline{B}.A + C.B.\overline{A} + D.\overline{C}.\overline{B}.\overline{A}$$

| D.C \ B.A | 0.0 | 0.1 | 1.1 | 1.0 |
|---|---|---|---|---|
| 0.0 | | | | |
| 0.1 | | | | |
| 1.1 | | | | |
| 1.0 | | | | |

(ii) Simplify the expression for the output Q of this logic system. Show and label on the map any groups you created to produce this expression. [4]

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*(c)* Apply DeMorgan's theorem to the following expression **and** simplify the result. [3]

$$Q = \overline{\overline{A} + (\overline{B.A})}$$

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**Turn over.**

**5.** *(a)* Give **one** advantage and **one** disadvantage of coding information using BCD rather than Binary. [2]

(i) Advantage: .....

(ii) Disadvantage: .....

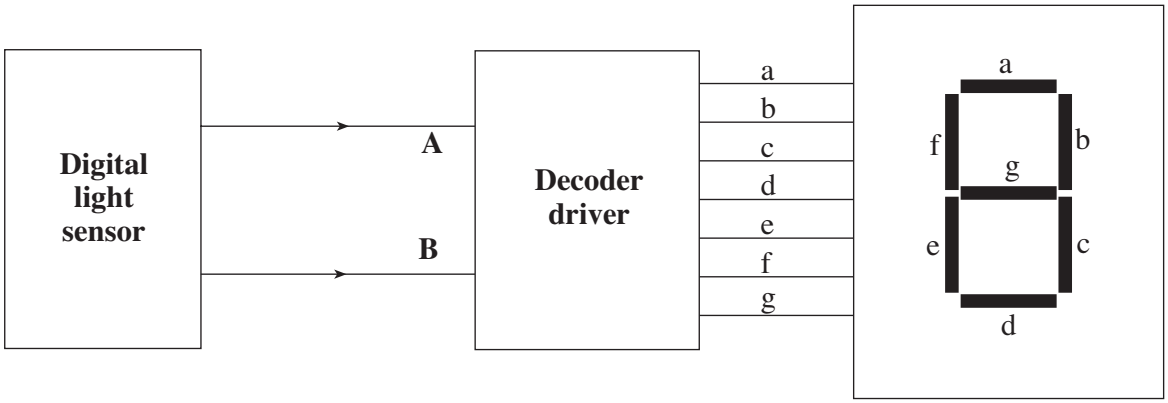
*(b)* A camera light meter is fitted with a light sensor which produces a 2-bit output. The sensor is connected through a decoder-driver to a 7-segment display.

If it is too dark to take a photograph the display shows the letter 

If the light is satisfactory it displays the letter 

If there is too much light the display show the letter 

A block diagram for the system is shown below.




The sensor produces the digital signals shown in the following table.

| Light Intensity | **A** | **B** |
|---|---|---|
| too dark | 0 | 0 |
| satisfactory | 0 | 1 |
| | 1 | 0 |
| too light | 1 | 1 |

(i) Complete the following table to show the seven signals **a** to **g** needed to light each display. Logic 1 from the decoder will light each segment. [2]

| Display | A | B | a | b | c | d | e | f | g |
|---|---|---|---|---|---|---|---|---|---|
|  | 0 | 0 | | | | | | | |
|  | 0 | 1 | | | | | | | |
| | 1 | 0 | | | | | | | |
|  | 1 | 1 | | | | | | | |

(ii) Which single logic gate in the decoder would generate the required signal for segment e? [1]

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(iii) Which segment does not require a logic gate to control it? [1]

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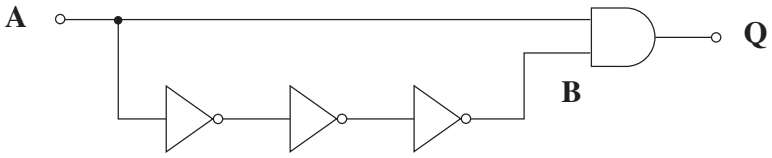
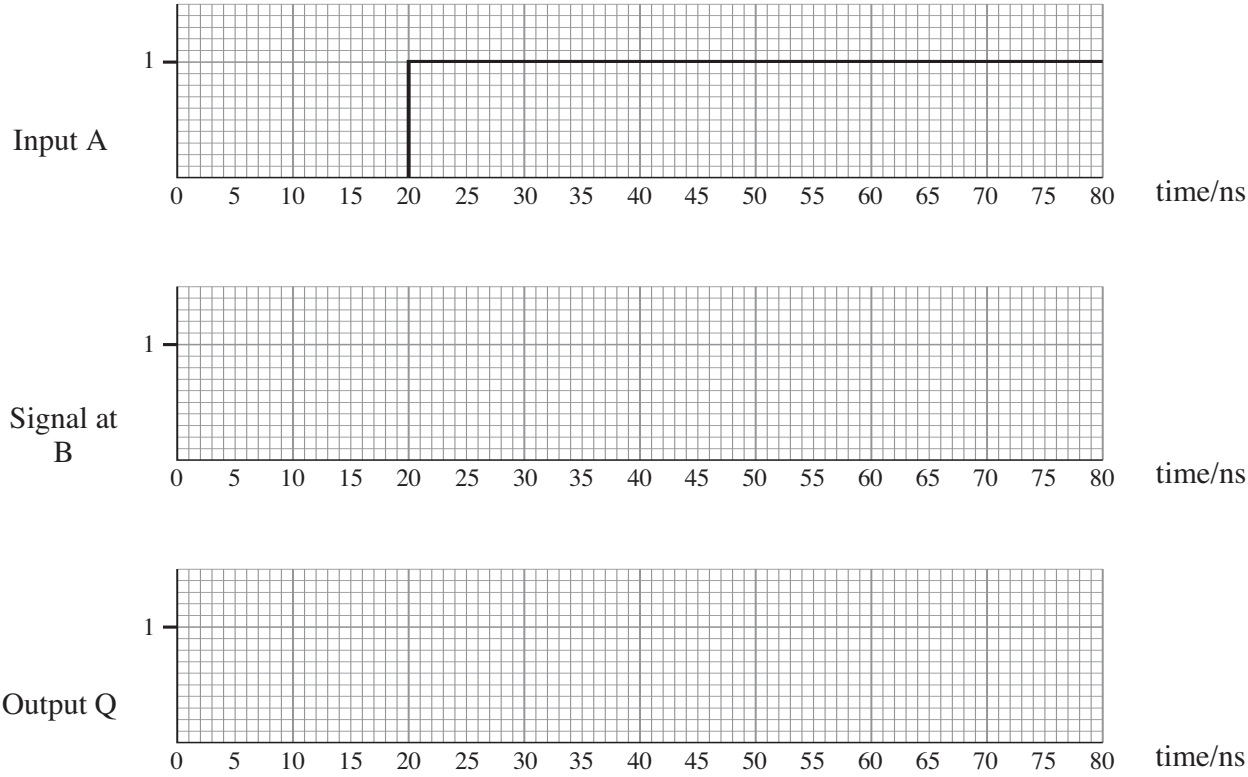
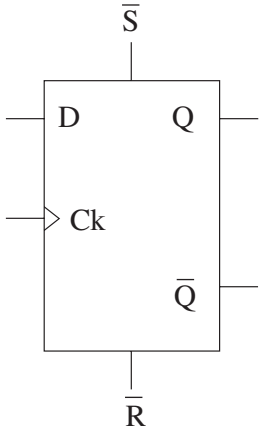
**6.** The following diagram shows the circuit for a *transition gate*.
The logic gates each have a propagation delay of 5 ns.




*(a)* Complete the following diagram to show how the signal at **B** and output **Q** change when the pulse shown is applied to input **A**.
**Initially, output Q is at logic 0.** [5]




*(b)* The D-type flip flop shown below contains a transition gate.




(i) What job does the transition gate perform within the D-type? [1]

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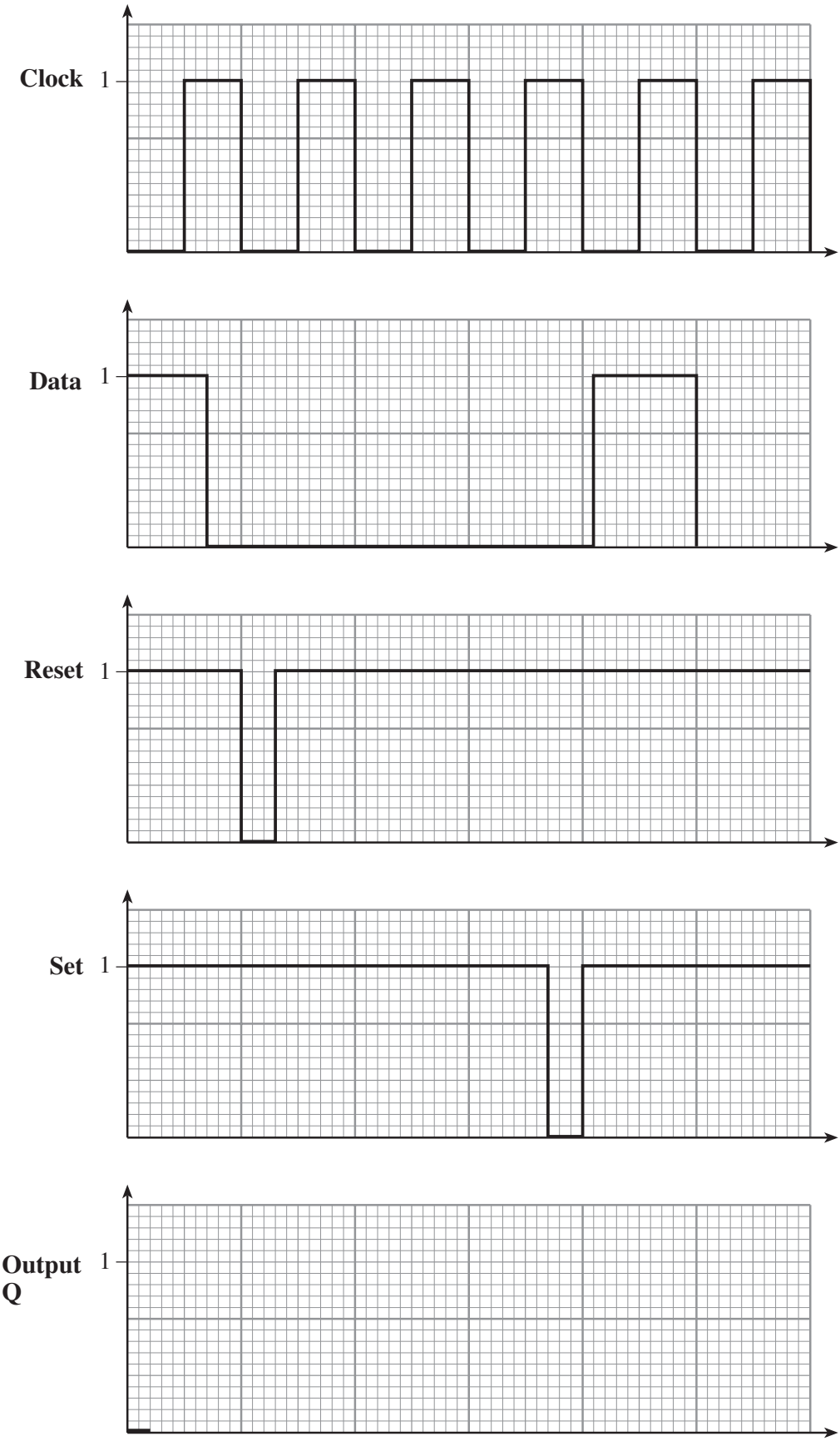
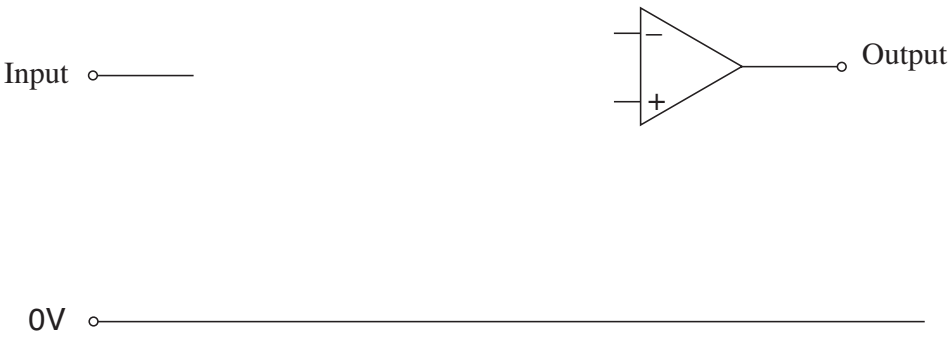
(ii) The signals shown in the timing diagrams below are applied to the *rising-edge triggered* D-type. Complete the timing diagram for the output Q.
The SET and RESET are *active low.* [Ignore propagation delays.] [4]



**7.** *(a)* Draw the circuit diagram for an inverting voltage amplifier, based on an op-amp. [3]




*(b)* Select suitable value resistors to give a voltage gain of -24. [2]

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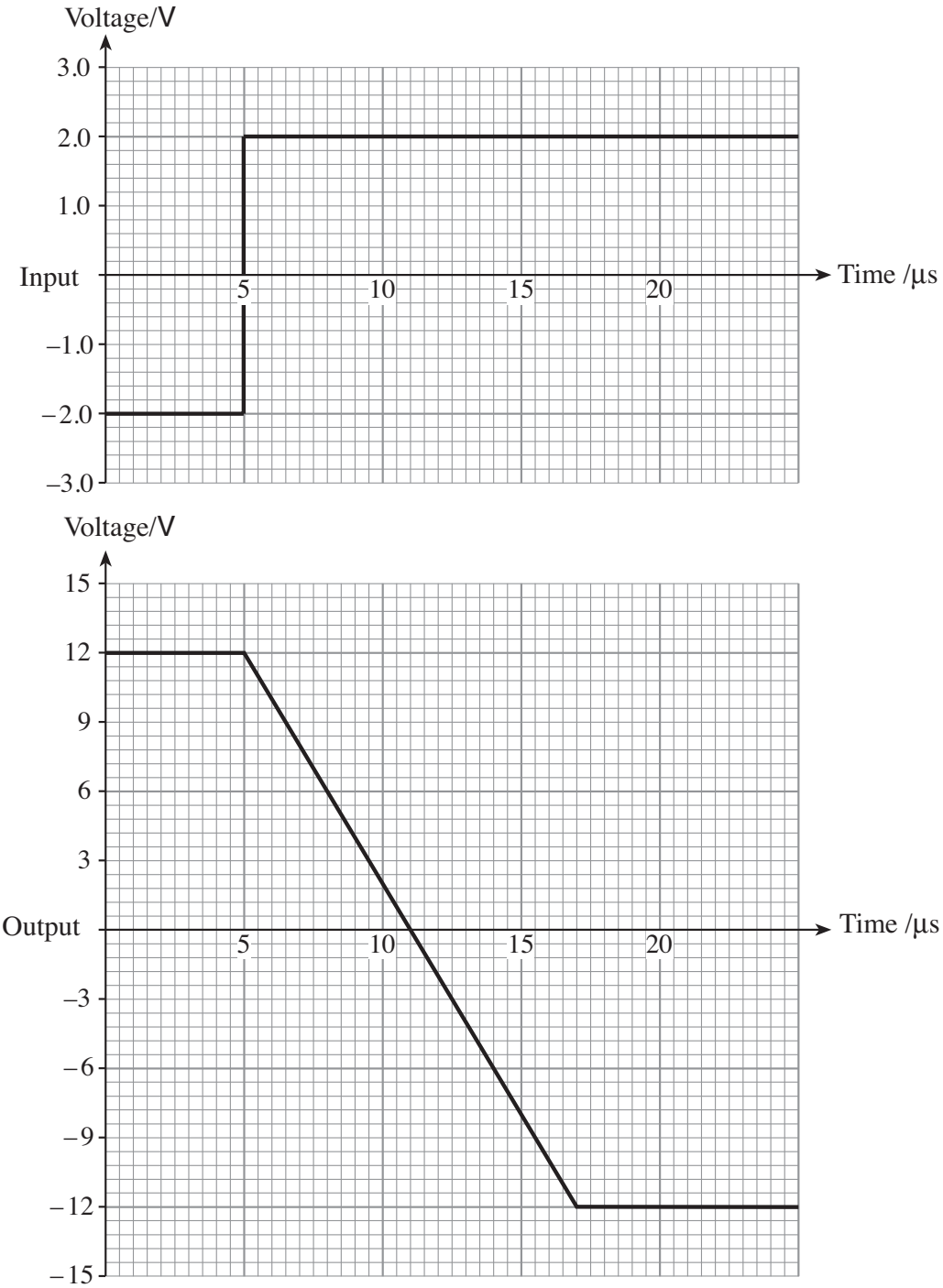
*(c)* The upper graph shows a signal applied to the input of the voltage amplifier. The lower graph shows the resulting output.




Estimate the slew-rate for the op-amp, **giving the appropriate unit**. [3]

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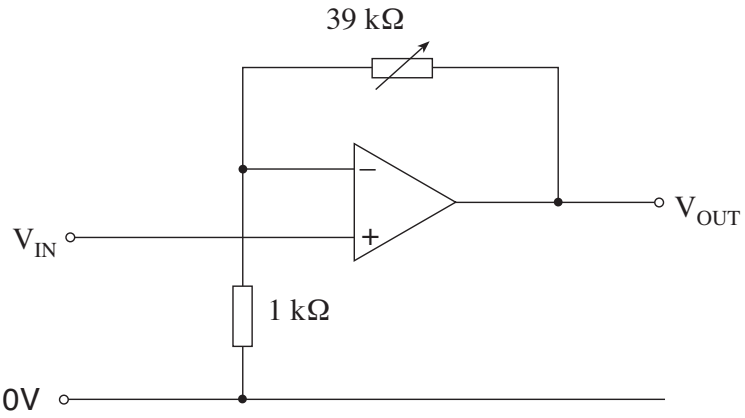
**8.** An extract from the data sheet of an op-amp is shown in the following table.

| Parameter | Value |
|---|---|
| Input Impedance | 10 MΩ |
| Output Impedance | 100 Ω |
| Open Loop Gain | $10^6$ |
| Gain Bandwidth Product | 1.2 MHz |

The circuit diagram shows the op-amp set up as a voltage amplifier. The variable resistor allows the user to change the gain. The value of this resistor can be altered from 0 to 39 kΩ.




The op-amp is powered from a ±12V supply and saturation occurs at ±11V.

*(a)* What is the input impedance of this amplifier? [1]

.....

*(b)* Calculate the maximum and minimum voltage gain of the amplifier.

Maximum gain = ..... [1]

Minimum gain = ..... [1]

*(c)* (i) The variable resistor is adjusted to give a voltage gain of 25. Calculate the bandwidth of the amplifier when the voltage gain is 25. [2]

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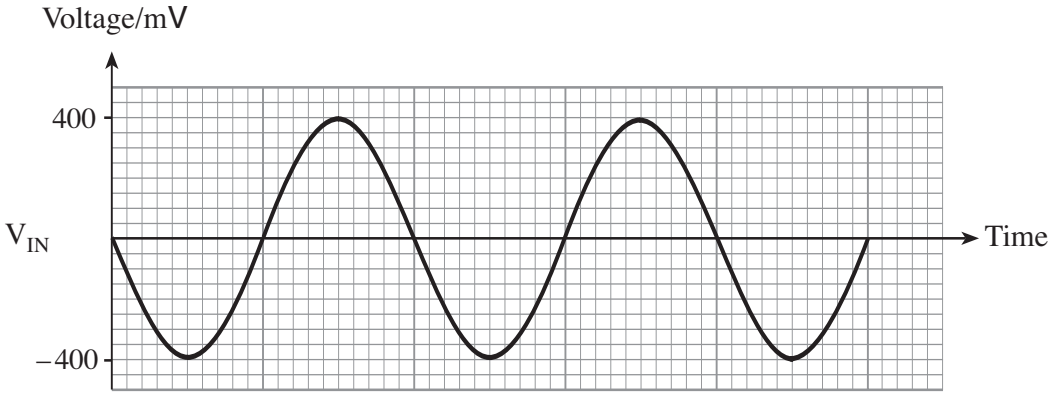
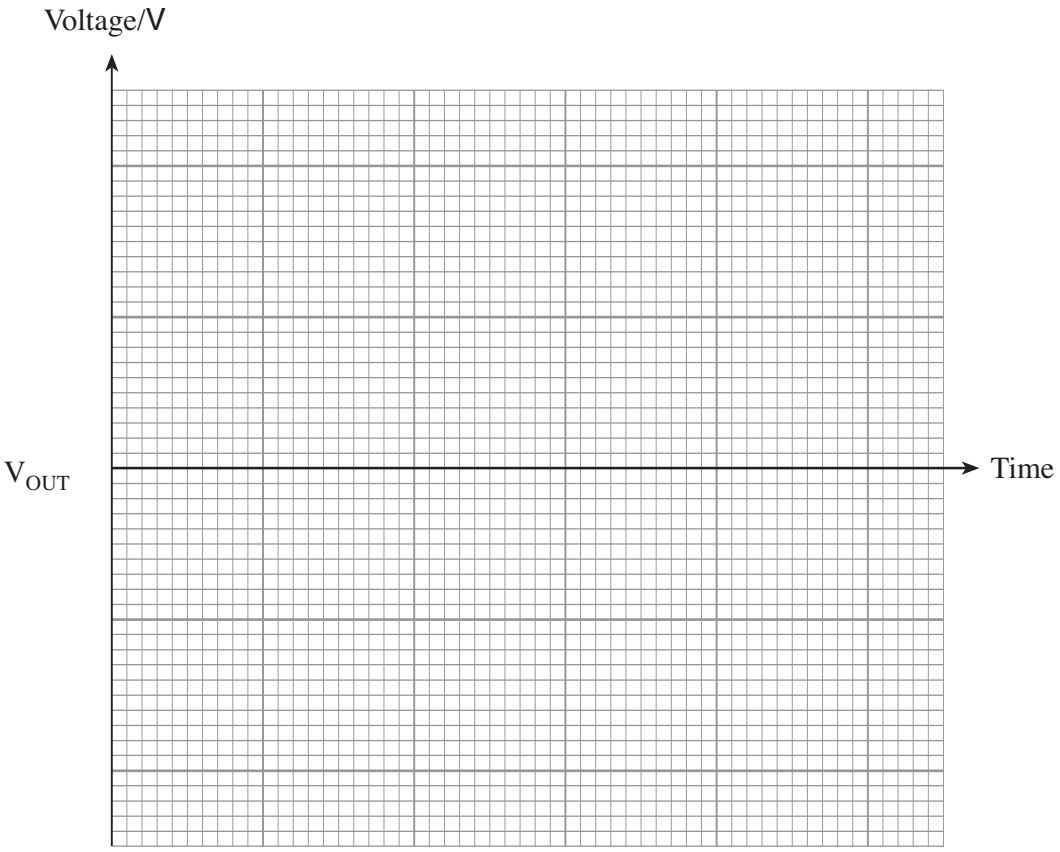
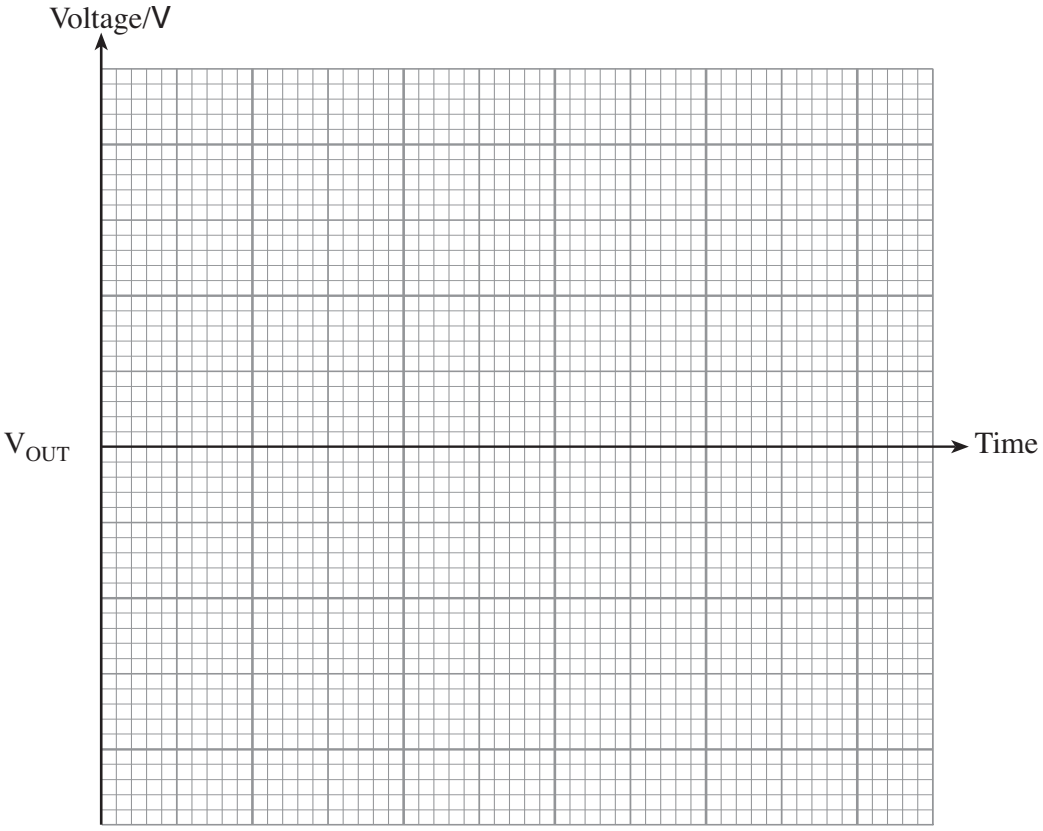
(ii) With the voltage gain set to 25 the signal $V_{IN}$ is applied to the input.
Draw the output voltage $V_{OUT}$ on the axes provided. Label important voltage values on the axes. [3]




**The question continues on page 16**

*(d)* The variable resistor is now adjusted to give a voltage gain of 35. Sketch the output voltage on the axes provided. [2]




*(e)* State what change, **if any**, occurred to the following when the voltage gain of the amplifier was increased.

(i) Input impedance ..... [1]

(ii) The bandwidth ..... [1]

**FOR USE ONLY IF YOU HAVE MADE SUBSTANTIAL DELETIONS IN PARTS OF YOUR ANSWERS OR NEED MORE SPACE TO COMPLETE THEM. BE SURE TO INDICATE THE QUESTIONS CONCERNED.**