OXFORD CAMBRIDGE AND RSA EXAMINATIONS
AS GCE

F612/01

ELECTRONICS

Signal Processors

THURSDAY 21 MAY 2015: Afternoon
DURATION: 1 hour 30 minutes
plus your additional time allowance

MODIFIED ENLARGED

Candidate forename		Candidate surname	

Centre number						Candidate number				

Candidates answer on the Question Paper.

OCR SUPPLIED MATERIALS:
None

OTHER MATERIALS REQUIRED:
Scientific calculator

A SCIENTIFIC CALCULATOR MAY BE USED FOR THIS PAPER

READ INSTRUCTIONS OVERLEAF

DC (RW/SW) 6084013811 112997/1

INSTRUCTIONS TO CANDIDATES

Write your name, centre number and candidate number in the boxes on the first page. Please write clearly and in capital letters.

Use black ink. HB pencil may be used for graphs and diagrams only.

Answer ALL the questions.

Read each question carefully. Make sure you know what you have to do before starting your answer.

Write your answer to each question in the space provided. Additional paper may be used if necessary but you must clearly show your candidate number, centre number and question number(s).

INFORMATION FOR CANDIDATES

The number of marks is given in brackets [ ] at the end of each question or part question.

The total number of marks for this paper is 90.

You will be awarded marks for your Quality of Written Communication.

You are advised to show all the steps in any calculations.

Any blank pages are indicated.

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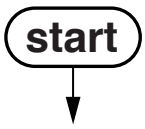
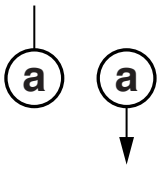
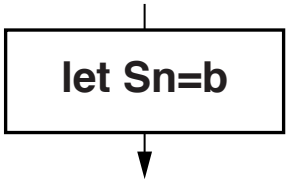
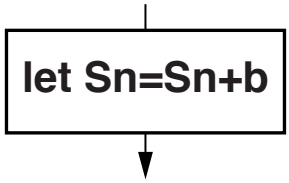
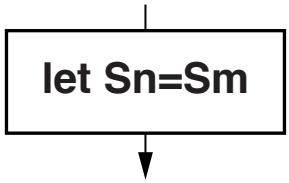
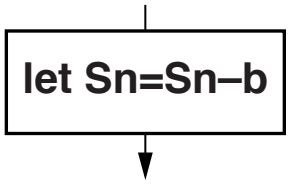
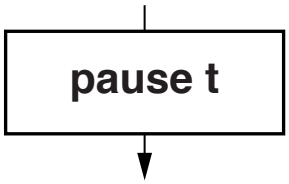
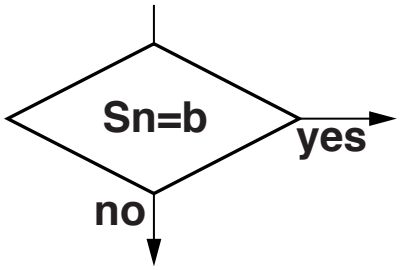
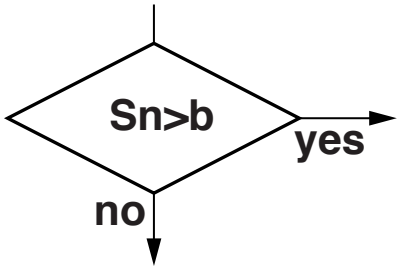
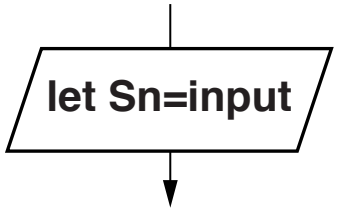
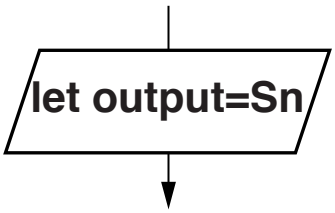
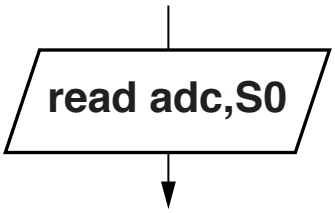
DATA SHEET

SYMBOL	MEANING
	start the program
	link to part of the program with the same label a
	stop the program
	place the byte b in register Sn
	add the byte b to the byte in register Sn
	copy the byte in register Sm into register Sn
	subtract the byte b from the byte in register Sn
	introduce a time delay of t milliseconds

	**branch if the byte in register Sn is equal to the byte b**
	**branch if the byte in register Sn is greater than the byte b**
	**copy the byte at the input port to register Sn**
	**copy the byte in register Sn to the output port**
	**activate the analogue-to-digital converter and store the result in register S0**

DATA SHEET

Unless otherwise indicated, you can assume that:

op-amps are run off supply rails at +15V and –15V

logic circuits are run off supply rails at +5V and 0V.

resistance	$R = \frac{V}{I}$
power	$P = VI$
series resistors	$R = R_1 + R_2$
time constant	$\tau = RC$
monostable pulse time	$T = 0.7\,RC$
relaxation oscillator period	$T = 0.5\,RC$
frequency	$f = \frac{1}{T}$
voltage gain	$G = \frac{V_{out}}{V_{in}}$
open-loop op-amp	$V_{out} = A(V_+ - V_-)$
non-inverting amplifier gain	$G = 1 + \frac{R_f}{R_d}$
inverting amplifier gain	$G = -\frac{R_f}{R_{in}}$

summing amplifier $$-\frac{V_{out}}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} \ldots$$

break frequency $$f_0 = \frac{1}{2\pi RC}$$

Boolean Algebra

$$A.\overline{A} = 0$$

$$A + \overline{A} = 1$$

$$A.(B + C) = A.B + A.C$$

$$\overline{A.B} = \overline{A} + \overline{B}$$

$$\overline{A + B} = \overline{A}.\overline{B}$$

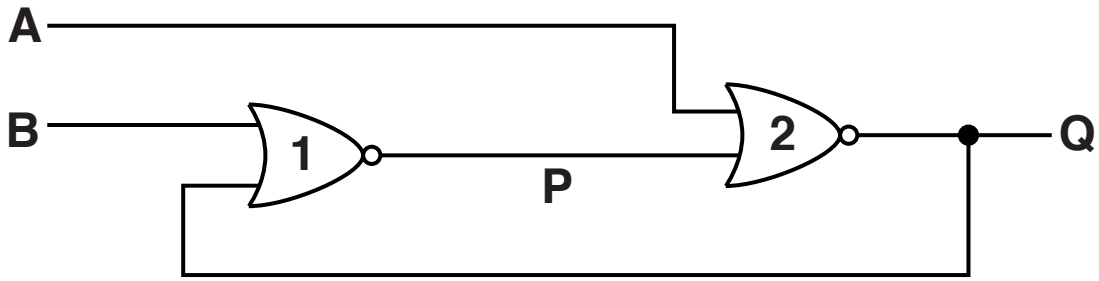
$$A + A.B = A$$

$$A.B + \overline{A}.C = A.B + \overline{A}.C + B.C$$

Answer ALL the questions.

1 The circuit of Fig. 1.1 is a NOR-gate bistable.

FIG. 1.1



(a) The output of a NOR-gate bistable can be SET and RESET with appropriate signals at the ACTIVE HIGH INPUTS.

(i) Explain the meaning of the terms SET, RESET and ACTIVE HIGH INPUT.

_____

_____

_____

_____

_____ **[3]**

(ii) State what happens to the output Q when both inputs go low.

_____

_____ **[1]**

(b) (i) Complete the truth table below for gate 2 of Fig. 1.1.

A	P	Q
1	1	
1	0	
0	1	
0	0	

[1]

(ii) Explain the sequence of signals required to make the bistable store a 1.

_____

_____

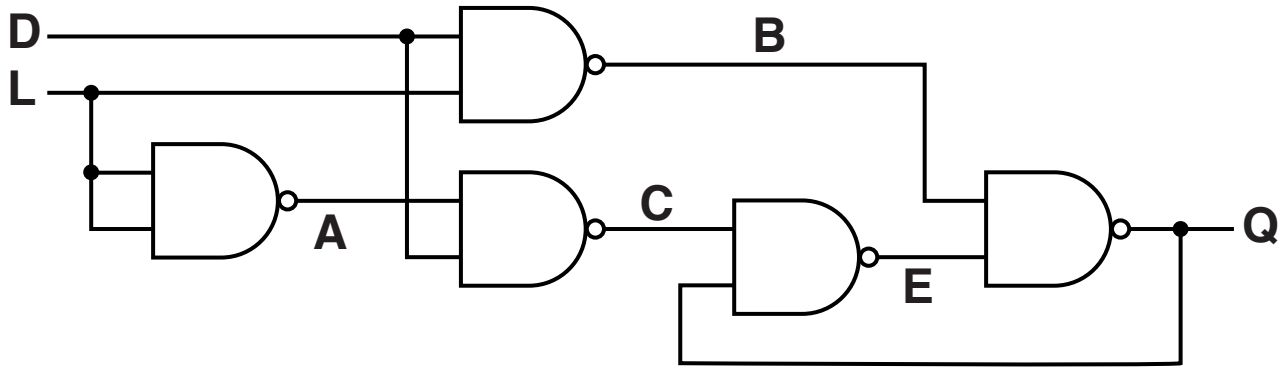
_____

_____

_____ **[3]**

2 The circuit of Fig. 2.1 is a latch made from NAND gates.

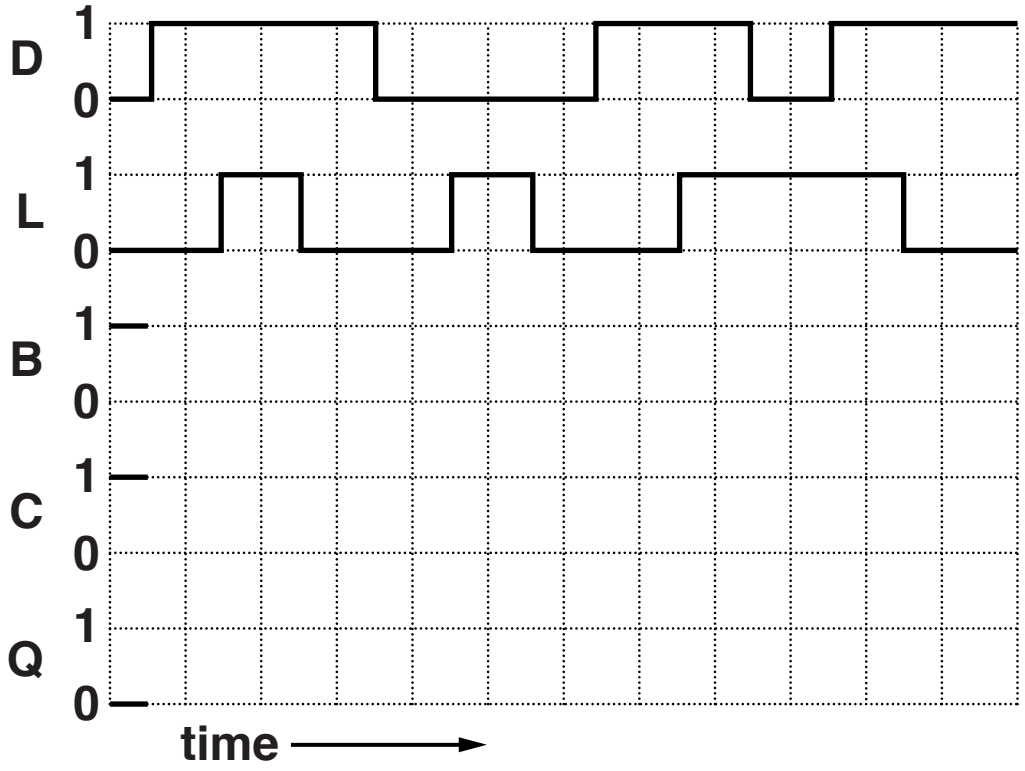
FIG. 2.1



The state of D is copied to Q whenever the enable input L goes high.

Complete the timing diagram of Fig. 2.2.

FIG. 2.2



[5]

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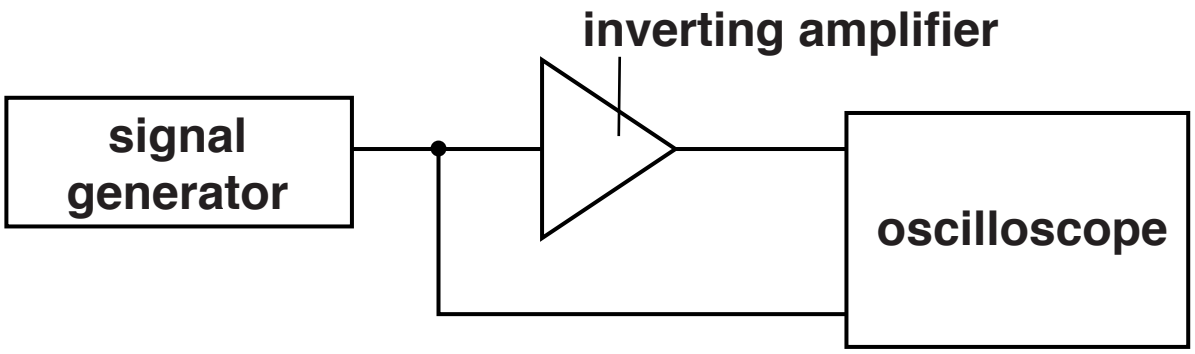
3 A student uses the test arrangement of Fig. 3.1 to verify the transfer characteristic of an inverting amplifier.

FIG. 3.1



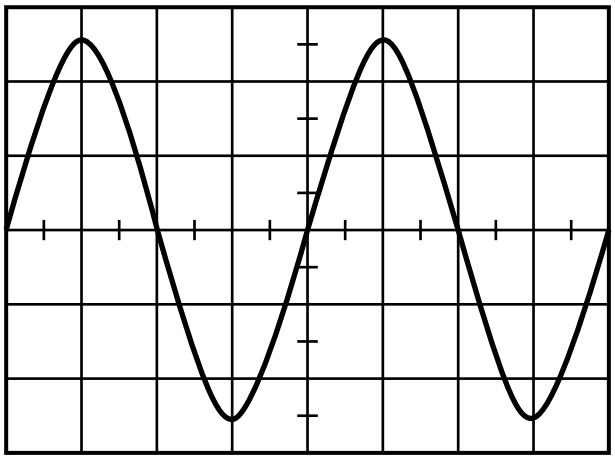
(a) The inverting amplifier has the following properties.

voltage gain of –2.5

input impedance of 30 kΩ

(i) **Fig. 3.2 shows an oscilloscope trace of the signal at the OUTPUT of the amplifier.**

FIG. 3.2



On Fig. 3.2, sketch the trace of the signal at the INPUT of the amplifier.

Both traces have the same oscilloscope vertical amplifier setting of 2V/div. **[3]**

(ii) **Draw in the space below to show how the amplifier can be constructed from an op-amp and resistors. Show all component values.**

[4]

(b) The amplifier of Fig. 3.1 alters some properties of the input signal but leaves others unaltered.

(i) State ONE property of the input signal which is altered by the amplifier.

_____

_____ **[1]**

(ii) State TWO properties of the input signal which are NOT altered by the amplifier.

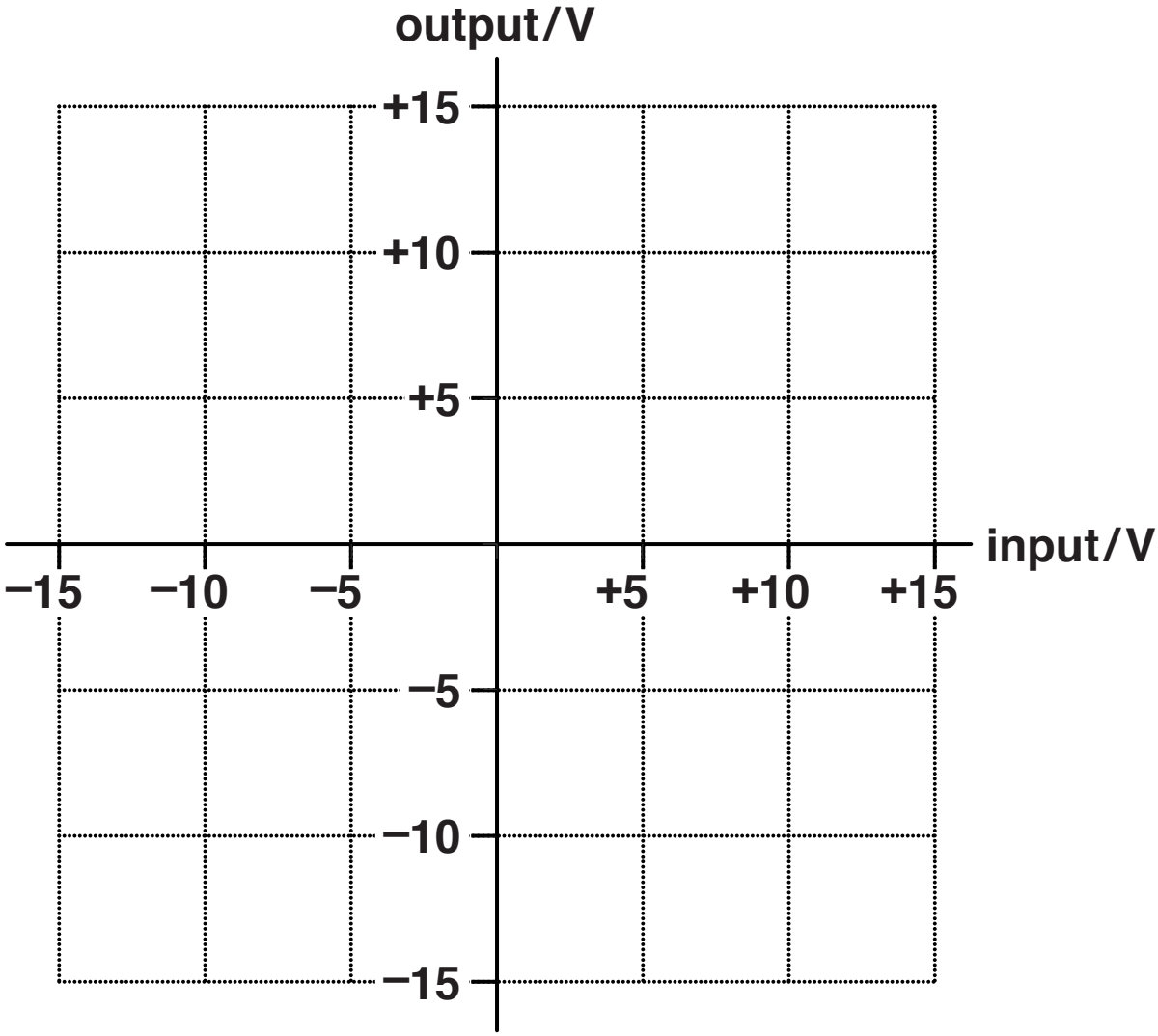
_____

_____

_____ **[2]**

(c) Sketch the transfer characteristic of the inverting amplifier of Fig. 3.1 on the axes of Fig. 3.3.

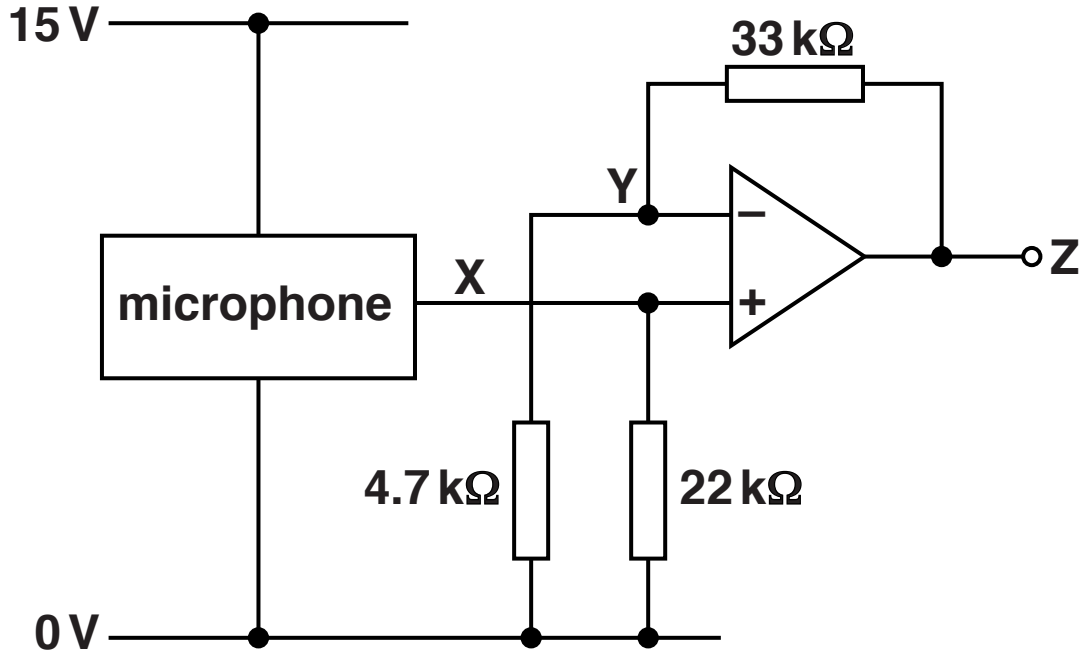
FIG. 3.3



[3]

4 The circuit of Fig. 4.1 shows a microphone connected to an amplifier.

FIG. 4.1



(a) During a test of the system, the microphone produces a signal at X which has an amplitude of 150 mV.

(i) Calculate the amplitude of the signal at Z.

amplitude = _____ V [3]

(ii) Use the transfer characteristics of an op-amp to explain why the signals at X and Y are almost identical.

_____

_____

_____

_____

_____

_____ **[4]**

(b) The microphone has an output impedance of 12 kΩ.

(i) Explain why replacing the 22 kΩ resistor with a 120 kΩ resistor would improve the performance of the circuit.

_____

_____

_____

_____

_____

_____ **[4]**

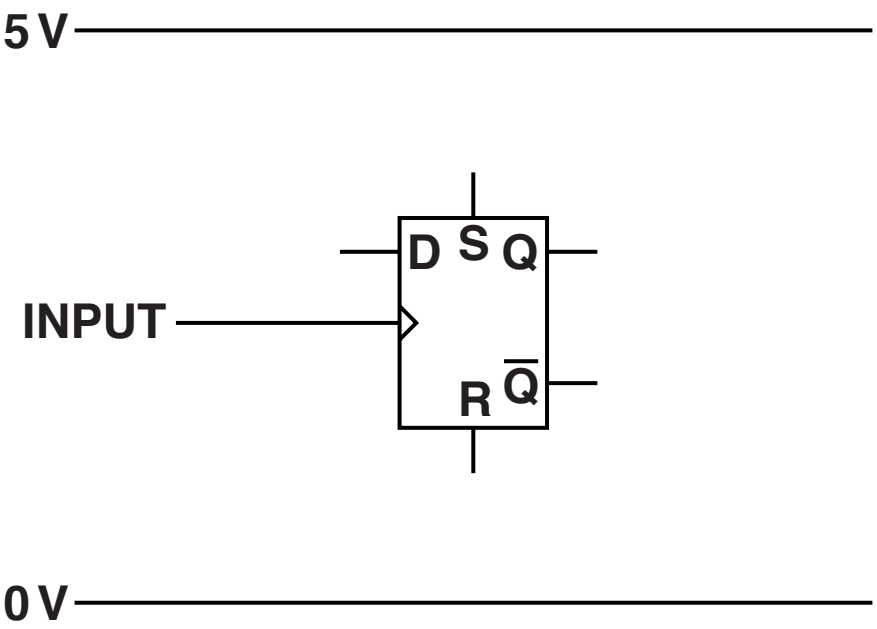
(ii) In another test, the amplitude of the signal at X is 250 mV when the 22 kΩ resistor is in place.

Calculate the amplitude of the signal at X when the 22 kΩ resistor is replaced with a 120 kΩ resistor.

amplitude = _____mV [4]

5 Fig. 5.1 contains the circuit symbol for a D flip-flop.

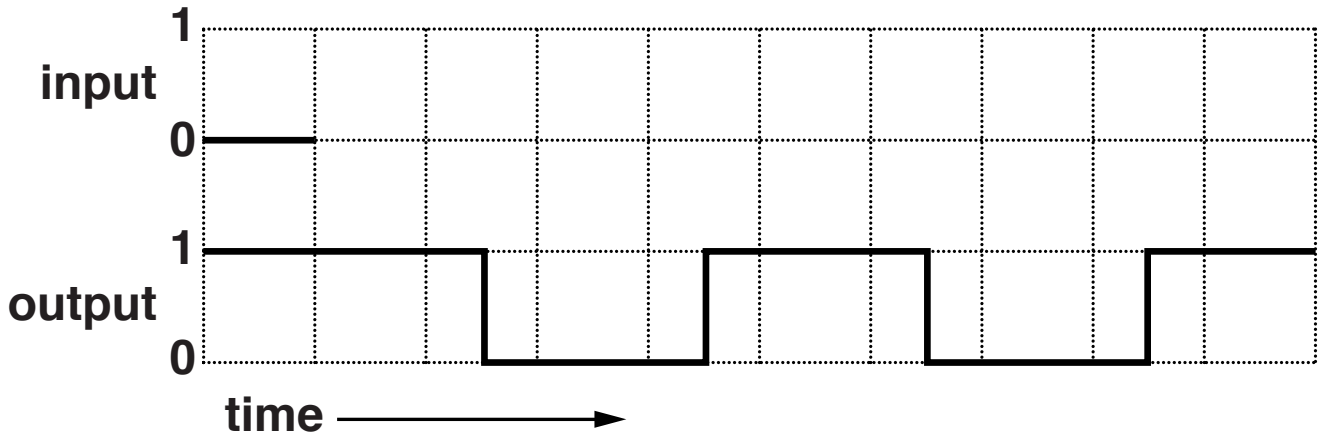
FIG. 5.1



(a) (i) Draw on Fig. 5.1 to show how the flip-flop should be connected to count pulses at the terminal labelled INPUT.
Label the OUTPUT of the counter. [3]

(ii) Complete the timing diagram of Fig. 5.2 to show the behaviour of the counter of Fig. 5.1.

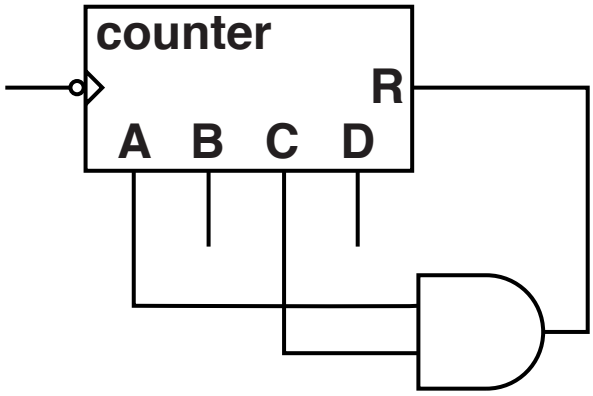
FIG. 5.2



[2]

(b) Fig. 5.3 shows a four-bit counter and a logic gate.

FIG. 5.3



(i) Explain the effect of the logic gate on the behaviour of the circuit of Fig. 5.3.

_____

_____

_____

_____ **[2]**

(ii) Complete the pulse table for the circuit of Fig. 5.3.

pulse	A	B	C	D
0	1	1	0	0
1				
2				
3				
4				

[3]

(iii) A signal of frequency 15 kHz is applied to the input of the circuit of Fig. 5.3.

Calculate the frequency of the signal at C.

frequency = _____ kHz [1]

6 The circuit of Fig. 6.1 opposite makes a pair of LEDs glow in a continuous sequence.

(a) Show that each cycle of the sequence lasts for about 35 seconds.

[4]

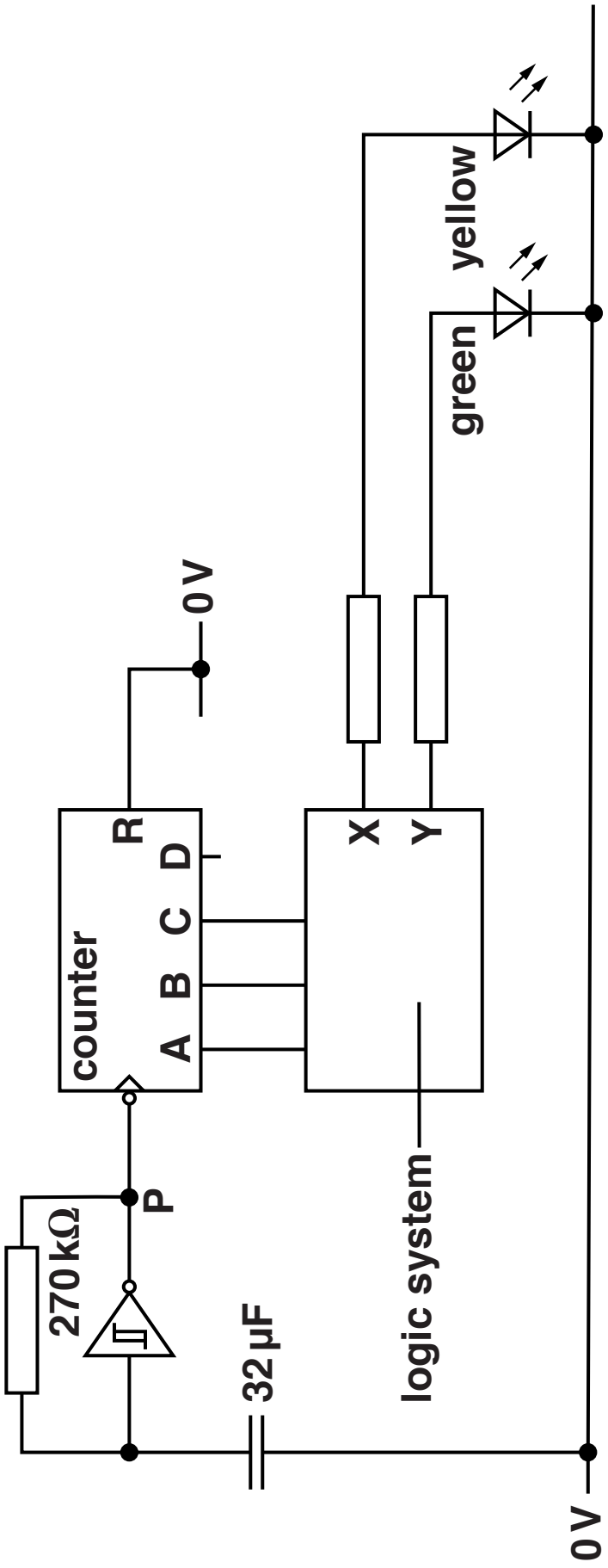

0 V
yellow
green
R
D
C
B
A
counter
X
Y
P
270 kΩ
32 µF
logic system
0 V

FIG. 6.1

(b) Fig. 6.2 shows part of the logic system of Fig. 6.1.

Complete the timing diagram of Fig. 6.3.

FIG. 6.2

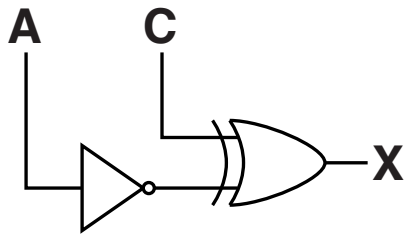
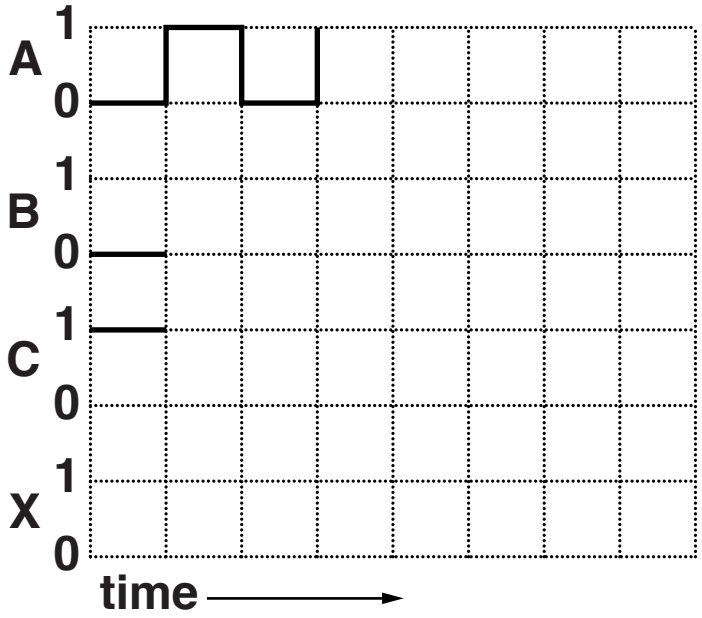


FIG. 6.3



[4]

(c) The green LED connected to Y only glows for these three states of the counter:

CBA = 010

CBA = 110

CBA = 011

(i) Write down a Boolean expression for Y in terms of C, B and A.

You do not have to simplify it.

[1]

(ii) Use the theorems of Boolean algebra to show that $Y = \overline{C}.B + B.\overline{A}$.

[2]

(iii) Draw a NAND gate circuit in the space below to show how Y can be generated from C, B and A.

[3]

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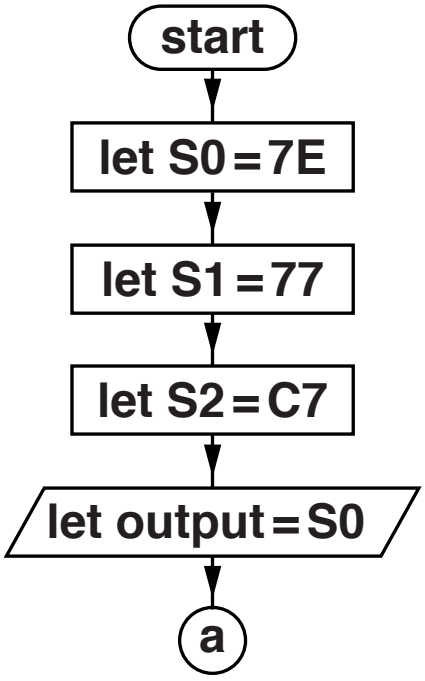
7 The microcontroller system of Fig. 7.1 opposite is programmed to act as a flood alarm.

Each sensor is in a different location and only outputs a 1 when it is underwater.

(a) The first part of the program flowchart is shown in Fig. 7.2.

FIG. 7.2



(i) Complete the table below.

HEXADECIMAL	BINARY
7E	01111110
77	
C7	

[1]

(ii) Explain, in detail, the effect of copying the contents of register S0 to the output port.

_____

_____

_____

_____ **[3]**

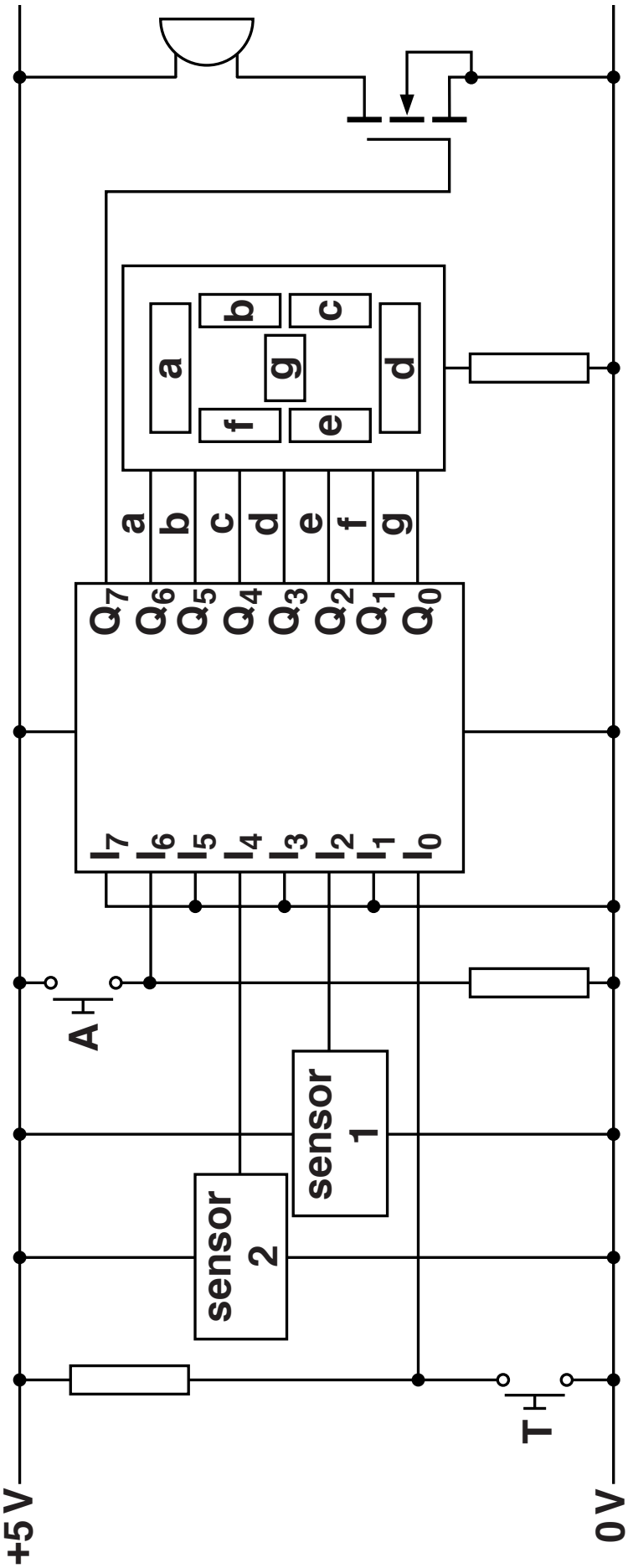

a
b
c
d
e
f
g
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
I7 I6 I5 I4 I3 I2 I1 I0
A
sensor 1
sensor 2
T
+5 V
0 V

FIG. 7.1

(b) The flowchart for the next part of the program is shown in Fig. 7.3 opposite.

Explain the effect that this part of the program has on the system of Fig. 7.1.

_____

_____

_____

_____

_____

_____

_____

_____

_____

_____ **[6]**

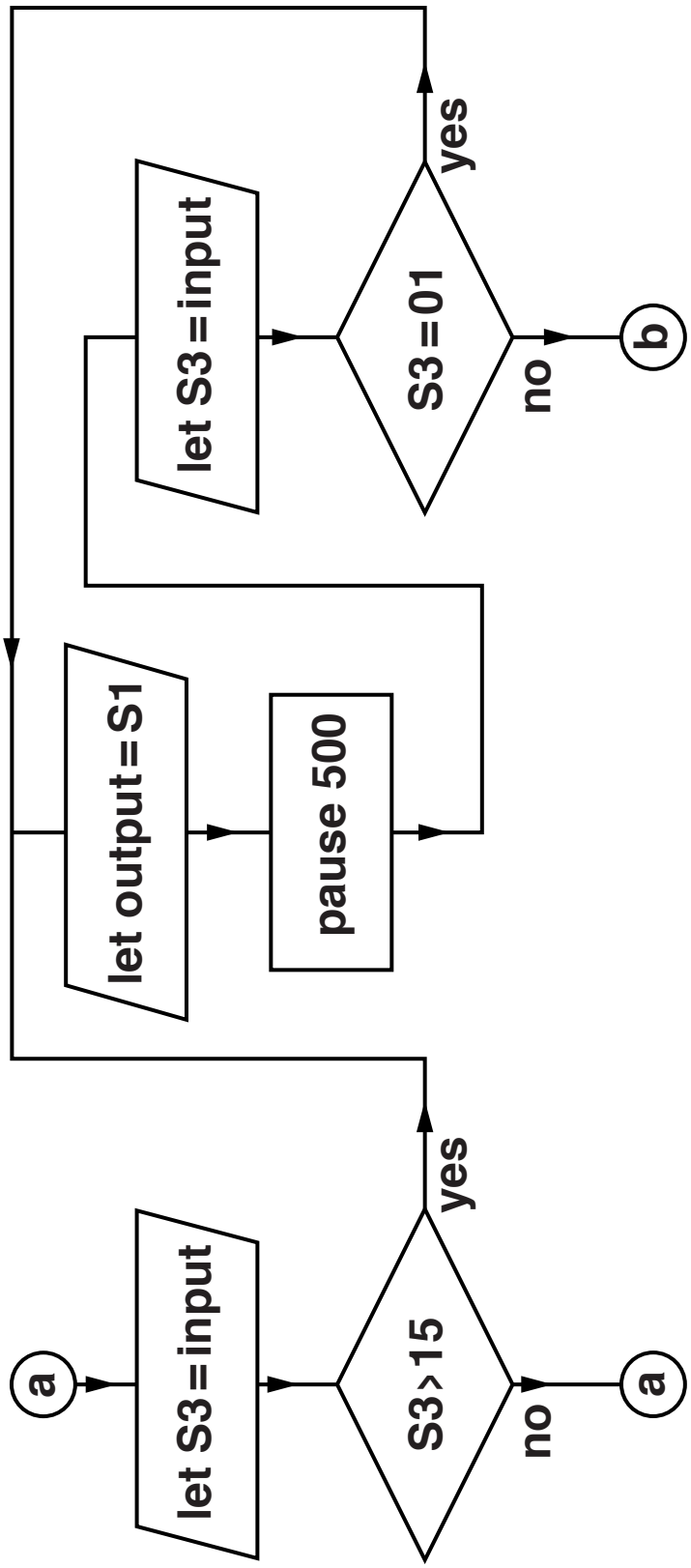

a
let S3 = input
S3 > 15
yes
no
a
let output = S1
pause 500
let S3 = input
S3 = 01
yes
no
b

FIG. 7.3

(c) The last part of the flowchart makes the system behave as follows:

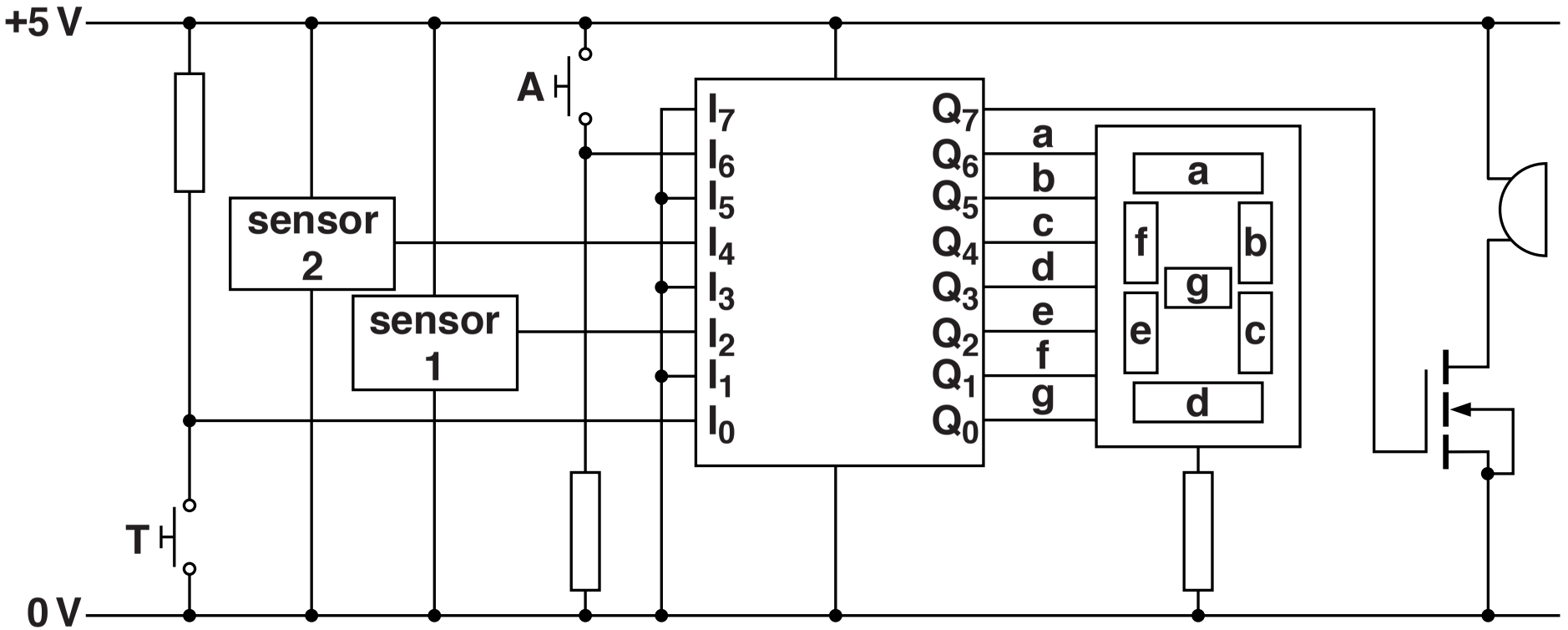
if there is a flood, continually display 'F' and turn on the buzzer

if switch T is closed, display '8' and turn on the buzzer for 500 ms, then return control to a.

Draw a suitable flowchart in the space below. A copy of Fig. 7.1 is provided opposite.

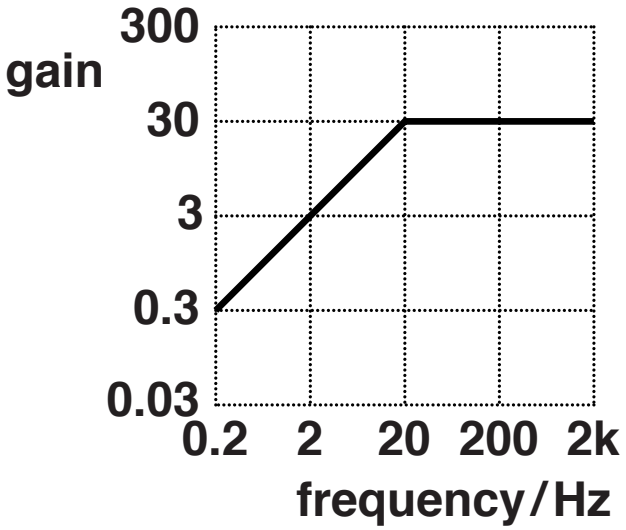
[4]

Copy of FIG. 7.1



8 Fig. 8.1 is the transfer characteristic of a tone control.

FIG. 8.1



(a) Explain why an audio system might contain this tone control.

_____

_____

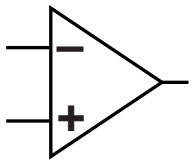
_____

_____ **[2]**

(b) Complete the circuit of Fig. 8.2 to show how the tone control can be assembled.

Show all component values and justify them with calculations.

FIG. 8.2



[5]

Quality of Written Communication [3]

END OF QUESTION PAPER