## GCE

## Electronics

Unit F614: Electronic Control Systems
Advanced GCE

Mark Scheme for June 2014

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This mark scheme is published as an aid to teachers and students, to indicate the requirements of the examination. It shows the basis on which marks were awarded by examiners. It does not indicate the details of the discussions which took place at an examiners' meeting before marking commenced.

All examiners are instructed that alternative correct answers and unexpected approaches in candidates' scripts must be given marks that fairly reflect the relevant knowledge and skills demonstrated.

Mark schemes should be read in conjunction with the published question papers and the report on the examination.

OCR will not enter into any discussion or correspondence in connection with this mark scheme.

## Quality of Written Communication

The candidate expresses complex ideas extremely clearly and fluently. Sentences and paragraphs follow on from one another smoothly and logically. Arguments are consistently relevant and well structured. There will be few, if any, errors of grammar, punctuation and spelling.

2 The candidate expresses straightforward ideas clearly, if not always fluently. Sentences and paragraphs may not always be well connected. Arguments may sometimes stray from the point or be weakly presented. There may be some errors of grammar, punctuation and spelling, but not such as to suggest a weakness in these areas.

The candidate expresses simple ideas clearly, but may be imprecise and awkward in dealing with complex or subtle concepts. Arguments may be of doubtful relevance or obscurely presented. Errors in grammar, punctuation and spelling may be noticeable and intrusive, suggesting weaknesses in these areas.
$0 \quad$ The language has no rewardable features.

| question | grade | expected answer | mark | additional guidance |
| :---: | :---: | :---: | :---: | :---: |
| 1a | E | 2.9 V | 1 | Allow 2.8 V - 2.9 V |
| 1bi | $\begin{aligned} & \hline \mathrm{D} \\ & \mathrm{C} \\ & \mathrm{C} \\ & \hline \end{aligned}$ | G from switch is -5 V <br> S is 0 V so $\mathrm{VGS}=-5 \mathrm{~V}$ <br> VGS < threshold <br> so MOSFET not conducting | $\begin{aligned} & 1 \\ & 1 \\ & 1 \end{aligned}$ | Resistance of MOSFET very high |
| 1bii | $\begin{aligned} & \hline \mathrm{E} \\ & \mathrm{D} \\ & \mathrm{D} \end{aligned}$ | line at 0 from $t=0$ to $t=4$ oscillation from 4 to end around 0 V same amplitude, shape and phase as input | $\begin{aligned} & 1 \\ & 1 \\ & 1 \end{aligned}$ |  |


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| 2a | $\begin{aligned} & \hline \mathrm{E} \\ & \mathrm{E} \\ & \mathrm{E} \\ & \mathrm{E} \\ & \mathrm{E} \\ & \hline \end{aligned}$ | six D-type flip-flops <br> $5 \times \mathrm{Q}$ to next D <br> clocks connected together and labelled <br> serial in correctly labelled at first D <br> outputs correctly labelled at all Qs | $\begin{aligned} & \hline 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & \hline \end{aligned}$ |  |
| 2 bi | $\begin{aligned} & \mathrm{C} \\ & \mathrm{D} \\ & \mathrm{~A} \end{aligned}$ | first two clock periods correct periods 3 \& 4 correct periods 5, 6 correct | $\begin{aligned} & 1 \\ & 1 \\ & 1 \end{aligned}$ | correct shape but changing on falling edge [2] |
| 2bii | A | 110001 no ecf | 1 | beware of reversing order of bits |
| 2biii | C | 49 (ecf from bii) | 1 |  |


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| :---: | :---: | :---: | :---: | :---: |
| 3a | $\begin{aligned} & \mathrm{A} \\ & \mathrm{E} \\ & \mathrm{~B} \\ & \mathrm{C} \\ & \mathrm{E} \end{aligned}$ | go: MOVI Sn, 04 <br>  IN $\mathrm{Sm}, \mathrm{I}$ <br>  AND $\mathrm{Sn}, \mathrm{Sm}$ <br>  JZ go <br>  RET | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | $n \neq m n \& m \leq 7$ <br> OR AND Sm, Sn <br> Lose 1 mark if SUB $\mathrm{Sm}, \mathrm{Sn}$ JNZ go (does not work if $X$ pressed or other I float high) |
| 3b | $\begin{aligned} & \text { C } \\ & \text { B } \\ & \text { B } \end{aligned}$ | $\begin{aligned} & \hline 44 \\ & 4 \mathrm{C} \\ & 55 \\ & 5 \mathrm{D} \\ & 77 \\ & \text { first one correct } \\ & \text { next two correct } \\ & \text { last two correct } \\ & \hline \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \\ & 1 \end{aligned}$ |  |
| 3c | D C A <br> D <br> B <br> E | Max 7 of: <br> Initialise pointer to start of look-up table <br> output number from table <br> move pointer to next item in table <br> check to see if at end of table <br> if so reset to start of table <br> Mask for X <br> check to see if switch is pressed <br> if not go back and output next number from table <br> if pressed return to main program | 7 | Make dice show 1 <br> Allow loop 6 times owtte |


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| :---: | :---: | :---: | :---: | :---: |
| 3d | D | make Q7 high | 1 | $0<j \leq 7,0<k \leq 7, j \neq k$ |
|  | B | without changing Q0-Q6 | 1 | beep: MOVI Sk, 80 |
|  | C | inititialise counter with C8 (hex for 200) | 1 |  |
|  | C | time delay | 1 | EOR S0,Sk |
|  | A | make Q7 low without changing Q0-Q6 | 1 | OUT Q,S0 |
|  | E | return | 1 | MOVI Sj, C8 |
|  |  |  |  | lbl: RCALL wait1ms <br> DEC Sj <br> JNZ lbl |
|  |  |  |  | $\begin{array}{ll} \text { EOR } & \text { S0,Sk } \\ \text { OUT } & \text { Q,S0 } \end{array}$ |
|  |  |  |  | RET |


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| 4a | $\begin{aligned} & \mathrm{E} \\ & \mathrm{E} \end{aligned}$ | diodes used to produce rectifier with correct polarity | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ |  |
| 4b | CD | Max 2 of: <br> unstabilised has (a large) ripple (wtte) <br> unstabilised output voltage depends on ac input (wtte) <br> regulated output has no/very little ripple (wtte) regulated output fixed/not dependent on input (wtte) regulator keeps the voltage at a constant voltage (wtte) | 2 |  |
| 4c | $\begin{aligned} & \hline \mathrm{C} \\ & \mathrm{C} \\ & \mathrm{~A} \\ & \mathrm{~A} \end{aligned}$ | correct reference with zener and resistor connected to op-amp input MOSFET used correctly at output negative feedback from regulated output | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ |  |




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| :---: | :---: | :---: | :---: | :---: |
| 6a | DDEE | Max 4 of: <br> - subroutines can be re-used <br> - subroutines can be tested separately <br> - programs easier to read <br> - programs easier to write due to structure <br> - saves memory because subroutine only needs to be stored once | 4 | 1 mark for state, 1 mark for explain |
| 6b | $\begin{aligned} & \mathrm{C} \\ & \mathrm{C} \\ & \mathrm{~A} \end{aligned}$ | value retrieved from stack and stored in program counter to instruction after RCALL stack pointer changed by 1 | $\begin{aligned} & 1 \\ & 1 \\ & 1 \end{aligned}$ |  |
| 6c | $\begin{aligned} & \mathrm{A}^{*} \\ & \mathrm{~A}^{*} \\ & \mathrm{~A}^{*} \\ & \mathrm{~A}^{*} \\ & \mathrm{~A}^{*} \end{aligned}$ | instructions unchanged program counter $=2 \mathrm{E}$ <br> stack pointer changed by 1 (56 or 58) <br> all but one data value unchanged <br> one data value now 2C (address 56, 57 or 58) | $\begin{aligned} & \hline 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & \hline \end{aligned}$ | Allow 2D |


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| 7a | $\begin{aligned} & \mathrm{E} \\ & \mathrm{E} \\ & \mathrm{E} \end{aligned}$ | $\begin{aligned} & \text { input connected to } V_{G} \\ & \text { output connected to } V_{D} \\ & \text { each input connected through a capacitor } \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \\ & 1 \end{aligned}$ |  |
| 7bi | $\begin{aligned} & \hline \mathrm{A} \\ & \mathrm{~B} \\ & \mathrm{~A} \end{aligned}$ | from graph $\mathrm{g}_{\mathrm{m}}=0.05 \mathrm{~S}$ $\begin{aligned} & \mathrm{R}=200 \Omega \\ & \text { gain }=-0.05 \times 200=-10\left(\text { ecf } g_{m}\right) \\ & \hline \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \\ & 1 \end{aligned}$ | transconductance calculated $200 \Omega$ used <br> gain -ve |
| 7bii | $\begin{aligned} & \mathrm{A}^{*} \\ & \mathrm{~A}^{*} \\ & \mathrm{~A}^{*} \\ & \mathrm{~A}^{*} \\ & \mathrm{~A}^{*} \\ & \mathrm{~A}^{*} \end{aligned}$ | $\begin{array}{\|l\|} \hline \mathrm{V} \text { across } 200 \Omega: 18-10=8 \mathrm{~V} \\ \mathrm{I}=8 / 200=0.04 \mathrm{~A} \\ \text { from graph } \mathrm{V}_{\mathrm{G}}=2.3 \mathrm{~V} \\ \mathrm{I} \text { in } 470 \mathrm{k} \Omega: 2.3 / 470000=4.89 \mu \mathrm{~A} \\ \mathrm{~V} \text { across } \mathrm{R}: 10-2.3=7.7 \mathrm{~V} \text { (ecf from } 8 \mathrm{bii}) \\ \mathrm{R}=7.7 / 4.89 \times 10^{-6}=1600 \mathrm{k} \Omega \\ \hline \end{array}$ | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ |  |
| 7c | $\begin{aligned} & \text { A* } \\ & \text { A* } \end{aligned}$ | MOSFETs have different characteristics Affects bias design not so sensitive to different MOSFETs | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ |  |


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| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 8ai | $E$$E$$E$ |  |  |  | 111 | 1 mark for each correct row |
|  |  | Q | U | L |  |  |
|  |  | 0 | open | closed |  |  |
|  |  | 1 | closed | open |  |  |
|  |  | High impedance | open | open |  |  |
| 8aii | $\begin{aligned} & \hline D \\ & D \\ & D \end{aligned}$ | logic to turn off both analogue switches with E logic turns off both analogue switches when E high logic turns reproduces A at Q (for one or more states of E) |  |  | $\begin{aligned} & 1 \\ & 1 \\ & 1 \end{aligned}$ |  |
|  |  |  |  |  |  |  |
| 8b | $\begin{aligned} & \mathrm{D} \\ & \mathrm{E} \end{aligned}$ | to disconnect the so that more than bus | from th ry can | ed to the same | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ |  |
| 8c | $\begin{aligned} & \hline \mathrm{E} \\ & \mathrm{E} \\ & \mathrm{E} \\ & \mathrm{D} \\ & \mathrm{D} \\ & \mathrm{~B} \end{aligned}$ | tristates between 2Qs to each Data 2Ds to each data Read operates tris write operates clo A0 routes read and | Q <br> correc |  | $\begin{aligned} & \hline 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ |  |


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| :--- | :---: | :--- | :---: | :---: |
| 8 d | E | information lost when power is turned off | 1 |  |

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