GCE

## Electronics

## Mark Scheme for June 2010

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This mark scheme is published as an aid to teachers and students, to indicate the requirements of the examination. It shows the basis on which marks were awarded by Examiners. It does not indicate the details of the discussions which took place at an Examiners' meeting before marking commenced.

All Examiners are instructed that alternative correct answers and unexpected approaches in candidates' scripts must be given marks that fairly reflect the relevant knowledge and skills demonstrated.

Mark schemes should be read in conjunction with the published question papers and the Report on the Examination.

OCR will not enter into any discussion or correspondence in connection with this mark scheme.
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## General advice to Assistant Examiners on the procedure to be used

## YOU WILL BE REQUIRED TO MARK PRACTICE AND STANDARDISATION SCRIPTS BEFORE STARTING TO MARK LIVE SCRIPTS.

1 The schedule of dates for the marking of this paper is very important. It is vital that you meet these requirements. If you experience problems then you must contact your Team Leader (Supervisor) without delay.

2 An element of professional judgement is required in the marking of any written paper. Candidates often do not use the exact words which appear in the detailed sheets which follow. If you are in doubt about the validity of any answer then consult your Team Leader (Supervisor) by phone, the messaging system within scoris, or e-mail.

3 Correct answers to calculations always gain full credit, even if no working is shown (The "Show your working" instruction is to help candidates, who may then gain credit even if their final answer is not correct.)

4 Some questions may have a 'Level of Response' mark scheme. Any details about these will be in the Additional Guidance.

5 Follow the current guidance on crossed-out work.
6 In addition to the award of 0 marks there is a NR (No Response) option in scoris.

## Award 0 marks

- if there is any attempt that earns no credit (including copying out the question or some crossed out working)


## Award NR (No Response)

- if there is nothing written at all in the answer space

OR

- if there is any comment which does not in any way relate to the question being asked (eg 'can't do', 'don't know') OR
- if there is any sort of mark which is not an attempt at the question (eg a dash, a question mark)

7 The Abbreviations, annotations and conventions used in the detailed Mark Scheme are:

## [QM to insert]

8 The Comments box will be use by your PE to explain their marking of the practice scripts. Please refer to these comments when checking your practice scripts.

Any questions or comments you have for your Team Leader should be communicated by phone, via the scoris messaging system, or e-mail.

## 9 Annotations in scoris

The following annotations are available:
[QM to amend/add others]
$\checkmark \quad=$ correct response
x = incorrect response

Highlighting is also available to highlight any particular points on the script.
[The following questions should be annotated with ticks to show where marks have been awarded in the body of the text: (QM to add)]

10 Please send a brief report on the performance of candidates to your Team Leader (Supervisor) by the end of the marking period. The Assistant Examiner's Report Form (AERF) can be found on the RM Cambridge Assessment Support Portal.

Your report should contain notes on particular strength displayed as well as common errors or weaknesses. Constructive criticism of the question paper/mark scheme is also appreciated.

| Question | Grade | Expected answer | Mark | Additional guidance |
| :---: | :---: | :---: | :---: | :---: |
| 1 (a) | $\begin{aligned} & \mathrm{B} \\ & \mathrm{C} \end{aligned}$ | processes / converts voltage / signal (at input) into a binary word / byte / bits / 1s and 0s / highs and lows/(hexadecimal) code | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | accept analogue signal look for more than one bit in binary output |
| 1 (b) (i) | $\begin{aligned} & \mathrm{E} \\ & \mathrm{D} \end{aligned}$ | EITHER <br> faster response because program goes in steps / limited by clock speed OR cheaper to make a circuit because no need for host computer <br> OR <br> limited ability to deal with analogue signals because only processes binary words <br> OR <br> easier to set up <br> because no need write programs / use a computer <br> OR <br> easier to fault-find <br> than finding an error in the program <br> OR <br> can process wider range of voltages because microcontroller run off 5 V and 0 V | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | look for advantage [1] look for a reason [1] <br> accept wtte for reasons |


| 1 (b) (ii) | $\begin{aligned} & \mathrm{E} \\ & \mathrm{E} \end{aligned}$ | any two of the following: <br> - cheaper components <br> - easy to design / make circuit <br> - components reusable <br> - circuit behaviour / program easily changed <br> - no need to rewire circuit when changed <br> - only one chip / fewer components <br> - smaller circuit (board) <br> - one chip can do many different things <br> - easier to replicate the circuit <br> - quicker to build <br> - check the design with a simulator | 2 | each point for [1] |
| :---: | :---: | :---: | :---: | :---: |
| 1 (c) | B C | $\begin{aligned} & \text { just R } \\ & B \text { and } G \end{aligned}$ | 1 1 |  |
| 1 (d) | $\begin{aligned} & \mathrm{E} \\ & \mathrm{E} \\ & \mathrm{C} \end{aligned}$ | if S0 above 4A; then OF at output port; D8 at output port if S0 between 4A and 08 | 1 1 1 | accept reference to input signal instead of S0 accept correct binary instead of hexadecimal accept reference to LEDs instead of port, including ecf from (c) <br> accept D8 at output if S0 above 08 |


| 1 (e) | E D C B A A | process boxes to load S1 and S2 process box to load S3 with 60 output box for S3 input box to any register other than S1, S2 appropriate decision box for that register appropriate loop back from yes or no before going to a | 1 1 1 1 1 1 | three process boxes in any order any register other than S1 or S2 ecf:accept "let output =60" for [1] <br> can test for $=0$ or $>0$ or $=20$ (in hex) <br> accept $=32$ (in decimal) <br> allow ecf from incorrect input for pin I5 <br> accept loop back to any part of flowchart before input box <br> shape of box must be correct to earn each mark <br> box must be in appropriate place in flowchart to earn each mark <br> accept pins instead of input or output ignore $\$$ in front of hex words |
| :---: | :---: | :---: | :---: | :---: |
| 2 (a) | C E A | any three of the following, [1] each: <br> - gain of op-amp when no feedback <br> - difference in voltage of inputs <br> - multiplied / amplified by 200000 <br> - if not saturated / limited by power supply values | 3 | not just voltage at input ignore $V_{\text {out }}=A\left(V_{+}-V_{-}\right)$ accept any mention of saturation for [1] |


| 2 (b) | $\begin{aligned} & \hline \mathrm{D} \\ & \mathrm{C} \end{aligned}$ | EITHER <br> negative feedback from output keeps inputs at same voltage OR use of $V_{\text {out }}=A\left(V_{+}-V_{-}\right)$ to prove that $G=200000 / 200001$ or $Y+Y / A$ | $1$ | accept output to inverting input as -ve feedback <br> accept use of non-inverting amplifier rule [1] with $R_{\mathrm{f}}=0$ giving $G=+1$ [1] |
| :---: | :---: | :---: | :---: | :---: |
| 2 (c) (i) | $\mathrm{E}$ E | $\begin{aligned} & I=\frac{V}{R}=\frac{5}{27 \times 10^{3}} \\ & I=1.9 \times 10^{-4} \mathrm{~A} / 0.19 \mathrm{~mA} \end{aligned}$ | 1 | look for correct transposition and substitution, including correct powers of 10 (not k) accept $0.2 \mathrm{~mA} / 0.18 \mathrm{~mA}$ look for evidence of calculation performed |
| 2 (c) (ii) | $\begin{aligned} & \hline \mathrm{B} \\ & \mathrm{E} \end{aligned}$ | no current at input of op-amp / high input impedance $1.9 \times 10^{-4} \times 5=9.5 \times 10^{-4} \mathrm{~W} \text { or } 0.95 \mathrm{~mW}$ | 1 1 | accept $1 \times 10^{-3} \mathrm{~W}$ or 1 mW allow ecf from incorrect (c) (ii) |
| 2 (c) (iii) | $\begin{aligned} & \mathrm{E} \\ & \mathrm{D} \\ & \mathrm{C} \end{aligned}$ | $\begin{array}{\|l\|} \hline V=5 \mathrm{~V} \\ l=5 / 40=0.125 \mathrm{~A} \\ P=5 \times 0.125=0.625 \mathrm{~W} \end{array}$ | 1 1 1 | accept 0.6 W <br> allow ecf from incorrect I <br> allow ecf from incorrect $V$ <br> e.g. 13 V gives 0.33 A for [1] and 4.2 W for [1] |
| 3 (a) | A | frequency steadier with time (wtte) | 1 | accept crystals have smaller tolerances / are more accurate than resistors / capacitors |
| 3 (b) | $\begin{aligned} & \mathrm{E} \\ & \mathrm{C} \end{aligned}$ | counter chain by connecting an output from first two counters to clock input of next counter output from ninth output of counter chain | 1 |  |


| 3 (c) | $\begin{aligned} & \mathrm{E} \\ & \mathrm{D} \\ & \mathrm{~B} \\ & \mathrm{~A} \\ & \mathrm{E} \end{aligned}$ | Q-bar to D of each flip-flop Q-bar to clock of next flip-flop outputs in correct sequence NOT gate before first clock R connected to each other (and 0 V ) | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ |  |
| :---: | :---: | :---: | :---: | :---: |
| 3 (d) | E D E D | ```seven-segment LED to display numbers (0 to 9) decoder / driver to convert 4-bit (BCD) word to 7-bit word (for LEDs)``` | 1 1 1 1 | ```accept LED display / LCD accept logic system accept to provide current for LEDs if driver [1]``` |
| 4 (a) | E D C | microphone first, loudspeaker last voltage amplifier somewhere before power amplifier volume control somewhere before power amplifier | 1 1 1 |  |


| 4 (b) | $\begin{aligned} & \hline \mathrm{B} \\ & \mathrm{D} \\ & \mathrm{C} \\ & \mathrm{~B} \\ & \mathrm{E} \\ & \mathrm{E} \end{aligned}$ | correct circuit input through $47 \mathrm{k} \Omega$ resistor $940 \mathrm{k} \Omega$ feedback resistor 34 nF capacitor (accept 33 nF ) use of break frequency formula to find $C$ use of inverting amplifier gain formula to find $R_{f}$ | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | accept missing 0 V label <br> ecf: $20 \times$ incorrect input resistor for [1] allow ecf in calculating $C$ for incorrect value of input resistor $R_{\text {in }} C=1.6 \mathrm{~ms} \text { for }[1]$ |
| :---: | :---: | :---: | :---: | :---: |
| 4 (c) | $\begin{aligned} & \mathrm{E} \\ & \mathrm{~A} \\ & \mathrm{C} \\ & \mathrm{E} \end{aligned}$ | input impedance $4.7 \mathrm{k} \Omega$ (either type of amp) non-inverting amplifier circuit resistors to give gain of 20 (either type of amp) use of gain formula for type of amplifier attempted | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | 0 V label must be present ignore range of resistor values |


| 4 (d) (i) | $\begin{aligned} & \hline \mathrm{E} \\ & \mathrm{E} \\ & \mathrm{E} \end{aligned}$ | correct symbol one track end to 0 V other track end to input, wiper to output |  |  |  |  | 1 | ignore any resistor in series with input or output |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 5 (a) (i) | E | hold D low/ logic 0 / 0 V pulse E / hold E high |  |  |  |  | 1 1 |  |
| 5 (a) (ii) | $\begin{aligned} & \mathrm{E} \\ & \mathrm{~B} \end{aligned}$ | Q goes high as E rises and stays there until E rises again $Q$ follows $D$ during second high pulse of $E$ and stays low |  |  |  |  | 1 1 | accept Q simultaneously high and low before E rises. |
| 5 (b) | $\begin{aligned} & \hline \text { D } \\ & \text { B } \\ & \text { A } \end{aligned}$ | each correct column [1] with ecf |  |  |  |  | 3 | ecf: $\mathrm{R}=\overline{\mathrm{F} . \mathrm{E}}=\overline{\mathrm{F}}+\overline{\mathrm{E}}$ |
|  |  | D | E | F | S | R |  |  |
|  |  | 0 | 0 | 1 | 1 | 1 |  |  |
|  |  | 0 | 1 | 1 | 1 | 0 |  |  |
|  |  | 1 | 0 | 0 | 1 | 1 |  |  |
|  |  | 1 | 1 | 0 | 0 | 1 |  |  |


| 5 (c) | $\begin{aligned} & \hline \text { C } \\ & \text { A } \\ & \text { B } \end{aligned}$ | Gate output only low when both inputs high So $Q$ and $R$ high means $P$ is low - and so $Q$ is high If $Q$ is low, $P$ is high with $S-$ so $Q$ is low | $\begin{aligned} & 1 \\ & 1 \\ & 1 \end{aligned}$ | description of NAND gate behaviour for [1] why $\mathrm{Q}=1$ is stable for [1] <br> why $\mathrm{Q}=0$ is stable for [1] |
| :---: | :---: | :---: | :---: | :---: |
| 5 (d) | $\begin{aligned} & \hline \text { C } \\ & \text { B } \\ & \text { A } \\ & \text { A } \\ & \text { A } \end{aligned}$ | Any of the following for [1] each: <br> D flip-flop description: <br> - D copied to Q when CK rises <br> - Q doesn't change otherwise <br> Circuit explanation: <br> - when $E_{n}$ is high $D_{n}$ copied to $Q_{n}$ (transparent) <br> - when $E_{n}$ is low $Q_{n}$ does not change (frozen) <br> - when CK low $D_{1}$ copied to $Q_{1}$ but no change at $Q_{2}$ <br> - as CK goes high $Q_{1}$ copied to $Q_{2}$ <br> - when CK high no change at $Q_{1}$ so no change at $Q_{2}$ <br> - as CK goes low, $\mathrm{D}_{2}$ no longer copied to $\mathrm{Q}_{2}$ | 6 | for each correct and precise statement about a latch or D flip-flop, award [1] |
| 6 (a) | $\begin{aligned} & \mathrm{E} \\ & \mathrm{E} \\ & \mathrm{C} \end{aligned}$ | $\begin{aligned} & T=0.5 R C=0.5 \times 33 \times 10^{3} \times 47 \times 10^{-6} \\ & =0.78 \mathrm{~s} \\ & \text { ecf: } f=1 / T=1.3 \mathrm{~Hz} \end{aligned}$ | 1 1 1 | ecf: $T=R C$ gives 1.6 s [1] and 0.64 Hz [1] ecf: $T=0.7 R C$ gives 1.1 s [1] for 0.92 Hz [1] ignore use of break frequency formula. |
| 6 (b) | $\begin{aligned} & \hline \mathrm{E} \\ & \mathrm{E} \\ & \mathrm{D} \end{aligned}$ | AND gate controlling R A and C to inputs | 1 1 1 |  |
| 6 (c) | $\begin{aligned} & \mathrm{E} \\ & \mathrm{~A} \end{aligned}$ | $V_{1}, V_{2}=+5 \mathrm{~V}$ and use of summing amp formula $V=-4.5 \mathrm{~V}$ | 1 1 | ecf: $V_{1}, V_{2}=+1 \mathrm{~V}$ gives $V=-0.9 \mathrm{~V}$ for [1] must have correct sign to earn the mark |


| 6 (d) | $\begin{aligned} & \hline \mathrm{B} \\ & \mathrm{E} \\ & \mathrm{D} \\ & \mathrm{E} \end{aligned}$ | correct circuit (including 0 V to + input) resistors between $1 \mathrm{k} \Omega$ and $10 \mathrm{M} \Omega$ feedback resistor 0.4 times input resistor use of $G=-R_{f} / R_{\text {in }}$ | 1 1 1 1 |  |
| :---: | :---: | :---: | :---: | :---: |
| 6 (e) | D | maximum when $\mathrm{CBA}=100$, giving -6.0 V at S so T at +2.4 V | 1 | ecf incorrect S: CBA $=111$ gives $\mathrm{T}=4.2 \mathrm{~V}$ for [1] ecf incorrect S: CBA $=101$ gives $\mathrm{T}=3.0 \mathrm{~V}$ for [1] $\mathrm{S}=-4.5 \mathrm{~V}$ gives $\mathrm{T}=1.8 \mathrm{~V}$ for [1] |

## Quality of Written Communication

3 The candidate expresses complex ideas extremely clearly and fluently. Sentences and paragraphs follow on from one another smoothly and logically. Arguments are consistently relevant and well structured. There will be few, if any, errors of grammar, punctuation and spelling.

2 The candidate expresses straightforward ideas clearly, if not always fluently. Sentences and paragraphs may not always be well connected. Arguments may sometimes stray from the point or be weakly presented. There may be some errors of grammar, punctuation and spelling, but not such as to suggest a weakness in these areas.

1 The candidate expresses simple ideas clearly, but may be imprecise and awkward in dealing with complex or subtle concepts. Arguments may be of doubtful relevance or obscurely presented. Errors in grammar, punctuation and spelling may be noticeable and intrusive, suggesting weaknesses in these areas.

0 The language has no rewardable features.

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