OCR
RECOGNISING ACHIEVEMENT

GCE

Electronics

Advanced GCE **A2 7826**

Advanced Subsidiary GCE **AS 3826**

Mark Schemes for the Units

June 2009

3826/7826/MS/R/09

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MARK SCHEMES FOR THE UNITS

2526 Foundations of Electronics

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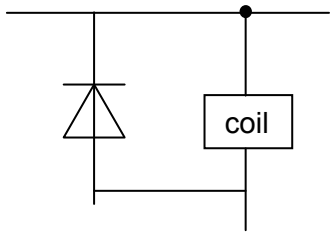
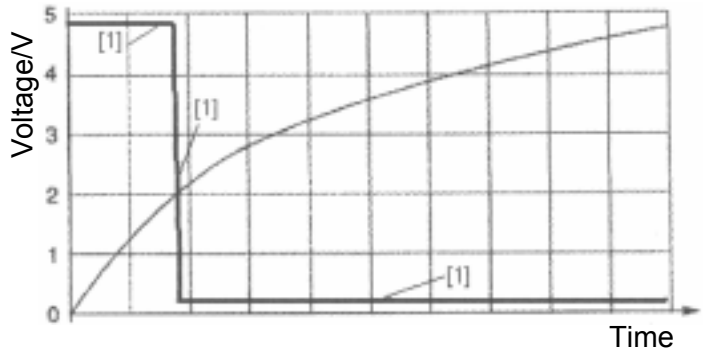
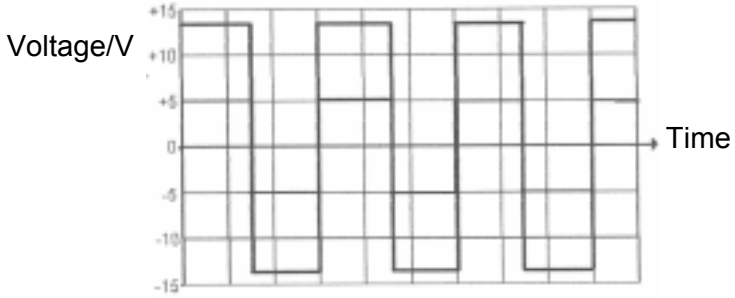
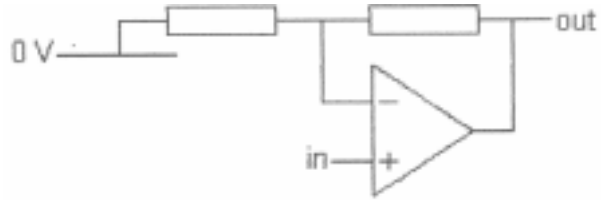
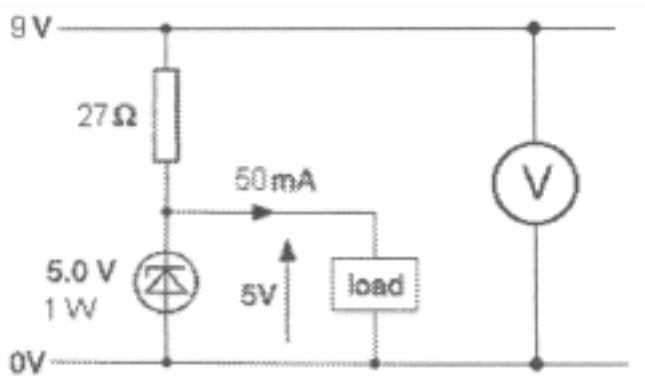
<tr><th colspan="2">Question</th><th>Grade</th><th>Expected answer</th><th>Mark</th></tr>
<tr><td>1</td><td>(a)</td><td>de</td><td>1 is +5V/near top supply rail/above 2.5 V or 3.0 V</td><td>[1]</td></tr>
<tr><td></td><td></td><td>de</td><td>0 is 0V/near bottom supply rail/below 2.5 V or 2.0 V.
ACCEPT 1 is high and 0 is low (voltage) for [1]</td><td>[1]</td></tr>
<tr><td></td><td>(b)</td><td>de</td><td>First line 1</td><td>[1]</td></tr>
<tr><td></td><td></td><td>de</td><td>ecf: last three lines opposite to first
<table><tr><td>B</td><td>A</td><td>Q</td></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table></td><td>[1]</td></tr>
<tr><td></td><td>(c)</td><td>de</td><td>[1] per correct column, ecf from previous columns.
<table><tr><td>C</td><td>D</td><td>E</td><td>F</td><td>G</td><td>H</td><td>J</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr></table></td><td>[5]</td></tr>
<tr><td></td><td></td><td>de</td><td></td><td></td></tr>
<tr><td></td><td></td><td>de</td><td></td><td></td></tr>
<tr><td></td><td></td><td>bcd</td><td></td><td></td></tr>
<tr><td></td><td></td><td>bcd</td><td></td><td></td></tr>
<tr><td></td><td>(d)</td><td>de</td><td>Output high/5V/1 when inputs are different (wtte)</td><td>[1]</td></tr>
<tr><td></td><td></td><td>de</td><td>Output low/0V/0 when inputs are the same (wtte)</td><td>[1]</td></tr>
</table>

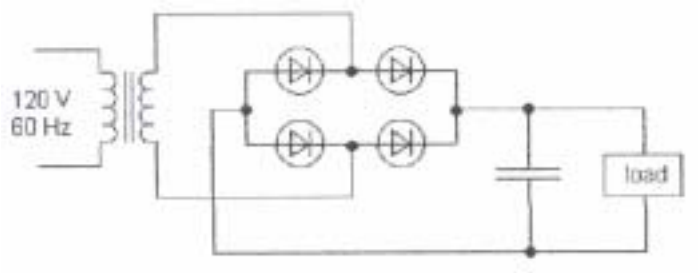
Question	Grade	Expected answer	Mark
2 (a) (i)	de	LDR indicated with an X nearby or through it.	[1]
(ii)	de	LDR/light dependent resistor.	[1]
(b)	bcd	Diode in parallel with coil.	[1]
	ab	Reverse bias.	[1]
			
(c)	de	48 kΩ	[1]
	bcd	Rules being used: • V proportional to R • $I = V/R$ followed by $R = V/I$ • $V = V_s \frac{R_1}{R_1 + R_2}$	[1]
	ab	Use of rules to justify choice.	[1]
(d)	de	Up to five of the following, [1] each:	[5]
	de	• LDR resistance high	
	bcd	• so A below 3V	
	bcd	• non-inverting input lower (than inverting input)	
	ab	• so B saturates low (at -13V)	
		• sinking current from coil (wtte)	
		• closing the switch/energising the relay	
		• allowing current in/voltage across the motor.	

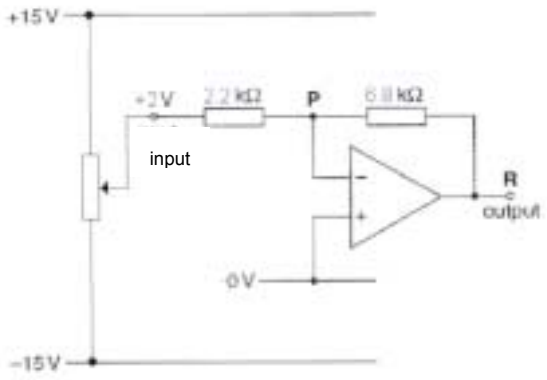
Question	Grade	Expected answer	Mark
3 (a)	de	starts high, then goes low.	[1]
	de	drops/changes sharply at 2V	[1]
	bcd	high at 4.8V, low at 0.2 V (by eye).	[1]
			
(b) (i)	de	Show: $\tau = RC$	[1]
	bcd	$R = 22 \times 10^3 \Omega$, $C = 56 \times 10^{-9}$F (units conversion)	[1]
	bcd	$\tau = \underline{1.2} \times 10^{-3}$ s	[1]
(ii)	ab	$t = \tau \ln (V_0/V)$ (eor)	[1]
	ab	$t = 1.2 \times 10^{-3} \times \ln (5/3) = 6.1 \times 10^{-4}$s	[1]
(c) (i)	de	LED off	[1]
	bcd	because Y is low so R is high forcing Q low	[1]
(ii)	de	pressing switch pulls CK high	[1]
	bcd	copying high at D to Q	[1]
	bcd	so LED glows	[1]
	ab	Q remains high when switch released.	[1]

Question	Grade	Expected answer	Mark
4 (a) (i)	de	input and output signals have the same sign (wtte)	[1]
(ii)	bcd	data from graph e.g. 13V out for +4V in	[1]
	bcd	use of $G = \frac{V_{out}}{V_{in}} = 3.3$	[1]
(b)	de	correct shape and phase	[1]
	bcd	saturates at +13V and -13V (by eye)	[1]
			
(c)	de	negative feedback with resistor	[1]
	de	non-inverting input of op-amp to input	[1]
	bcd	inverting input to 0V via resistor	[1]
	bcd	in and out labelled correctly	[1]
	ab	$R_f = 2 \times R_d$	[1]
	ab	both resistors between 100Ω and 10MΩ.	[1]
			

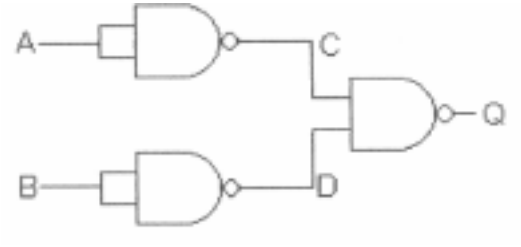
Question	Grade	Expected answer	Mark
5 (a)	de	correct symbol	[1]
	de	correct connection	[1]
			
(b) (i)	de	evidence of rule	[1]
	de	substitution	[1]
	bcd	evaluation	[1]
		$R = \frac{V}{I} = \frac{5}{50\text{x}10^{-3}} = 100\ \Omega$	
(ii)	de	$P = VI$ (eor)	[1]
	de	$P = 5 \times 50 \times 10^{-3}$	[1]
	bcd	P = 0.25W or 250 mW.	[1]
(c) (i)	de	Show: $I = \frac{V}{R}$	[1]
	de	$V = 9 - 5 = 4$V	[1]
	bcd	$I = 4/27 = \underline{0.148}$ A	[1]

Question	Grade	Expected answer	Mark
(ii)	ab	ecf: 148 - 50 = 98 mA or 0.098 A ACCEPT 150 – 50 = 100 mA or 0.1 A	**[1]**
(iii)	bcd	Show: $P = VI$	**[1]**
	bcd	ecf: $P = 5.0 \times 98 \times 10^{-3} = 0.49$ mW	**[1]**
	ab	0.49 W < 1 W (owtte)	**[1]**
(d)	bcd	no current at low voltage	**[1]**
	bcd	current starts at breakdown voltage / 5 V (owtte)	**[1]**
	ab	rising rapidly as voltage rises further (above breakdown voltage).	**[1]**

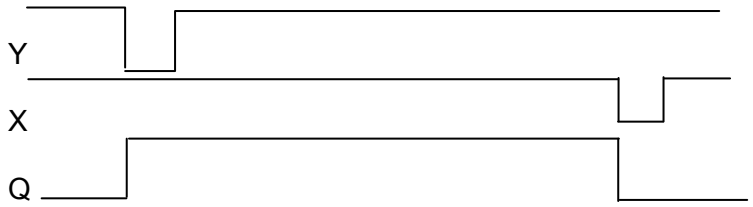
Question	Grade	Expected answer	Mark
6 (a)	de	correct diode bridge arrangement	[1]
	de	connected correctly to secondary	[1]
	bcd	capacitor correctly connected to bridge	[1]
	bcd	load in parallel with capacitor	[1]
	ab	mains supply to primary	[1]
	ab	recognisable symbols throughout.	[1]
			
(b)	de	peak output of secondary V_0 = 9V + 1.4V = 10.4V	[1]
	bcd	because current / charge passes through two diodes	[1]
	ab	ecf incorrect V_0: $V_{rms} = V_0/1.4 = 10.4/1.4 = 7.4V$	[1]
(c)	de	$T = \frac{1}{f}$ (eor)	[1]
	de	T = 1/60 = 0.017s	[1]
	bcd	ecf incorrect T: period of ripple = $0.017/2 = 8.3 \times 10^{-3}$s	[1]
(d)	de	$V_r = \frac{It}{C}$ (eor)	[1]
	bcd	$I = V/R$ = 9/33 = 0.27A	[1]
	ab	ecf: $V_r = 0.27 \times 8.3 \times 10^{-3}/2200 \times 10^{-6} = 1.0V$	[1]

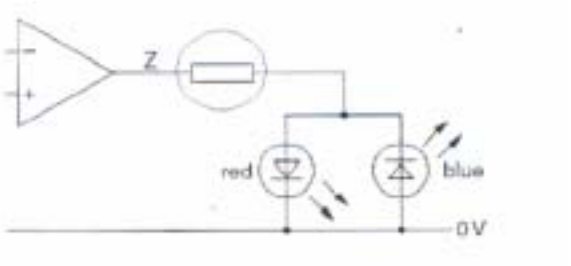
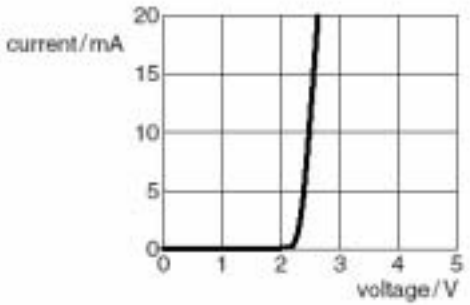
Question	Grade	Expected answer	Mark
7 (a)	de		[1]
(b)	de	0V	[1]
(c)	de	$G = -R_f/R_{in}$	[1]
	bcd	G = -6.8/2.2 = -3.1	[1]
	ab	ecf: output = +2 x -3.1 = -6.2V	[1]

Question	Grade	Expected answer	Mark
8 (a)	de	all four combinations of BA	[1]
	de	Q = 0 when BA = 11	[1]
	de	Q = 1 when BA ≠ 11	[1]
		B A Q: 0 0 1; 0 1 1; 1 0 1; 1 1 0	
(b) (i)	de	output low when both inputs low	[1]
	de	otherwise output high	[1]

Question	Grade	Expected answer	Mark
(ii)		circuit:	
	de	output from NAND gate	**[1]**
	de	whose inputs are fed from A and B via NAND inverters	**[1]**
			
		truth table:	
	bcd	all four combinations of inputs	**[1]**
	bcd	C = NOT A	**[1]**
	ab	D = NOT B	**[1]**
	ab	Q = C NAND D	**[1]**

A	B	C	D	Q
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

Question	Grade	Expected answer	Mark
(c) (i)	bcd	Q high forces P low, allowing Q to remain high	[1]
	ab	Q low forces P high, allowing Q to remain low	[1]
(ii)	bcd	P goes high	[1]
	bcd	both P and Y go high (makes Q low)	[1]
(iii)	de	Q goes high on falling edge of Y	[1]
	de	Q remains high when Y goes high	[1]
	bcd	Q goes low and stays low on falling edge of X	[1]
			

Question	Grade	Expected answer	Mark
9 (a) (i)	de		[1]
(ii)	de	no current at low voltage	[1]
	bcd	until about 2V	[1]
	ab	rising rapidly as voltage goes above 2V	[1]
			
(b) (i)	de	13 – 3.2	[1]
	de	= 9.8V	[1]
(ii)	de	$R = V/I$ (eor)	[1]
	de	ecf: $R = 9.8/12 \times 10^{-3}$	[1]
	bcd	$R = 820\ \Omega$ ecf: 13 V gives 1083 Ω	[1]
(c)	de	closed switch pulls X to 0V	[1]
	de	X below Y (at +0.7V) / inverting below non-inverting input	[1]
	bcd	so op-amp saturates high (at +13V)	[1]
	ab	and blue LED is reverse biased/has no current	[1]

Quality of Written Communication

3 The candidate expresses complex ideas extremely clearly and fluently. Sentences and paragraphs follow on from one another smoothly and logically. Arguments are consistently relevant and well structured. There will be few, if any, errors of grammar, punctuation and spelling.

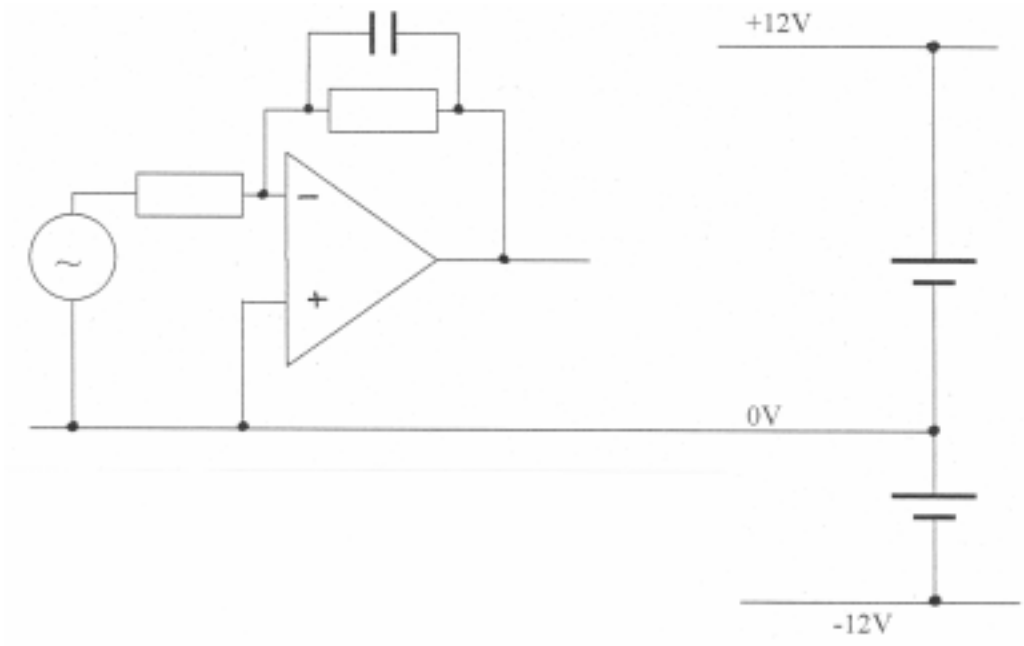
2 The candidate expresses straightforward ideas clearly, if not always fluently. Sentences and paragraphs may not always be well connected. Arguments may sometimes stray from the point or be weakly presented. There may be some errors of grammar, punctuation and spelling, but not such as to suggest a weakness in these areas.

1 The candidate expresses simple ideas clearly, but may be imprecise and awkward in dealing with complex or subtle concepts. Arguments may be of doubtful relevance or obscurely presented. Errors in grammar, punctuation and spelling may be noticeable and intrusive, suggesting weaknesses in these areas.

0 The language has no rewardable features.

2527 Signal Processing Circuits

Question	Expected Answer	Mark
1 (a)	Output = A Type of gate = AND	**[1]** **[1]**
1 (b)	Output = 1 (or logic 1) Type of gate = OR	**[1]** **[1]**
1 (c)	Output = 1 (or logic 1) Type of gate = NAND	**[1]** **[1]**
1 (d)	Output = NOT A Type of gate = NOR	**[1]** **[1]**
1 (e)	Output = NOT A Type of gate = EOR (accept XOR / EXOR)	**[1]** **[1]**
2 (a)	$Z = \overline{X}$	**[1]**
2 (b)	$P = \overline{X} . Y$	**[1]**
2 (c)	$Q = X + P$	**[1]**
2 (d)	$Q = X + \overline{X} . Y$	**[1]**

Question	Expected Answer	Mark
2 (e)		
(i)	Q = X + X . Y + Y . 1	**[1]**
(ii)	Q = X + Y (X + 1)	**[1]**
	= X + Y	**[1]**
(iii)	When X is logic one then Q = 1 Because the OR gate has a logic 1 input (or wtte)	**[1]**
	When X is logic. Zero then Q = Y Because the AND gate will output a 1 if Y is 1 and a 0 if Y is 0 (or wtte)	**[1]**
3 (a)		

Question	Expected Answer	Mark
3 (a) continued	±12V lines correctly shown	[1]
	OV line correctly shown	[1]
	Signal source correctly connected	[1]
	Non-inverting input connected to 0V line	[1]
	Correct inverting amplifier circuit	[1]
	Input resistor shown as 1.7 kΩ	[1]
	Gain formula shown as R_f/R_1	[1]
	Feedback resistor shown as 400 x 1.7 = 680 kΩ	[1]
	Capacitor correctly connected across feedback resistor	[1]
	Break frequency shown as ½ π RC	[1]
	Calculation of capacitance C = 1.56 x 10^{-9} F	[1]
3 (b)	Any constant gain breaking at 150 Hz	[1]
	Correct treble cut shaped graph	[1]
	Frequencies and gain values correctly marked	[1]
	Correct logarithmic roll off	[1]

Question	Expected Answer	Mark
4 (a)	(Inverting) Schmitt Trigger	[1]
4 (b)	Potentiometer correctly circled	[1]
4 (c)	R = V / I = (13 - 2) / 0.005 = 2200 Ω	[1] [1] [1]
(d) (i)	When V_{in} = 15V then $V_- > V_+$	[1]
	So op-amp is saturated negatively at -13V	
	LED G is in forward bias so is (fully) ON	[1]
	LED Y is in reverse bias so is OFF	[1]
(ii)	± (18 / 12 + 18) x 13	[1]
	= ± 7.8v	[1]
(iii)	LED Y stays OFF and LED G stays ON	[1]
	without any change in brightness	[1]
	until V_{in} reaches -7.8V	
	at which point positive feedback causes the output to flip saturation to	[1]
	+13V so LED Y comes (fully) ON and LED G goes OFF	
	No further change occurs to this state	

<table>
<tr><th>Question</th><th>Expected Answer</th><th>Mark</th></tr>
<tr><td>4 (d) (iv)</td><td>LED G stays OFF and LED Y stays ON

without any change in brightness

until V_{in} reaches +7.8V

at which point positive feedback causes the output to flip saturation to

-13V so LED G comes (fully) ON and LED Y goes OFF

No further change occurs to this state</td><td>[1]

[1]</td></tr>
<tr><td>5 (a)</td><td>
<table>
<tr><th>clock pulse</th><th>A</th><th>B</th><th>C</th><th>D</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>2</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>3</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
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<tr><td>5</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>6</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>7</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
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<tr><td>11</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>12</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>13</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
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<tr><td>17</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
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</td><td></td></tr>
</table>

Question	Expected Answer	Mark
5 (a) continued	Output A alternates 0/1	**[1]**
	Output B is half of A's frequency	**[1]**
	Output C is half of B's frequency until reset at 12	**[1]**
	Output D is half of Cs frequency Until reset at 12	**[1]**
	Thereafter new cycle begins with 13th pulse	**[1]**
5 (b) (i)	LED P lights up when A = 0 and B = 1	**[1]**
(ii)	LED Q lights up when B =: 1 and D = 1	**[1]**
5 (c) (i)	LED 1 lights up for 1 second	**[1]**
	then goes off for 3 seconds	**[1]**
	lights up for 1 second then goes off for 3 seconds repeatedly	**[1]**
(ii)	LED 2 lights up for 2 seconds	**[1]**
	then goes off for 10 seconds	**[1]**
	lights up for :2 seconds then goes off for 10 seconds repeatedly	

Question			Expected Answer			Mark
6	(a)	(i)	p.d. "lost" inside guitar pick-up	=	158 mV – 100 m V	
				=	58 mV	[1]
		(ii)	Current supplied by pick-up	=	100 m V / 4.7 kΩ	[1]
				=	21.3 X 10-6 A	[1]
		(iii)	Pick-up output resistance	=	58 x 10-3 / 21.3 X 10-6	[1]
				=	2726Ω	[1]
6	(b)	(i)	Peak current in loudspeaker	=	18V / 12 Ω	[1]
				=	1.5 A	[1]
		(ii)	Mean power to speaker	=	peak power / 2	[1]
				=	18x1.5/ 2	[1]
				=	13.5 W	[1]
6	(c)		Output voltage produced by amplifier resistance	=	18V + p.d. across output	
				=	18+1.5x4	[1]
				=	24 V	[1]
			Voltage gain of amplifier	=	24 / 100 X 10-3	
				=	240	[1]

7 (a) (i)

Key 1	Key 2	Key 3	Key 4	Key 5	Key 6	C	B	A
0	*0*	*0*	*0*	*0*	*0*	***0***	***0***	***0***
0	1	0	0	0	0	0	1	0
0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	1	0	0
0	0	0	0	1	0	1	0	1
0	0	0	0	0	1	1	1	0

Correct key press codes and correct corresponding binary codes **[1] [1] [1]**

(deduct one mark per error or omission)

(ii) Any OR gate used with inputs connected to any switch line

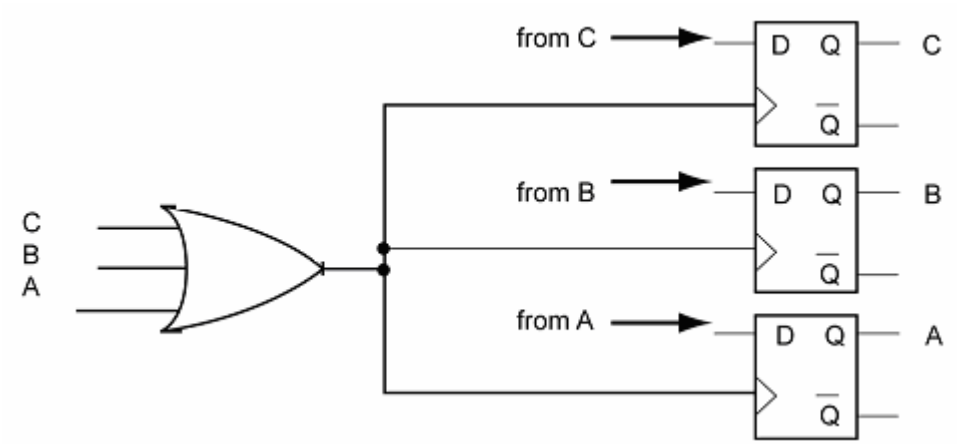
Three 3-input OR gates required for C, B and A **[1]**

Cs inputs connected to lines 4, 5 and 6 **[1]**

B's inputs connected to lines 2, 3 and 6 **[1]**

A's inputs connected to lines 1, 3 and 5 **[1]**

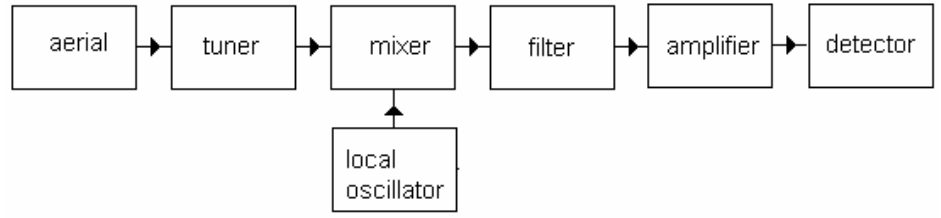
7 (b) (i)



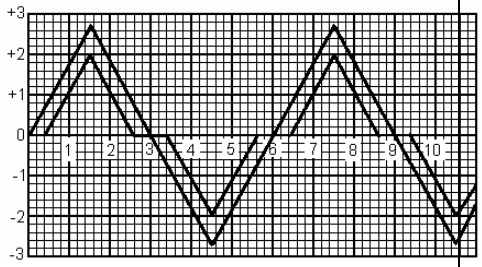
[1] **[1]** **[1]**

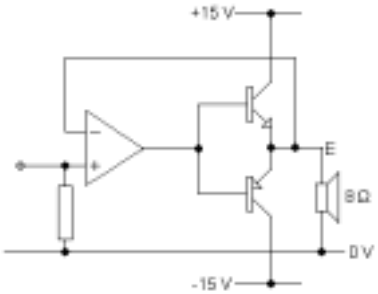
Question	Expected Answer	Mark
7 (b) (ii)	Keypad outputs CBA become the D inputs of the three D-types and the Q outputs become the stored values But the D-types must be clocked each time either A or B or C goes to logic 1 **[1]** (ignore the need for a short time delay between appearance of code CBA and the clocking of the D-types) **[1]**	

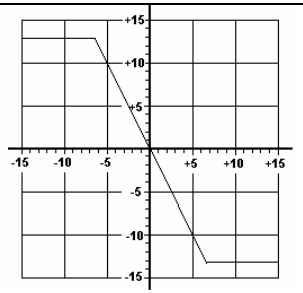
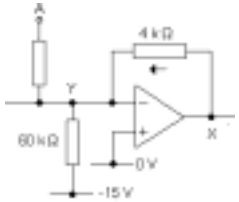
2529 Communications Circuits

Question	Grade	Expected answer	Mark
1 (a) (i)	DE	the amplitude of the carrier for AM (wtte) ACCEPT wave as carrier	**1**
	DE	the frequency of carrier for FM (wtte)	**1**
	BCD	codes / carries / represents the signal / information /data / voltage	**1**
1 (a) (ii)	DE	less susceptible to noise or interference (picked up in transmission) / improved signal-to-noise ratio	**1**
	BCD	because signal can be restored or cleaned up at receiver / noise affects frequency less than amplitude	**1**
1 (a) (iii)	AB	to reduce the bandwidth / create more channels NOT simpler / cheaper circuits	**1**
1 (b)		Correct use / definition of each underlined term in description, [1] each:	
	BCD	• (amplitude of) <u>video signal</u> determines brightness / colour	**1**
	DE	• of a point on the screen called a <u>pixel</u>	**1**
	DE	• pixels arranged in rows called <u>lines</u>	**1**
	DE	• pixels are illuminated one at a time in a <u>raster</u> <u>scan</u>, line by line from top to bottom	**1**
	DE	• to make a complete <u>field</u>	**1**
	BCD	• <u>synchronisation</u> <u>signals</u> tell receiver when to start a new line or field	**1**
1 (c)	DE		**4**
	DE		
	BCD		
	BCD	[1] per correct box	

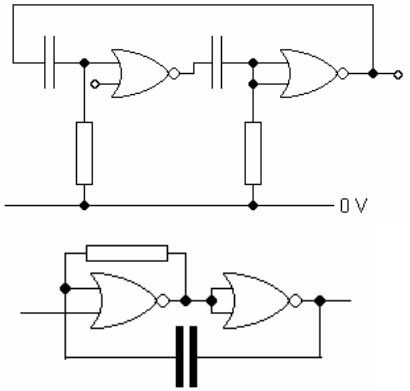
Question	Grade	Expected answer	Mark
2 (a)	DE	<u>current</u> amplified / delivered	**1**
	BCD	as signal / voltage passes from B to E	**1**
	AB	positive voltage transferred by NPN / negative voltage by PNP	**1**
2 (b)	DE	modulus of output less than modulus of input (any shape)	**1**
	DE	output horizontal when input crosses 0 V (any duration)	**1**
	BCD	correct shape, peak offset and duration of crossover distortion (by eye) look for parallel lines and apex through +2 V, -2 V	**1**
2 (c) (i)	DE	to switch on / have current in a transistor	**1**
	BCD	need voltage difference of 0.7 V between base and emitter ACCEPT V_{BE} = 0.7 V	**1**
	AB	so no signal transferred when amplitude less than 0.7 V (wtte)	**1**
2 (c) (ii)	BCD	op-amp output to bases	**1**
	BCD	inverting input to emitters (can be through resistor)	**1**
	AB	non-inverting input to 0 V via 47 kΩ	**1**

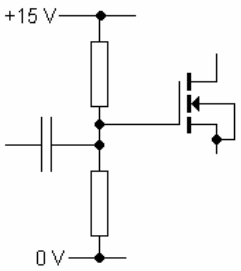
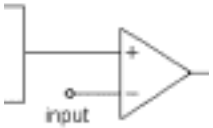
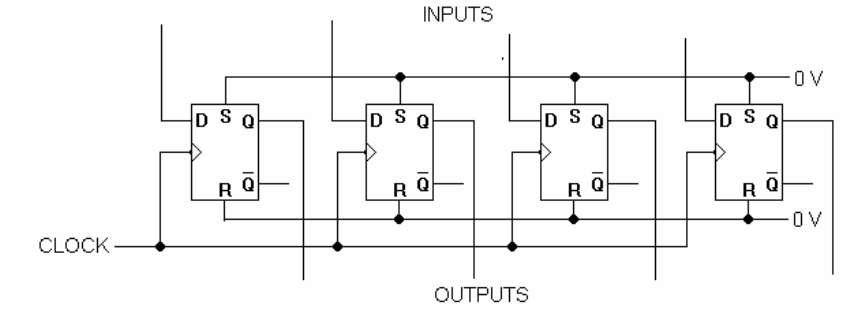




Question	Grade	Expected answer	Mark
2 (c) (iii)	DE	method (eor) [1], evaluation [1]	
	BCD	$I = V/R = 2.7 / 47\times10^{3} = 5.75\times10^{-5}$ A	**1**
		$P = VI = 2.7 \times 5.75\times10^{-5} = 1.6 \times10^{-4}$ W accept use of $P = V^2/R$ for [2]	**1**
2 (c) (iv)	DE	peak output power: method (eor) [1], evaluation [1]	
	BCD	$I = V/R = 2.7 / 8 = 0.338$ A	**1**
	AB	ecf incorrect V: $P = VI = 2.7\times 0.338 = 0.91$ W V = 2.0 V gives 0.5 W, V = 15V gives 28 W	**1**
		ecf incorrect output power: gain = $0.91 / 1.6\times10^{-4} = 5.7\times10^{3}$ 150 μW gives 6.07×10^{3}	**1**
3 (a)	DE	straight line through origin 	**1**
	DE	gain of -2 (by eye)	**1**
	BCD	saturates at ±13 V (by eye)	**1**
3 (b) (i)	BCD	arrow close to 4 kΩ resistor, to the left 	**1**
		ACCEPT drawn on the wire with upwards on the right or downwards on the left	

Question	Grade	Expected answer		Mark
3 (b) (ii)	AB	EITHER	OR	
	AB	Show: $G = -R_f / R_{in} = -4/60 = -0.0667$	Show: $I = V/R = 15/60\times10^{3} = 2.5\times10^{-4}$ A	**1**
	AB	Show: $V_{out} = G \times V_{in}$ (eor) $= -15 \times -0.0667 = +1$ V	Show: $V = IR = 2.5\times10^{-4} \times 4\times10^{3} = 1$ V	**1**
		Show: output $= 1 \times -2 = -2$ V		**1**
		ACCEPT use of summing amplifier formula	look for formula, powers of ten (as shown), correct signs	
		...		
3 (c) (i)	DE	maximum = 1.5 V		**1**
	DE	minimum = 0.5 V		**1**
3 (c) (ii)	BCD	need at least two samples per cycle		**1**
	AB DE	(fastest) cycle time $= 2 \times 50\times10^{-6}$ s $= 100\times10^{-6}$ s		**1**
	DE	$f = 1/T$ (eor)		**1**
		ecf incorrect T: $f = 1/100\times10^{-6} = 1.0\times10^{4}$ Hz = 10 kHz	$1 / 50\times10^{-6} = 20$ kHz worth [2]	**1**
3 (c) (iii)	DE	more input resistors / terminals / bits		**1**
	DE	smaller steps in output signal / greater resolution		**1**
		ACCEPT different resistors to increase range for [2]	NOT anything which improves response time	

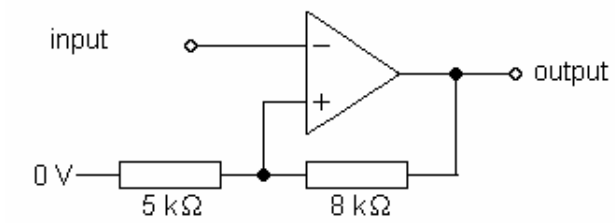
Question	Grade	Expected answer	Mark
4 (a)	DE BCD DE BCD AB	correct circuit (two possibilities), [1] per error or omission an error or omission can be • incorrect gates • R swapped for C consistently • missing RC *R* at least 5 kΩ EITHER $T = 1 / 70\times10^3$ (= 14 μs) OR $f \propto 1/RC$ (eor) *RC* between 30 μs and 5 μs ACCEPT both gates wired up as NOTs 	**2** **1** **1** **1**
4 (b)	DE BCD AB	square wave (wtte) alternates between 0 V and 0.7 V voltage across a (forward biased) diode independent of current / always 0.7 V	**1** **1** **1**
4 (c) (i)	AB DE	resistance changes rapidly at threshold voltage ACCEPT stated voltage e.g. 0.7 V, 2 V ... falling as voltage rises	**1** **1**
4 (c) (ii)	DE BCD AB	$G = 1 + R_f / R_d$ maximum: 1 + 1200/100 = 13 minimum: 1 + 1200 / ∞ = 1 ecf: use of $G = -R_f / R_{in}$ gives -12 for [1] and 0 for [1] ACCEPT 0 as maximum and -12 as minimum for [2]	**1** **1** **1**

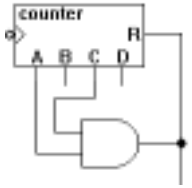
Question	Grade	Expected answer	Mark
4 (d) (i)	DE BCD AB	pulldown resistor to 0 V pullup resistor to +5 V or +15 V rail correct capacitor and gate connection 	1 1 1
4 (d) (ii)	DE DE DE	evidence of correct rules being used (e.g. voltage divider rule, $R = V/I$, voltage drop proportional to resistance) resistor values in correct ratio of 1:4 to achieve +3 V (e.g. 3 kΩ, 12 kΩ) resistors at least 1 kΩ.	1 1 1
5 (a)	DE		1
5 (b)	DE DE DE BCD AB	Q to outputs, $\overline{Q}$ ignored D to inputs CLOCK in parallel S and R to 0 V blobs / bridges as required 	1 1 1 1 1

Question	Grade	Expected answer	Mark
5 (c)	DE	counter has 2^4 = 16 states / goes from 0 to 15	**1**
	BCD	16 clock pulses per sample (eor)	**1**
	BCD	ecf incorrect number of clock pulses: 16 ×20 000 = 320 000 Hz = 320 kHz ecf: 4 pulses gives 80 kHz for [1], just 320 kHz for [2]	**1**
5 (d)	DE DE DE DE	[1] for each correct column, ecf from previous column look for signal to only change on every falling edge of signal in previous column	**4**
5 (e)	DE	oscillator provides (clock) pulses	**1**
	DE	which make counter outputs change	**1**
	DE	voltage at output of DAC determined by inputs from counter	**1**
	BCD	op-amp comparator compares DAC output with (analogue) input	**1**
	BCD	clock pulse to latch when DAC output rises above analogue input	**1**
	AB	latch stores digital output of system	**1**

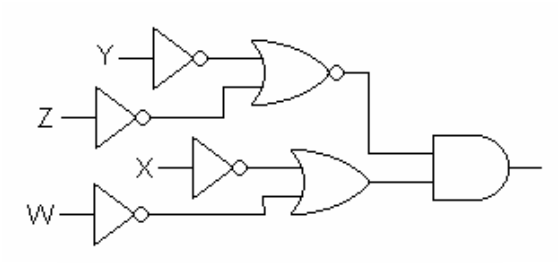
pulse	A	B	C	D
0	0	1	0	1
1	1	1	0	1
2	0	0	1	1
3	1	0	1	1
4	0	1	1	1

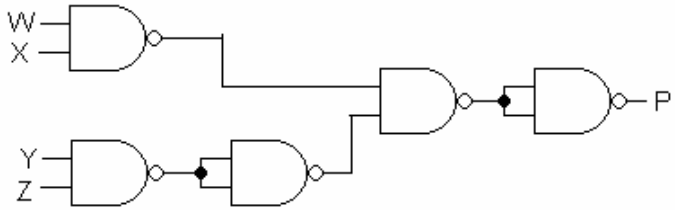
Question	Grade	Expected answer	Mark
6 (a) (i)	DE	reduces / eliminates noise / cleans up the signal ACCEPT interference for noise	1
	DE	by restoring signal to digital format / making into square wave / sharpening edges	1
6 (a) (ii)	BCD	positive feedback via resistor	1
	BCD	non-inverting input to 0 V via resistor	1
	DE	input to inverting input (can be via resistor)	1
	AB	correct resistor ratio of 8:5	1
	AB	calculation to justify correct values	1
	DE	resistors between 1 kΩ and 1 MΩ	1
6 (b)	DE	AND gate	1
	DE	output to R	1
	BCD	A and C as inputs ignore NOT gate from B	1
6 (c) (i)	DE	any of the following for [3]: ignore any incorrect processing	3
	DE	$P = \overline{W}.\overline{X}.Y.Z + W.\overline{X}.Y.Z + \overline{W}.X.Y.Z$	
	DE	$P = (\overline{W} + \overline{X}).Y.Z$	
		$P = (\overline{W.X}).Y.Z$	
		deduct [1] for each missing or incorrect term represented $(\overline{X} + \overline{W}).\overline{(\overline{Y} + \overline{X})}$ worth [0]	

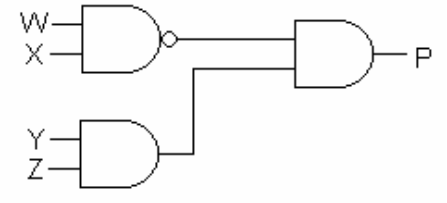


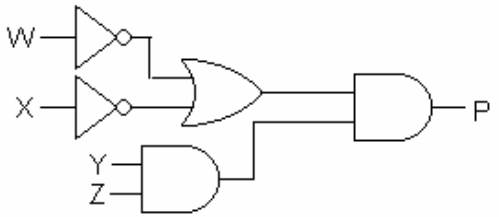


Question	Grade	Expected answer	Mark
6 (c) (ii)	BCD BCD AB	Award [1] for each correct (and different) use of Boolean algebra theorems illustrated below: De Morgan's Theorem: e.g. $\overline{\overline{Y} + \overline{Z}} = Y.Z$ De Morgan's Theorem e.g. $\overline{X} + \overline{W} = \overline{X.W}$ Brackets elimination e.g. $(\overline{X} + \overline{W}).(Y.Z) = \overline{X}.Y.Z + \overline{W}.Y.Z$ Term insertion e.g. $\overline{X}.Y.Z = (W + \overline{W}).\overline{X}.Y.Z$ Look for some steps in 6ci if necessary	3
6 (c) (iii)	DE DE BCD BCD	Useful logic circuit with labels W, X, Y and Z at input, P at output, and correct symbols Any circuit which has correct truth table deduct [1] for each extra / missing term of P achieved by the circuit e.g.	1 3









Question	Grade	Expected answer	Mark
7 (a)	DE DE BCD BCD	any of the following, for [1] each up to a maximum of [4] • tune by altering capacitance • so that resonant frequency matches channel carrier frequency • tuned circuit has large impedance / resistance only for this frequency • so current in aerial becomes voltage at output • lower frequency currents pass through inductor (to ground) • higher frequency currents pass through capacitor (to ground)	**4**
7 (b)	DE BCD AB	$f = \frac{1}{2\pi\sqrt{LC}}$ (eor) $C = \frac{1}{4\pi^2 f^2 L}$ $f = 1.2\times10^6$ Hz, $L = 270\times10^{-6}$ H (units conversion) ecf incorrect units conversion: $C = 6.5\times10^{-11}$ F = 65 pF	**1** **1** **1**
7 (c)	DE DE BCD	any of the following, [1] each up to a maximum of [3]: • lower Q / lower impedance at resonance • resonance less sharp / wider bandwidth • less selective / more stations at once • less sensitive / smaller signal received / harder to get weak stations • resonant frequency unchanged	**3**

Quality of Written Communication

3 The candidate expresses complex ideas extremely clearly and fluently. Sentences and paragraphs follow on from one another smoothly and logically. Arguments are consistently relevant and well structured. There will be few, if any, errors of grammar, punctuation and spelling.

2 The candidate expresses straightforward ideas clearly, if not always fluently. Sentences and paragraphs may not always be well connected. Arguments may sometimes stray from the point or be weakly presented. There may be some errors of grammar, punctuation and spelling, but not such as to suggest a weakness in these areas.

1 The candidate expresses simple ideas clearly, but may be imprecise and awkward in dealing with complex or subtle concepts. Arguments may be of doubtful relevance or obscurely presented. Errors in grammar, punctuation and spelling may be noticeable and intrusive, suggesting weaknesses in these areas.

0 The language has no rewardable features.

2530 Control Circuits

Question	Expected answer		Mark
1 (a)	RAM	Read And write Memory Data can be removed or stored in memory cells	[1]
	ROM	Read Only Memory Data can extracted from cells but cell contents cannot be changed	[1]
(b)	Byte	A group of 8 bits	[1]
	Word	A group of any number of bits	[1]
(c)	Data bus	Wires/tracks linking microprocessor to memory/ports Allows data to flow into or out of μP from/to memory/ports	[1] [1]
	Address bus	Wires/tracks linking microprocessor to memory/ports Information flow from μP -+ memory To communicate which cells in memory are to be accessed	[1]
(d)	BCD	Group of 4 bits representing a decimal number 0 to 9	[1]
	Hexadecimal	Number system with sixteen symbols Each symbol represents a 4-bit word	[1]
2 (a)	X =	Tristate	[1]
(b)	When the enable pin is logic 1	the output = the input	[1]
	When the enablepin is logic 0	the output floats (or wtte)	[1]
(c)	Digital Because tristate cannot handle analogue signals/is a digital component		[1]

Question	Expected answer	Mark
(d)	The D-type is wired to toggle That is the outputs alternate between 1 and 0 At the start of each clock cycle The output frequency is half the clock input frequency (any two points)	 [1] [1]
(e)	When Q = 1 and $\overline{Q}$ = 0 Tristate X is enabled so source A inputs data to line When Q = 0 and $\overline{Q}$ = 1 Tristate Y is enabled so source B inputs data to line	[1] [1]
3 (a) (i)	X correctly placed at the LDR	[1]
(ii)	Light Dependent Resistor	[1]
(b) (i)	Graph of Schmitt Any two constant saturation levels Any hysteresis shape Correct inverting hysteresis	 [1] [1]
(ii)	Switching thresholds = 18/(8+18) x 13 = 9V	[1] [1]
(iii)	Award full marks to any of several methods of showing voltage at A is -9V. eg If A is -9V there must be a pd of -9 - (-15) = 6V across the 2.4 kΩ Thus there must be 30 - 6 = 24V across the LDR So the resistance of the LDR must be four times greater than 2.4 kΩ.	 [1] [1]
(iv)	If voltage at A is +9V there is a pd of + 15 - (+9) = 6V across the LDR So the pd across the 2.4 kΩ resistor must be 30 - 6 = 24V So the LDR resistance must be one quarter of the 2.4k 600Ω	 [1] [1]

Question		Expected answer	Mark
(c)	(i)	Triac	[1]
	(ii)	Gate voltage = { 400 (400 + 2000)} x (13 - 0.7) = 2.05 V	[1] [1]
(d)	(i)	The Schmitt output is always saturated at ± 13 V Without the diode the gate voltage will always be ± 2.05 V The triac can fire on either polarity of gate so the triac is always on	[1] [1] [1]
	(ii)	When the diode is added the gate voltage is + 2.05V for positive saturation and is OV for negative saturation. So the triac only fires when V_{in} for the Schmitt goes below -9V ie in the dark	[1] [1]
(e)		r.m.s. current in lamp/triac = P / V = 85 / 24 = 3.54 A peak current in lamp/triac = $\sqrt{2}$ x 3.54 = 5.0 A	[1] [1] [1]
4 (a)	(i)	Total number of different addresses = 2^{10} = 1024	[1] [1]
	(ii)	Total number of cells = 1024 x 7 = 7168	[1]
	(iii)	Maximum unrepeated time = $\frac{\text{number of address locations}}{\text{rate of change of address}}$ = 1024 / 320 = 3.2 seconds	[1] [1]
	(iv)	Number of voltage levels = 2^7 = 128	[1] [1]

Question			Expected answer	Mark
		(v)	Maximum frequency in tune = ½ of memory access frequency = 160 Hz	[1] [1]
	(b)		The Reset pin is an input and inputs on (CMOS) chips should not be allowed to float The Reset pin is deactivated because the full range of counter outputs is required to maximise the number of address locations accessed	[1] [1]
5	(a)	(i)	Summing amplifier	[1]
		(ii)	Summing ouput P = -36/12(A+B) - 3 x sum of A and B	[1] [1]
		(iii)	Output B must be made negative otherwise P will always be negative Causing the integrator output to be always positive And the heater to be always on	[1] [1]
	(b)	(i)	Integrator drawing non-inverting input connected to OV Resistor to inverting input Capacitor in negative feedback	[1] [1] [1]
		(ii)	Integrator response -ve Output increases (linearly) till + ve saturation 0V No integration and output stays frozen (or wtte)	[1] [1] [1]
		(iii)	When Q is positive (>0. 7V) Transistor turns on and operates heater When Q is negative Transistor turns off so heater is off	 [1]
	(c)	(i)	When the temperature gets too hot P must be made to go +ve By making the voltage A become smaller than the fixed voltage at B So the thermistor must be R_2 Because thermistor resistance decreases as the temperature gets hotter	 [1] [1] [1]

Question	Expected answer	Mark
	(ii) The required temperature is set by the (negative) voltage at B If the temperature is too cold then the voltage at A will be more +ve than the -ve B So the output P will be a negative voltage because P = -3 x (A + B) This causes the integrator output Q to ramp positively Turning on the heater and causing the temperature to increase But the rate of increase of temperature decreases as the temperature increases Because the voltage at P becomes smaller and smaller Eventually the voltage at P becomes zero when A = -B And the output voltage Q freezes on a small value to compensate heat loss (any four marking points)	**[1][1]** **[1][1]**

Question	Expected answer				Mark
6	**(a)**	**Address**	**Contents**	**Explanation**	
	00	3A	EF	Swallow input	**[1]**
	02	E6	E0	Mask out all the Amplitude code = ???0 0000	**[1]**
	04	C6	1F	Add 1F to the Amplitude code to maximise value	**[1]**
	06	32	AA	Move new Amplitude code to M(AA) = ???1 1111	
	08	3A	EF	Swallow input	**[1]**
	0A	E6	1E	Mask out all but Frequency code = 000? ???0	**[1]**
	0C	C6	01	Add 01 to Frequency code to maximise value	**[1]**
	0E	32	BB	Move new Frequency code to M (BB) = 000? ???1	
	(b)	**Address**	**Contents**	**Explanation**	
	10	3A	EF	Swallow the input	**[1]**
	12	E6	01	And check for RUN button	**[1]**
	14	C2	60	If pushed then jump to address 60	**[1]**
	16	C3	00	If not pressed then return to start of program	**[1]**

for correct addresses **[1]**

NOTE: there are various ways of correctly delivering this coding

	(c)	**Address**	**Contents**	**Explanation**	
	60	3A	AA	Recover the maximum amplitude data to accumulator	
	62	32	CC	Move the maximum amplitude to memory M(CC) (Memory CC will hold the decreasing value of current amplitude starting from the maximum amplitude)	**[1]**
	64	3A	CC	Recover current amplitude value into accumulator	
	66	32	FF	Output current amplitude to M(FF)	**[1]**
	68	D6	01	decrement **current amplitude** value	**[1]**
	6A	CA	90	If **amplitude** has been reduced to zero then jump	**[1]**

			to 10 (to test for run switch)		
	6C	32	CC	If amplitude not yet zero then restore in M(CC)	**[1]**
	6E	3A	BB	Recover frequency value to accumulator	**[1]**
	70	D6	01	Subtract 01 repeatedly until	
	72	C2	70	frequency value goes to zero (time delay)	**[1]**
	74	C3	64	return to 64 to further reduce amplitude	**[1]**

Grade Thresholds

Advanced GCE Electronics (3826/7826)
June 2009 Examination Series

Unit Threshold Marks

Unit		Maximum Mark	A	B	C	D	E	U
2526	Raw	120	85	77	69	61	53	0
	UMS	120	96	84	72	60	48	0
2527	Raw	90	61	55	49	44	39	0
	UMS	90	72	63	54	45	36	0
2528	Raw	78	61	54	47	40	33	0
	UMS	90	72	63	54	45	36	0
2529	Raw	120	77	68	59	50	42	0
	UMS	120	96	84	72	60	48	0
2530	Raw	90	62	55	49	43	37	0
	UMS	90	72	63	54	45	36	0
2531	Raw	90	71	64	58	52	46	0
	UMS	90	72	63	54	45	36	0

Specification Aggregation Results

Overall threshold marks in UMS (ie after conversion of raw marks to uniform marks)

	Maximum Mark	A	B	C	D	E	U
3826	300	240	210	180	150	120	0
7826	600	480	420	360	300	240	0

The cumulative percentage of candidates awarded each grade was as follows:

	A	B	C	D	E	U	Total Number of Candidates
3826	29.83	61.4	77.19	93.86	100	100	114
7826	32.47	52.21	67.27	84.68	96.1	100	348

462 candidates aggregated this series

For a description of how UMS marks are calculated see:
http://www.ocr.org.uk/learners/ums_results.html

Statistics are correct at the time of publication.

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