THIS IS A LEGACY SPECIFICATION

OCR
RECOGNISING ACHIEVEMENT

**ADVANCED SUBSIDIARY GCE**

# ELECTRONICS

Signal Processing

**2527**

Candidates answer on the question paper

**OCR Supplied Materials:**
None

**Other Materials Required:**
- Calculator

**Monday 18 May 2009**
**Morning**

**Duration:** 1 hour 15 minutes

*CUP/T62405*

| Candidate Forename | | Candidate Surname | |
|---|---|---|---|

| Centre Number | | | | | | Candidate Number | | | | |
|---|---|---|---|---|---|---|---|---|---|---|

**INSTRUCTIONS TO CANDIDATES**

- Write your name clearly in capital letters, your Centre Number and Candidate Number in the boxes above.
- Use black ink. Pencil may be used for graphs and diagrams only.
- Read each question carefully and make sure that you know what you have to do before starting your answer.
- Answer **all** the questions.
- Do **not** write in the bar codes.
- Write your answer to each question in the space provided, however additional paper may be used if necessary.

**INFORMATION FOR CANDIDATES**

- The number of marks is given in brackets **[ ]** at the end of each question or part question.
- The total number of marks for this paper is **90**.
- You may assume, unless otherwise stated, that:
  - **(i)** the p.d. across a forward-biased silicon diode is 0.70V,
  - **(ii)** the base-emitter p.d. for a conducting silicon transistor is 0.70V,
  - **(iii)** the power supplies for operational amplifiers are +15V and –15V,
  - **(iv)** the saturation levels for operational amplifiers are +13V and –13V,
  - **(v)** logic 1 = 5V and logic 0 = 0V.
- The quality of written communication will be assessed in your answers to all questions.
- This document consists of **16** pages. Any blank pages are indicated.

**A calculator may be used for this paper**

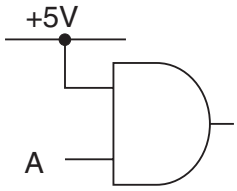
| Examiner's Use Only: | | | |
|---|---|---|---|
| 1 | | | |
| 2 | | | |
| 3 | | | |
| 4 | | | |
| 5 | | | |
| 6 | | | |
| 7 | | | |
| **QWC** | | | |
| **Total** | | | |



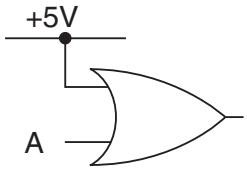

OCR is an exempt Charity

**1** Parts **(a)** to **(e)** below show a series of 2-input logic gates. In each case one of the inputs is connected to +5V or to 0V while the other input is connected to a logic input A. For each logic gate, state the type of gate being used and complete the equation for the output Q.

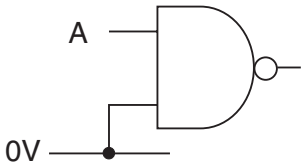
Choose from the list. **0** **1** **A** **$\bar{A}$**

**(a)** 

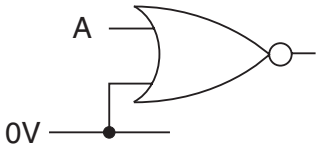

Q = ..... Type of logic gate = ..... **[2]**

**(b)** 

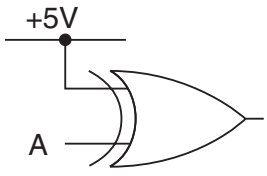

Q = ..... Type of logic gate = ..... **[2]**

**(c)** 


Q = ..... Type of logic gate = ..... **[2]**

**(d)** 


Q = ..... Type of logic gate = ..... **[2]**

**(e)** 


Q = ..... Type of logic gate = ..... **[2]**

**2** Fig. 2.1 shows a circuit containing three logic gates connected to two inputs X and Y.

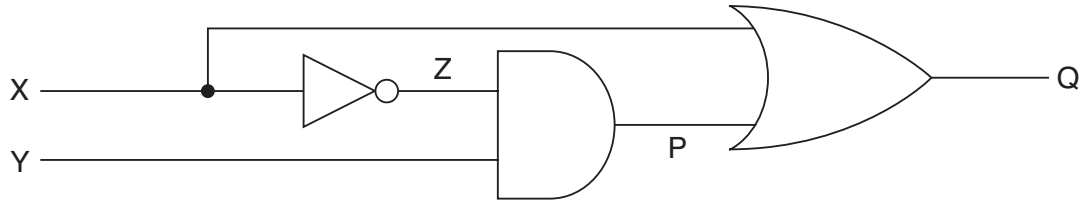



**Fig. 2.1**

**(a)** Write down a Boolean expression for Z in terms of X.

Z = ..... **[1]**

**(b)** Write down a Boolean expression for P in terms of X and Y.

P = ..... **[1]**

**(c)** Write down a Boolean expression for Q in terms of X and P.

Q = ..... **[1]**

**(d)** Write down a Boolean expression for Q in terms of X and Y.

Q = ..... **[1]**

**(e)** **(i)** Apply the race hazard theorem to your expression for **(d)**.

Q = ..... **[1]**

**(ii)** Use the rules of Boolean algebra to show that the circuit of Fig. 2.1 can be reduced to a single logic gate.

**[2]**

**(iii)** Explain how the circuit of Fig. 2.1 operates. Use the following beginning as a guide.

*When X is logic one then Q =* ..... *because* .....

.....

*and when X is logic zero then Q =* ..... *because* .....

..... **[2]**

**3** Fig. 3.1 shows an incomplete circuit for a **treble cut** filter which is to be operated from two 12V d.c. supplies. A signal source is used as the input to the filter.

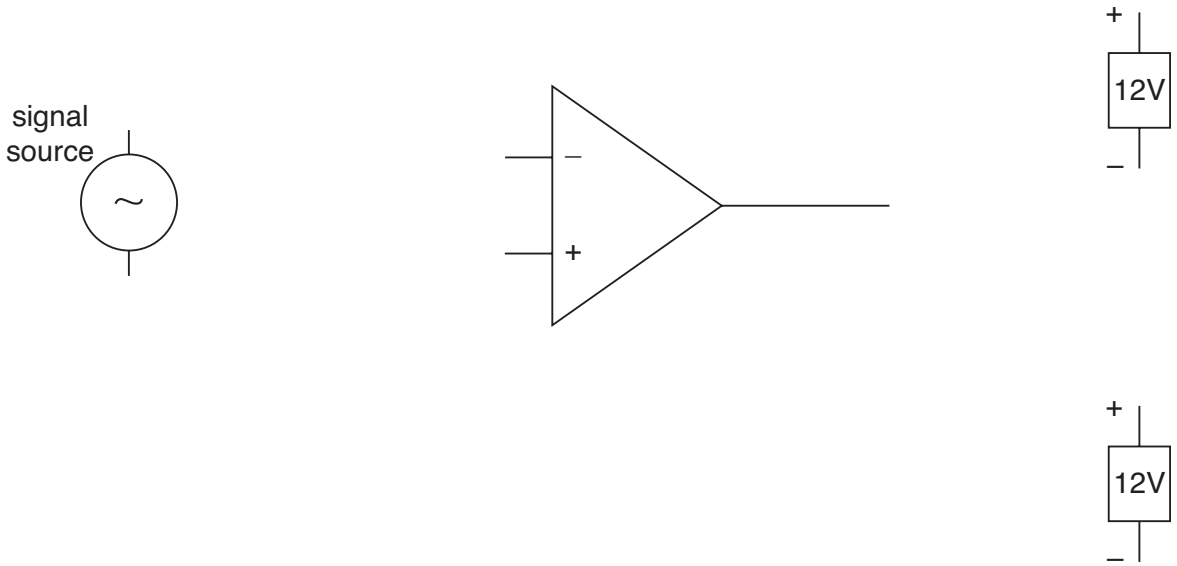



**Fig. 3.1**

The filter circuit has the following characteristics:

- Input resistance 1.7 kΩ
- Maximum gain 400
- Break frequency 150 Hz

**(a)** Complete Fig. 3.1 to show the circuit diagram of the treble cut filter. In particular, you must

- produce and label three power lines +12V, 0V and –12V from the two 12V supplies
- show how the signal source is connected as an input
- label any resistors and capacitors with their values
- show all formulae you have used
- show all your calculations.

**[11]**

**(b)** On the axes of Fig. 3.2, draw the frequency response to the treble cut filter of part **(a)**. Label the logarithmic axes with appropriate values.

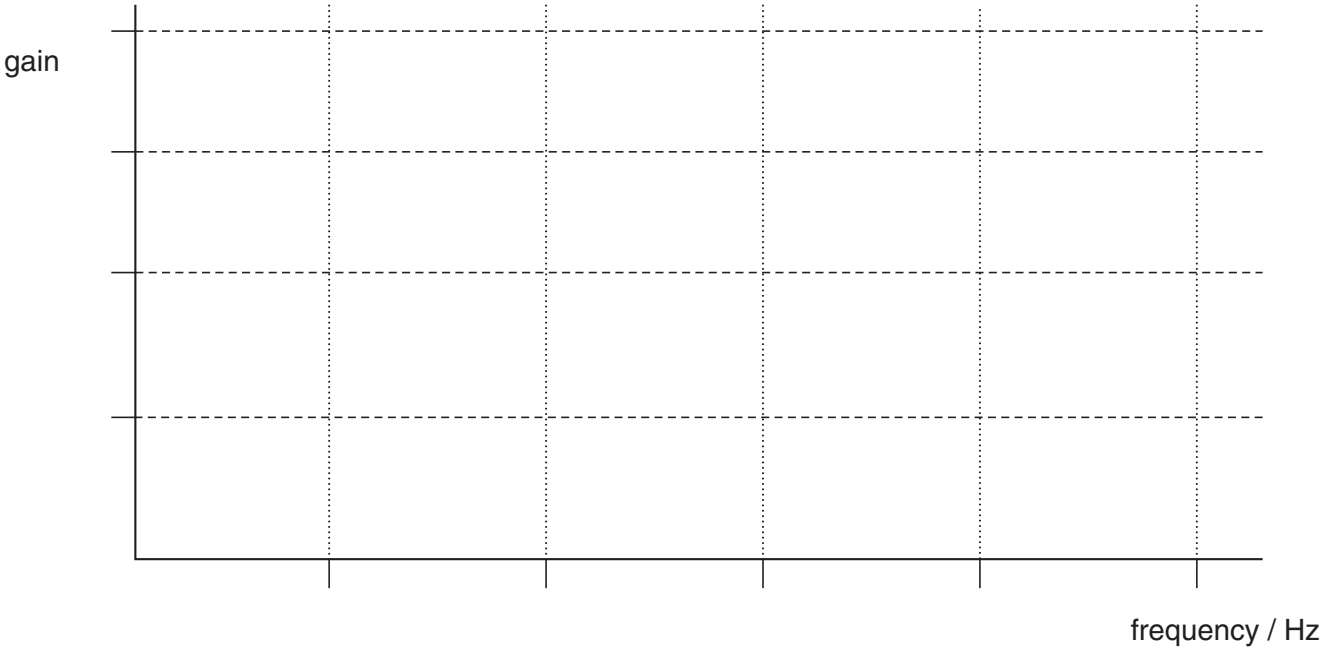



**Fig. 3.2**

**[4]**

**4** A teacher sets up the circuit shown in Fig. 4.1.

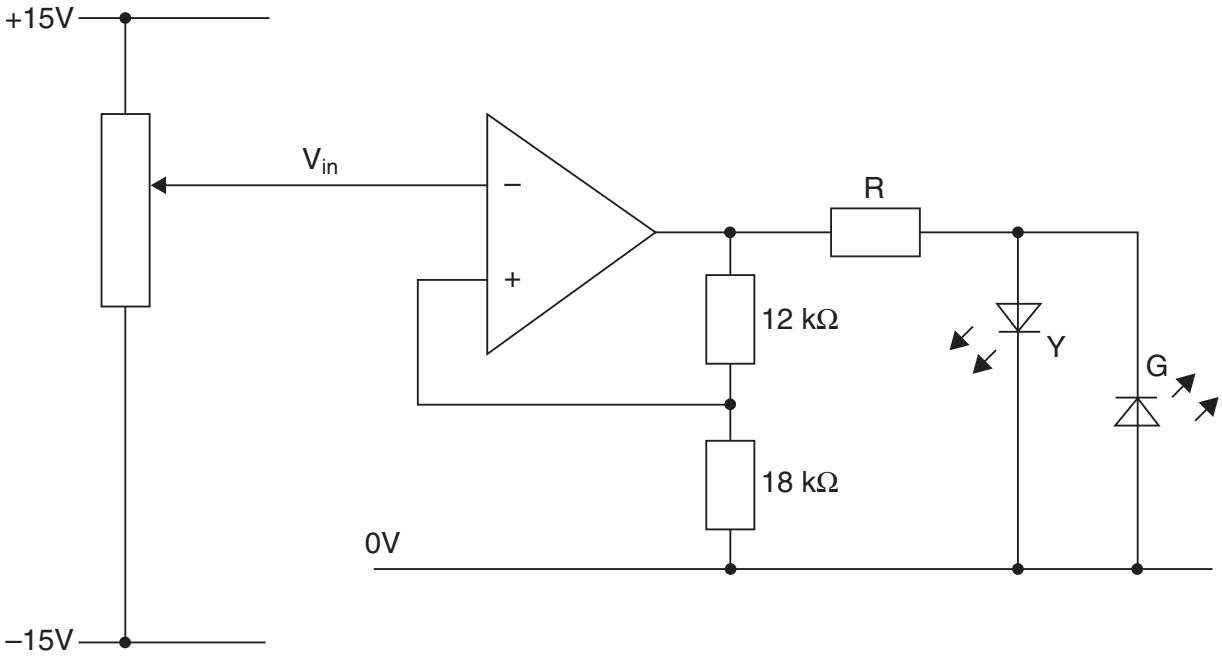



**Fig. 4.1**

**(a)** State the name of the type of op-amp circuit of Fig. 4.1.

..... **[1]**

**(b)** The circuit contains a potentiometer. Draw a ring around this component. **[1]**

**(c)** Calculate a suitable value for the resistor R to limit the current in the LEDs to 5 mA.

resistor R = ..... Ω **[3]**

**(d) (i)** The input voltage $V_{in}$ is set to +15 V.
Complete the sentences below for the LEDs.

LED G will be ..... because the op-amp .....

LED Y will be ..... **[3]**

**(ii)** Show that the switching thresholds of the circuit are about ±8V.

**[2]**

**(iii)** The input voltage $V_{in}$ is now decreased slowly from +15V to –15V.
Explain how the light intensity of the LEDs changes during this period.

.....

.....

.....

..... **[3]**

**(iv)** The input voltage $V_{in}$ is now increased slowly from –15V to +15V.
Explain how the light intensity of the LEDs changes during this period.

.....

.....

.....

..... **[2]**

**5** Fig. 5.1 shows a 1 Hz clock feeding pulses into a 4-bit up-counter.

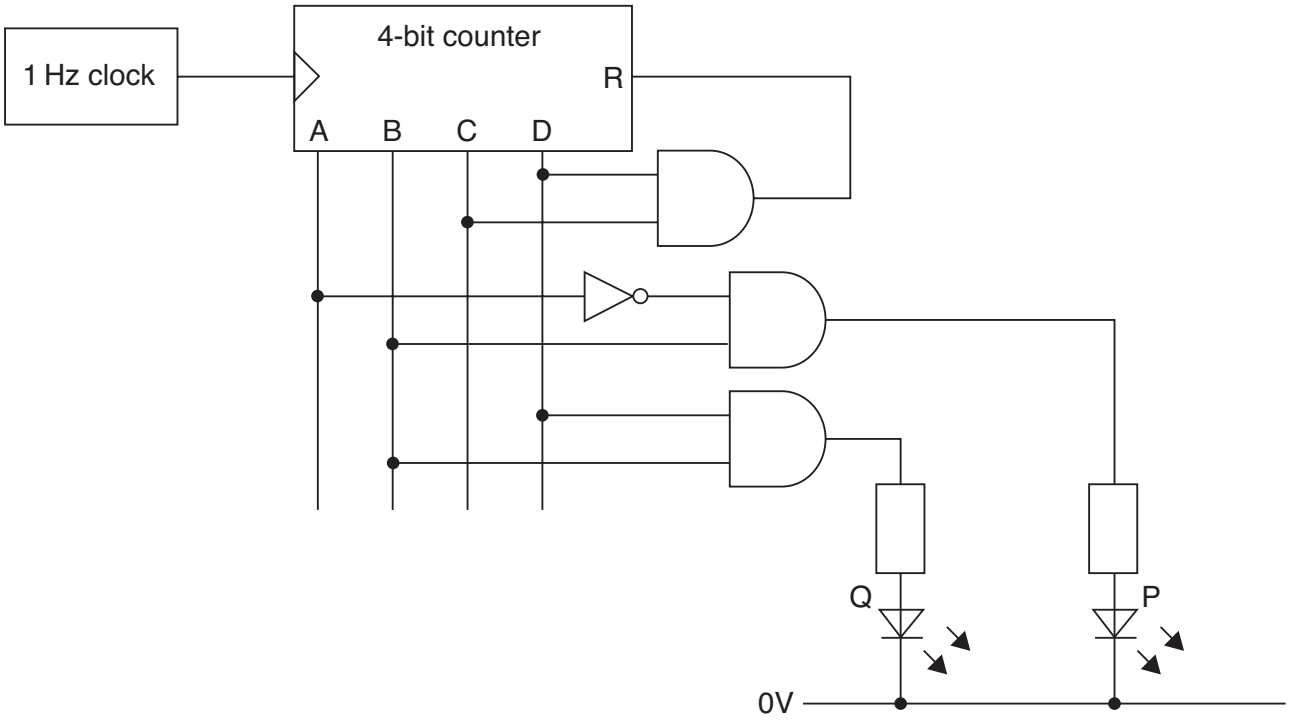



**Fig. 5.1**

**(a)** Complete the table below to show how the output states of the counter change with the number of clock pulses input. The counter starts from a reset state of DCBA = 0000 where A is the least significant bit.

| clock pulse | A | B | C | D |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | | | | |
| 2 | | | | |
| 3 | | | | |
| 4 | | | | |
| 5 | | | | |
| 6 | | | | |
| 7 | | | | |
| 8 | | | | |
| 9 | | | | |
| 10 | | | | |
| 11 | | | | |
| 12 | | | | |
| 13 | | | | |
| 14 | | | | |
| 15 | | | | |

**[5]**

**(b) (i)** Write down the output states of the counter which are necessary to cause LED P to glow.

..... **[1]**

**(ii)** Write down the output states of the counter which are necessary to cause LED Q to glow.

..... **[1]**

**(c)** Given that the clock in Fig. 5.1 has a frequency of 1 Hz, state

**(i)** how the brightness of LED P changes with time

.....

.....

..... **[3]**

**(ii)** how the brightness of LED Q changes with time.

.....

.....

..... **[2]**

**6** A student wishes to investigate their guitar pick-up, amplifier and loudspeaker system.
Fig. 6.1 shows the guitar pick-up being connected directly to an oscilloscope.

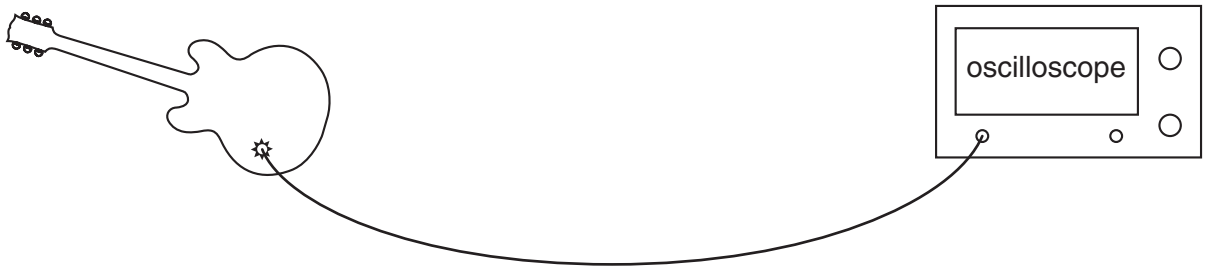



**Fig. 6.1**

When the student plays chords on the guitar, the oscilloscope shows a peak voltage of 158 mV.

The student now connects the pick-up to the amplifier input and the amplifier output to the loudspeaker.
One trace of the oscilloscope still shows the pick-up output while the other oscilloscope trace shows the loudspeaker input. This is shown in Fig. 6.2.

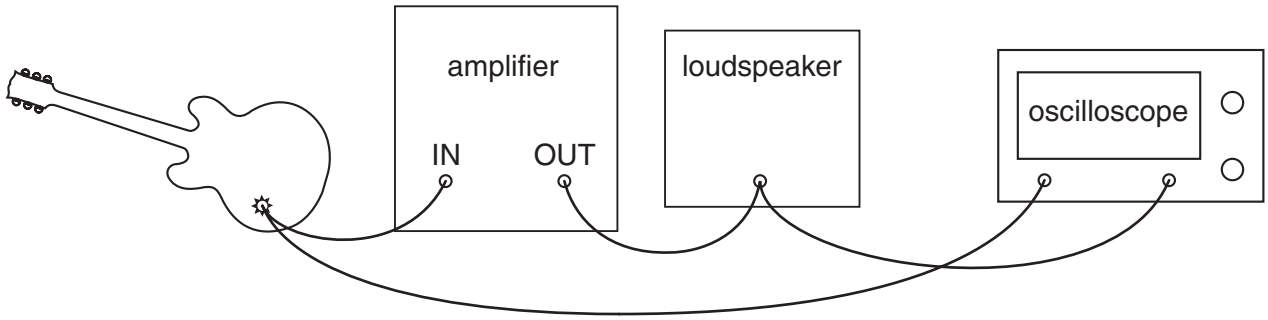



**Fig. 6.2**

When the student plays the guitar again, the oscilloscope shows:

- the peak voltage input to the amplifier has dropped to 100 mV
- the peak voltage output from the amplifier is 18 V.

The student looks up the data on his system and finds that:

- the amplifier input resistance is 4.7 kΩ
- the amplifier output resistance is 4 Ω
- the speaker resistance is 12 Ω.

**(a) (i)** Show that the voltage 'lost' inside the guitar pick-up is about 60 mV.

**[1]**

**(ii)** The amplifier input resistance is 4.7 k Ω.
Show that the peak current supplied by the pick-up is about 20 μA.

**[2]**

**(iii)** Calculate the output resistance of the guitar pick-up.

output resistance = ..... Ω **[2]**

**(b) (i)** The loudspeaker resistance is 12 Ω.
Calculate the peak current in the loudspeaker.

peak current = ..... A **[2]**

**(ii)** Calculate the mean power delivered to the loudspeaker.

mean power = ..... W **[3]**

**(c)** The amplifier output resistance is 4 Ω.
Calculate the voltage gain of the amplifier.

voltage gain = ..... **[3]**

**7** Fig. 7.1 shows part of a keypad circuit in which only **one** of the six push button switches (numbered 1 to 6) is to be pressed at a time.

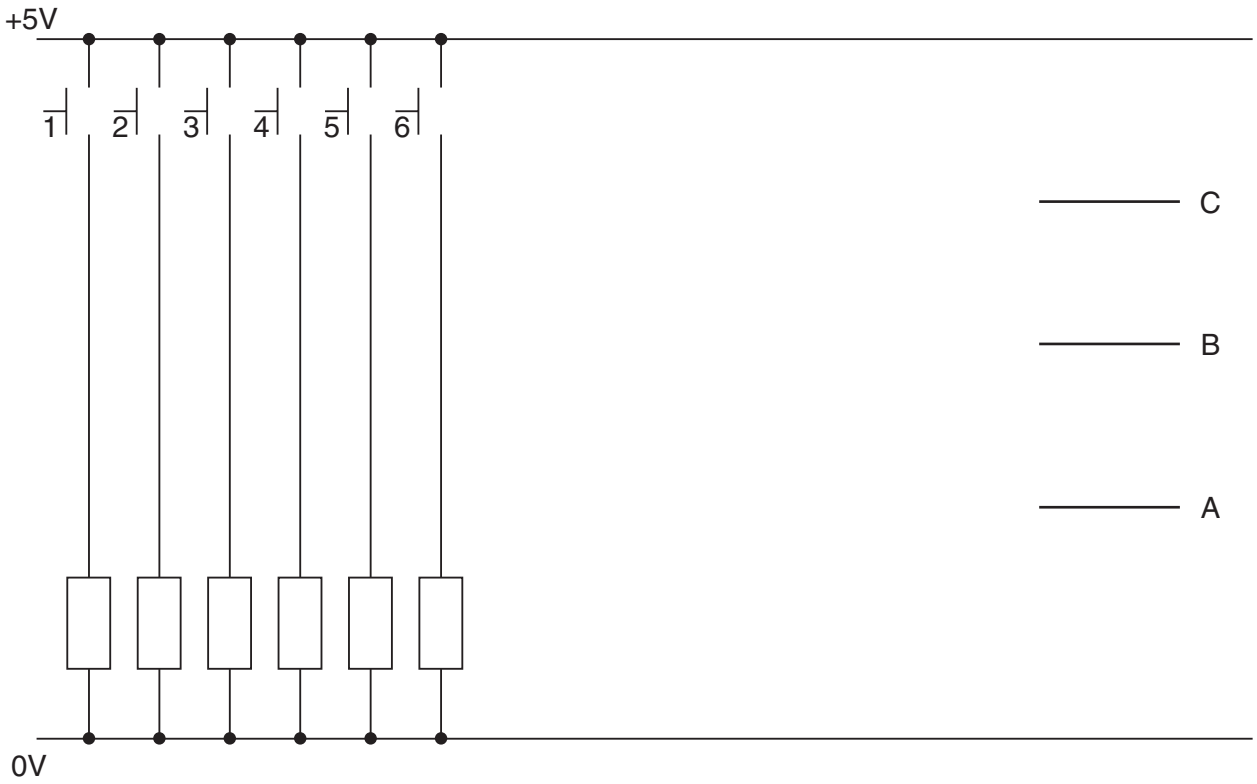



**Fig. 7.1**

When a switch is pressed, the 3-bit binary code CBA of the decimal number of the switch is to be generated. A is the least significant bit of the code CBA.

**(a) (i)** Complete the table below to show the operation of the keypad.
The first two lines have been done for you.

| Key 1 | Key 2 | Key 3 | Key 4 | Key 5 | Key 6 | C | B | A |
|---|---|---|---|---|---|---|---|---|
| *0* | *0* | *0* | *0* | *0* | *0* | *0* | *0* | *0* |
| *1* | *0* | *0* | *0* | *0* | *0* | *0* | *0* | *1* |
| | | | | | | | | |
| | | | | | | | | |
| | | | | | | | | |
| | | | | | | | | |
| | | | | | | | | |

**[3]**

**(ii)** Complete the circuit of Fig. 7.1 using logic gates. **[4]**

**(b)** In the keypad of Fig. 7.1, when a switch is released the code CBA simply returns to zero 000. It is required to store the code CBA on three D-type flip-flops each time a switch is pressed.

**(i)** Using Fig. 7.2 as a guide, complete the diagram to show how this can be done. Label appropriate inputs and outputs.

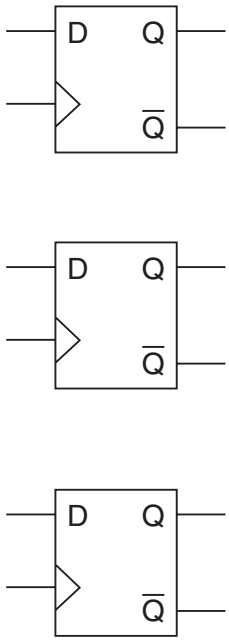



**Fig. 7.2**

**[4]**

**(ii)** Explain how your code storage system operates.

.....

.....

..... **[2]**

**Quality of written communication [3]**

**BLANK PAGE**

**PLEASE DO NOT WRITE ON THIS PAGE**

**BLANK PAGE**

**PLEASE DO NOT WRITE ON THIS PAGE**

**PLEASE DO NOT WRITE ON THIS PAGE**