GCE

Electronics

Advanced GCE **A2 7826**

Advanced Subsidiary GCE **AS 3826**

Report on the Units

June 2009

3826/7826/MS/R/09

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Advanced GCE Electronics (7826)

Advanced Subsidiary GCE Electronics (3826)

REPORTS ON THE UNITS

2526 Foundations of Electronics

General Comments

This paper was only taken by candidates wishing to improve their marks from last summer's exams. The range of ability of those students was surprisingly large, with fewer weak students than normal. The structure of the paper was kept the same as previous years, with no attempts at innovation or improvement. There was no indication that candidates ran out of time. Too many candidates show a poor understanding of basic d.c. electricity, often freely interchanging the terms current and voltage in their explanations of circuit behaviour. This is particularly problematic for candidates when they are presented with a circuit built out of passive components (such as a power supply or regulator, both of which featured on this year's paper) or have to explain the operation of an analogue circuit.

Question 1

This question about analysing combinations of logic gates was similar to the first question of previous papers, and most candidates earned high marks for most sections. As expected, weak candidates struggled with the last part which required them to describe the behaviour of a logic gates with words instead of algebra or tables - one mark was regularly lost because they failed to specify the output state for all four different input states.

Question 2

Every candidate correctly identified and named the LDR. However, only the strongest candidates were able to correctly draw in the protection diode. The calculation of resistor value was only difficult for weak candidates - many could guess the correct value but were unable to justify it. Explaining the operation of an analogue circuit proved to be difficult. Centres need to encourage their candidates to talk about voltage and current instead of signal and be specific about the part of the circuit they are discussing.

Question 3

Questions which involve the charging and discharging of capacitors have always proved to be troublesome for past candidates. This question compounded the difficulty by presenting a digital component in a novel context. All candidates managed to correctly sketch the output of the NOT gate from the information provided, but a significant proportion had problems in calculating the time constant - usually because they used 0.7RC. Even the strongest candidates only had moderate success in calculating the time delay - one suspects that many centres do not bother to teach this aspect of the course, depriving their candidates of a potential mark or two. The last part of the question required candidates to understand the operation of the circuit. Too often, it was obvious that candidates were not tracing voltages from input to output, but presuming the answer and working backwards to justify it. In particular, the incorrect notion that Q cannot be high until CK goes high was widespread amongst weaker candidates.

Question 4

Most candidates were able to correctly interpret the characteristic curve of the amplifier, although too many weak candidates failed to indicate that they had actually read values off the graph and worked out the gain instead of working back from the answer provided and quoting values which did not match the graph. Sketching the output waveform was not a problem for most candidates, providing that they remembered the saturation levels of +13 V and -13V. Designing an inverting amplifier was within the capabilities of most candidates, but even the

strongest lost marks through careless drawing (such omitting the 0 V at the end of the ground supply rail) or selecting resistor values below 1 kilohm.

Question 5

This question required candidates to have a good understanding of the behaviour of currents in a parallel circuit. Many did not. Although the vast majority of candidates could correctly draw the voltmeter then calculate the resistance and power of the load, only a minority successfully calculated the current in the Zener diode when the load current was 50 mA. Most of the descriptions of the Zener diode characteristic were poor, mainly because of incorrect use of the terms voltage and current.

Question 6

As expected, this proved to be the hardest question of the whole paper. Few candidates could correctly remember the arrangement of diodes for a diode bridge, and even fewer could correctly connect it to the load and transformer. Only some of the strongest candidates could use peak-to-rms conversion and 1.4 V diode loss to explain the required voltage at the secondary of the transformer. Most candidates failed to halve the period of the mains voltage to find the discharge time of the capacitor, and only a minority knew how to calculate the ripple across the load. This is probably because weak candidates are unable to recall a formula which has only one application and therefore does not get learned through repetition - unlike R=V/I or P=VI.

Question 7

This question provided excellent discrimination, with only the strongest candidates recognising the virtual earth at the input and the negative value of the voltage at the output.

Question 8

Although almost all candidates remembered the truth table for a NAND gate, some were unable to describe the behaviour of an OR gate. Drawing the correct circuit was difficult for weak candidates, who often failed to justify their circuit with a truth table showing outputs of all the gates used. As expected, only the strongest candidates were able to provide coherent explanations of the operation of the bistable circuit, although the majority of candidates could correctly summarise the behaviour with a timing diagram.

Question 9

Although all candidates could correctly identify the current-limiting resistor, too many failed to use the correct voltage drop in calculating its resistance, suggesting a lack of understanding of the way voltage is shared in a series circuit. Unexpectedly, few candidates could correctly draw the I-V characteristic for the LED, often failing to have the current rise steeply enough once conduction had been achieved. Perhaps centres don't allow candidates enough opportunities to measure these characteristics for themselves?

2527 Principal Moderator's Report - Signal Processing Circuits

General Comments

In what was the last sitting of this legacy AS specification, the majority of the candidates were able to demonstrate some degree of understanding of most aspects of the course.
The combinational logic questions were generally well answered but many could not apply the rules of Boolean algebra. For many it was relatively easy to design a treble cut filter but more of a challenge to sketch its frequency response. The action of a potential divider was clear to many but the meaning of switching thresholds for a Schmitt Trigger was not. The operation of a 4-bit up-counter was clearly understood whilst the action of the counter reset was not.

Question 1

This question was based upon the identification of logic gate arrangements and their Boolean algebra representations. Candidates were required to complete Boolean expressions by selecting items from a list provided. As expected nearly all candidates were able to correctly identify the type of logic gate. However a significant number of candidates did not select from the list provided when completing the Boolean expressions. For example for the AND gate Q= A.+5 was written instead of the expected answer of Q=A.

Question 2

This question required an understanding of combinational logic and Boolean algebra. Candidates were asked to produce Boolean algebra expressions to represent various points in the circuit and to combine them together, using the rules of Boolean algebra, to arrive at a simplified expression. The majority of candidates were able to generate the Boolean expressions required for parts (a) to (d). However part (e) proved to be challenge for a large number of candidates with very few able to demonstrate an understanding of the Race Hazard Theorem for part (i) and, although many recognised the combination of logic gates represented an OR gate, very few were able to use Boolean algebra to prove it as required for part (ii). In part (iii), although many candidates were able to explain why Q=1 when X held a value of 1, fewer were able to visualise the outcome when X held a value of 0.

Question 3

A treble cut filter was the basis of this question, with candidates being asked to complete a suitable circuit diagram with appropriate values and sketch its frequency response.
Many aspects of completing the circuit were well done by the majority of candidates, including the positioning of the capacitor, the use of both the break frequency and gain formula and the correct use of the inverting input. However some candidates found the selection of the + and – power supply a challenge along with the positioning of zero volts line and the connection of the signal source. The frequency response of the filter required for part (b) was only successfully completed by a few candidates. Although many understood the relevance of the break frequency and could draw the general shape of the filter, few were able to use logarithmic axes correctly and there were very few instances of the factor of 10 decrease beyond the break frequency being seen.

Question 4

The vast majority of candidates were able to correctly identify the circuit of this question as a Schmitt Trigger and the location of the potentiometer as required for parts (a) and (b). When required to determine a suitable limiting resistor for part (c), many candidates did not allow for the p.d. of the LED and incorrectly used 13 V in the calculation. The responses to parts (d) (i) and (ii) were generally correct and candidates clearly understood how to use the potential divider formula. However in parts (d) (iii) and (iv) there were many instances of a lack of understanding of the meaning of switching threshold and the general properties of a Schmitt Trigger when used in this way.

Question 5

This question focussed upon the action of a 4-bit up-counter and the role of the reset pin on the counter chip. The majority of the table in part (a) was correctly completed by most candidates with the significance of A being the least significant bit being clearly understood. However many candidates failed to identify the need for a reset on clock pulse 12 when both outputs C and D have a value of 1. Of those that did, some treated pulse 13 as the reset condition. Allowing for the errors of missing the reset condition, many candidates correctly stated the outcome states for part (b) (i) and (ii). The variation of brightness of the LEDs in part (c) (i) and (ii) was less clearly understood with many candidates expecting a continuous variation in intensity rather than the pulsing that would have occurred.

Question 6

Many candidates were able to demonstrate a clear understanding of some of the terminology associated with an amplification system in this question. The difference between mean and peak power in part (b) and the meaning of voltage gain in part (c) were understood by fewer candidates. Part (a) (i) and (ii) were generally well answered but many did not realise which voltage was required to calculate the pick-up output resistance in (iii). In part (b) (ii) there were many instances when the peak power was not halved to give the mean value. Whilst in part (c), many failed to include the p.d. across the output and used a value of 18 V instead of 24 V to calculate the voltage gain.

Question 7

This question was concerned with the action of a keypad circuit and the role of D-type flip-flops in storing a code. Part (a) was generally well done by the majority of candidates with a number of different solutions offered for (ii), although many recognised the use of a 3 input OR gate and selected the correct combination of switch inputs. The design of a circuit using the D-types for part (b) was less well done and there were many examples where candidates arranged the D-types to "toggle" the outputs or act as counters. In only a few instances was a 3 input OR gate used to clock the D-types. Only a few candidates correctly explained the operation of the code-retaining system in part (b) (ii) with many responses just concentrating on the general action of a D-type.

2528 Electronics (Project 1)

In this final (legacy) AS coursework module, very few candidates had been entered. Of these, the vast majority had been marked very well and no issues arose. This was the ninth year that the coursework module 2528 has been offered and it should be of no surprise that the raw marking was very accurate. For the small number whose marks were deemed to be outside the tolerance allowed by OCR, problems arose with the same criteria that have been consistently mentioned in these reports. It is worthwhile reminding centres of these problem areas as they are still very much part of the new specification.

Criterion D (building subsystems and the subsequent testing of the subsystems and the final circuit) – in order to score highly for this criterion, candidates must show evidence that all subsystems and the final circuit have been fully tested. As has often been mentioned, testing evidence can be in the form of scope traces, either Picoscope traces or clear, colour photos of screen shots with accompanying time-base and voltage amplification settings. For digital circuits, it may be more appropriate to offer photos of the state of LEDs hung on the outputs, or possibly a photo of the reading given by a logic probe. It is not necessary to offer evidence for all the tests performed on a subsystem. For example, if a filter is being tested, then it would be acceptable to offer evidence of a single test result, followed by a table of results of all data taken for the filter throughout the given frequency spectrum.

Criterion E links with criterion D and has also caused some trouble in the past. Having done the testing and obtained the raw data, candidates are then expected to fully analyse the data and relate it back to the subsystem specification. Often, this will include numerical analysis which some candidates fail to address. It must be remembered that the final circuit should also be thoroughly tested and analysed. For some candidates, this is often overlooked yet it is a vital part of any testing and analysis programme.

How much of the original specification has been achieved (Criterion F) also caused trouble. Again, there must be evidence within the report to support the awarded mark. A mark of 4/4 cannot be awarded if the evidence is not to be found in the report.

Finally, criterion K (accuracy of the report) has also been noted as a criterion which is often marked too generously. Candidates fail to report on any debugging they perform in the building of the circuits – it seems that many candidates build all the subsystems perfectly first time and do not experience problems. This is most unlikely and the debugging performed should be reported on.

2529 Communication Circuits

General Comments

This was the last paper of the old specification. It turned out to be harder than its predecessors, but still discriminated as well as they did. Part of the difficulty may have arisen from the themed nature of the questions. Each question probes a candidate's understanding of a section of the specification. If candidates have only a superficial acquaintance with that section, possibly because it does not feature regularly in the exams, they are severely disadvantaged if a whole question is based on that section. Centres need to be aware that any part of the specification may appear in an exam, and to not give each section due attention during the course is to potentially leave their candidates at a disadvantage.

Question 1

This question probed candidates' understanding of TV systems. As ever, weak candidates lost marks throughout by either omitting to provide all details required or not being specific enough. So in the first part, strong candidates would use the terms carrier and signal correctly for different things, whereas weak candidates would apply the term signal indiscriminately and confusingly. Similarly, weak candidates would explain how lines were made of pixels without stating what a pixel was. The block diagram of the superhet caused problems for most candidates, with few realising that the last box had to be the detector.

Question 2

Many candidates were clearly unfamiliar with the operation of a push-pull follower, assuming that it behaved as a driver instead of a follower. This meant that even partially correct sketches of output waveforms were quite rare. Many weak candidates didn't even attempt it. Similarly, too many candidates assumed that crossover distortion was caused by interference of two different signals. However, strong candidates were able to provide good answers to all parts.

Question 3

This question was largely synoptic, causing fewer problems. The vast majority of candidates were able to correctly sketch the transfer characteristic of the inverting amplifier and indicate the direction of the current in the feedback resistor. Many lost marks for the "show that" calculation because they didn't write down formulae or all the steps. Part cii was poorly answered because the question was badly written, although many candidates still earned one mark. Only a minority of candidates could apply the Nyquist criterion to calculate the maximum signal frequency for the DAC, with the majority simply dividing the conversion time into one to obtain their answer (for half marks). Finally, only a minority of strong candidates were able to state that increasing the number of inputs to the DAC would increase its resolution. Most candidates suggested other ways of speeding up the response time, mostly by using smaller resistors or omitting the inverting amplifier (for no marks).

Question 4

As a whole, this question performed well. It was good to see that the majority of candidates could correctly draw an astable. Weak candidates often used f=RC to select their component values. However, the responses to the diode network question suggested that many candidates thought that the output of the oscillator was sinusoidal instead of square. Only a minority of candidates recognised the clamping effect of the diode. The majority of candidates knew the resistance characteristic of the MOSFET, although weak candidates lost a mark by failing to mention the rapid change at the threshold voltage. Although many candidates failed to recognise

the non-inverting amplifier arrangement (despite having being told in the stem of the question!), the application of error-carried-forward meant that they could earn some marks for what they could do. The final part of the question about bias networks discriminated well, with weak candidates often putting the capacitor between the voltage divider and the gate.

Question 5

This question introduced candidates to a complex circuit and required them to explain its operation. This is still a difficult thing for many candidates to do, despite this style of question appearing at least twice on every exam paper of the series. Too often, weak candidates lost marks by not providing enough detail. Many failed to mention that the oscillator provided pulses for the counter to count, that the DAC generated a voltage which increased in steps. However, most candidates could correctly identify the input to the system and correctly connect the flip-flops as a counter (although many left S and R unconnected to anything). Few candidates realised that the counter had to count sixteen pulses for every conversion, so only a minority were able to correctly calculate the frequency of the oscillator. Finally, too many candidates insisted on making A the msb of the counter, consequently leading to errors in the pulse table.

Question 6

It was good to find that most candidates could explain the function of a Schmitt trigger in a serial transfer system, although, as expected, only a minority were able to construct one correctly. The resistor selection proved to be difficult for many candidates. However, the vast majority of candidates could correctly add the reset logic gate to the counter, write down a correct expression for the combination of outputs and draw a logic circuit to implement it. The use of De Morgan's Theorem was familiar for many candidates, but only a few were able to show all the steps in their argument, losing marks accordingly.

Question 7

The final question was about tuned circuits. The calculation performed as expected, with only weak candidates unable to unscramble the algebra in the formula to calculate the value of the capacitor. Although most candidates knew that the tuned circuit's impedance was a maximum at a particular frequency, and that the frequency could be altered by changing the capacitance, too many lost marks by failing to use the terms current and voltage correctly. Too often, they used vague terms such as signal, which earned no credit. Only a minority of candidates mentioned that the aerial was a source of alternating current or that the signal passed on to the next stage was the alternating voltage across the tuned circuit. Many candidates assumed that increasing the resistance in the tuned circuit was good thing, improving selectivity and sensitivity. They probably got confused with the benefits of increasing the input impedance of the next amplifying stage.

2530 Control Circuits

General Comments

As has been the case in previous years, there was a wide range of responses seen by examiners with some candidates showing a high level of understanding and the ability to apply their knowledge whilst others showed little awareness of even the basic concepts.
Overall the standard remains high and many candidates were able to make good attempts at every question with some outstanding responses in a few cases.

Question 1

In keeping with tradition the first question related to the meaning of terms in the context of microprocessor systems. The majority of candidates clearly understood the meaning of the terms ROM and RAM and were familiar with the differences in terms of volatility and storage capability. In contrast there was a lack of clarity between the terms byte and word with many candidates of the opinion that a word contained a fixed number of bits. The difference between Data and Address Bus was also not clear to some candidates and, especially, the role of the Address Bus. Although Hexadecimal was clear to most candidates, Binary Coded Decimal as a group of 4 bits was not.

Question 2

This question linked D-types and tristates in a data transmission system. The operation of the circuit was understood by the majority of candidates. In part (b), the action of the enable in the operation of a tristate was clearly stated and there were many references to the output "floating" although some candidates did not define what value of the enable input made this occur. The action of the D-type in "toggling" its output between 1 and 0 when clocked was also understood by a large number of candidates when answering part (d) although some failed to describe its action "as connected in the circuit" and simply referred to its general operation.

Question 3

A Schmitt Trigger operating a triac to light a lamp under varying lighting conditions was the basis for this question. It was pleasing to note that a large number of candidates could correctly sketch the input / output characteristics of the Schmitt Trigger and many correctly labelled the switching thresholds, although it was not required by the mark scheme. The calculation of the switching thresholds was also achieved by many and a number of methods were used to obtain correct answers to parts (b) (iii) and (iv). Where mistakes were made, it was in determining the correct p.d. across the LDR or resistor, or incorrectly applying the potential divider formula. Identification of the triac in part (c) was straightforward but a number of candidates failed to realise the impact of the diode when calculating the gate voltage of (c) (ii), incorrectly using 13 V as the p.d.. The operation of the triac and its property of firing irrespective of the direction of p.d. across it, was clear from the majority of candidate responses to (d) (i) as was the role of the diode in (d) (ii). Where marks were lost, candidates were not specific enough, dealing in generalities rather than quoting values relating to the question itself. The last section (e) relating to r.m.s. and peak current was not well done with many candidates being unable to quote or use the formula that links the two quantities.

Question 4

This question, based upon the use of a memory device that enabled a tune to be played, was either answered very well or very badly by candidates. There were some excellent responses to part (a), showing a clear understanding of the concepts, although some found determining the

maximum frequency in the tune (part (v)) a challenge. Most candidates recognised the relevance of the R pin in part (b) and that it should not be allowed to "float". Only a few related this to the application itself where it is was essential that the tune repeated itself and was not interrupted.

Question 5

The combined action of a Summing Amplifier and Ramp Generator in maintaining a steady temperature in a box was the basis for this question. The vast majority recognised the Summing Amplifier in (a) (i) but some selected Comparator as the correct response. Some candidates failed to provide the correct response to (a) (ii), often giving the general formula whilst many omitted the minus sign. Many of the responses to (a) (iii) referred to the need for the Summing Amplifier to have a positive output but few linked this to the impact on the Ramp Generator or Transistor if this was not the case. The requirement in (b) (i) to provide a circuit diagram of the Ramp Generator was well met by candidates and many responses to (b) (ii) referred to a "ramping up" to positive saturation but few included the fact that the output would increase linearly. The response for a zero input to the Ramp Generator was more varied with many stating that the output would also be zero. The responses to (c) (i) were also quite varied with many candidates stating that the thermistor resistance decreases as the temperature increases, others going on to select R2 as the correct position and a few realising that voltage A became smaller in value. There were many good responses to (c) (ii) where candidates referred specifically to the circuit and clearly described the impact on the Ramp Generator and heater as the temperature approached the required value.

Question 6

As in the past candidates were asked to provide explanations for sections of microprocessor code and, this year, to write a small amount of code. Many candidates realised that there was a difference between stating the code and explaining its action. For example stating that E6 E0 meant performing an AND function on the accumulator with E0 did not get credit whereas explaining that the action of this was to mask out all the amplitude code did. Based upon the requirement for explanation, many candidates did well in (a), although few realised the significance of C6 1F and C6 01 in maximising the amplitude and frequency code respectively. The code writing section (b) was generally well done and clearly many candidates seemed to have had experience of writing such code. The section on the saw-tooth waveform (c) represented much more of a challenge to candidates but some clearly had an excellent understanding and were able to clearly explain the function, not simply state it. Many recognised that the combined effect of D6 01 and C2 70 as a time delay but only a few that it was required to reduce the frequency value to zero before proceeding

2531 Principal Moderator's Report - Electronics (Project 2)

In this penultimate coursework module, the standard of marking by centres was, in general, very good. The number of centres whose marks fell outside the tolerance allowed by OCR was very few, and most were subjected to small adjustments to bring them in line with the accepted standard. The range of projects undertaken by candidates was huge, as was the range in the number of subsystems attempted by candidates. Some offered projects which had very few subsystems, whilst others attempted large projects which contained a good number of subsystems. Interestingly, of all the candidates who suffered an adjustment in marks, a significant proportion was to those who attempted large projects. It seems that candidates doing large projects tend to omit the testing of ALL subsystems and the subsequent analysis of test results. They also omit to fully test the final circuit and show to what extent the final circuit has met the final circuit specification. The coursework is a process and that process must be adhered to irrespective of the complexity of the project. Some candidates will always want to attempt a large project and if they are capable of doing this, then there is no reason why they should not do it. However, it must be stressed upon them that they must adhere to the process and address all the marking criteria if they are to achieve high marks. The fact of doing a large and complex project does not guarantee high marks.

The following areas of concern have been noted by moderators, and the list is very similar to previous years. However, moderators have also noted an improvement in recent years in these areas of concern. The following criteria have been cited as still causing some concerns:

Criterion A   in the final circuit specification, equipment available should be quoted as this may impose some restrictions in circuit realisation and testing.

Criterion D   there should always be evidence of subsystem testing. Evidence can be Picoscope traces, photos of scope traces with voltage and time-base settings included, photos of LEDs connected to outputs (and inputs), photos of voltmeter readings, etc. Candidates should be trained to produce a testing plan before the actual test is carried out, and also trained to identify how they are to gather the evidence. Simulation packages do not give test results – they help with circuit understanding but must not be submitted as test results.

Criterion E   all test results should be analysed with respect to the subsystem specification. Analysis will usually have some numeric component (what is the gain? the frequency? etc) and this is commonly missed out by many candidates. The final circuit also needs to be fully tested and analysed and, again, this is an area often missed out by candidates. It is possible for a candidate who provides the evidence of a full testing programme but does no analysis of test results whatsoever to score 10/10 for criterion D and 0/8 for criterion E.

Criterion F   (how much of the initial specification has been achieved) also needs evidence to support the mark. This is sometimes omitted by candidates yet they had been awarded 3/4 or 4/4 for this criterion.

Criterion G   the circuit build should be meticulous to be awarded 8/8. Very few circuit builds have been seen which would warrant a mark of 8/8. Components should be flat to the board and in the horizontal/vertical plane. Wires should also be orthogonally arranged, colour coded, and neatly trimmed, subsystems should be placed logically to allow the shortest runs between subsystems. All these considerations need careful planning before the build begins.

Criterion K   accuracy of the report should also include any problems encountered, including all debugging of subsystems undertaken. This is missed out by most candidates but it is an important feature of the report.

Criterion M circuit diagrams should be neatly drawn/constructed; not too small; accurate and integrated circuits should have inputs on the left and outputs on the right (NOT pinout constructions).

Support for this legacy module, and the new coursework modules are available on the OCR website (www.ocr.org.uk). Should anyone have any further questions regarding coursework, do not hesitate to contact the Qualifications Manager at OCR.

Grade Thresholds

Advanced GCE Electronics (3826/7826)
June 2009 Examination Series

Unit Threshold Marks

Unit		Maximum Mark	A	B	C	D	E	U
2526	Raw	120	85	77	69	61	53	0
	UMS	120	96	84	72	60	48	0
2527	Raw	90	61	55	49	44	39	0
	UMS	90	72	63	54	45	36	0
2528	Raw	78	61	54	47	40	33	0
	UMS	90	72	63	54	45	36	0
2529	Raw	120	77	68	59	50	42	0
	UMS	120	96	84	72	60	48	0
2530	Raw	90	62	55	49	43	37	0
	UMS	90	72	63	54	45	36	0
2531	Raw	90	71	64	58	52	46	0
	UMS	90	72	63	54	45	36	0

Specification Aggregation Results

Overall threshold marks in UMS (ie after conversion of raw marks to uniform marks)

	Maximum Mark	A	B	C	D	E	U
3826	300	240	210	180	150	120	0
7826	600	480	420	360	300	240	0

The cumulative percentage of candidates awarded each grade was as follows:

	A	B	C	D	E	U	Total Number of Candidates
3826	29.83	61.4	77.19	93.86	100	100	114
7826	32.47	52.21	67.27	84.68	96.1	100	348

462 candidates aggregated this series

For a description of how UMS marks are calculated see:
http://www.ocr.org.uk/learners/ums_results.html

Statistics are correct at the time of publication.