THIS IS A LEGACY SPECIFICATION

OCR
RECOGNISING ACHIEVEMENT

ADVANCED SUBSIDIARY GCE

ELECTRONICS

Foundations of Electronics

2526

CUP/T72453

Candidates answer on the question paper

OCR Supplied Materials:
None

Other Materials Required:
- Calculator

Monday 18 May 2009
Morning

Duration: 1 hour 30 minutes

2526

Candidate Forename		Candidate Surname	

Centre Number						Candidate Number				

INSTRUCTIONS TO CANDIDATES

- Write your name clearly in capital letters, your Centre Number and Candidate Number in the boxes above.
- Use black ink. Pencil may be used for graphs and diagrams only.
- Read each question carefully and make sure that you know what you have to do before starting your answer.
- Answer **all** the questions.
- Do **not** write in the bar codes.
- Write your answer to each question in the space provided, however additional paper may be used if necessary.

INFORMATION FOR CANDIDATES

- The number of marks is given in brackets **[ ]** at the end of each question or part question.
- The total number of marks for this paper is **120**.
- You may assume, unless otherwise stated, that:
  - **(i)** the p.d. across a forward-biased silicon diode is 0.70V,
  - **(ii)** the power supplies for operational amplifiers are +15V and –15V,
  - **(iii)** the saturation levels for operational amplifiers are +13V and –13V,
  - **(iv)** logic 1 = 5V and logic 0 = 0V.
- The quality of written communication will be assessed in your answers to all questions.
- This document consists of **16** pages. Any blank pages are indicated.

A calculator may be used for this paper

Examiner's Use Only:			
1		9	
2		QWC	
3			
4			
5			
6			
7			
8			
Total			

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1 **(a)** Truth tables are filled with the symbols 1 and 0.

Explain what these symbols mean in the context of logic gates.

.....

.....

..... **[2]**

(b) Complete this truth table for a NOR gate.

B	A	Q
0	0	
0	1	
1	0	
1	1	

[2]

(c) The circuit of Fig. 1.1 has the behaviour of an EOR gate.

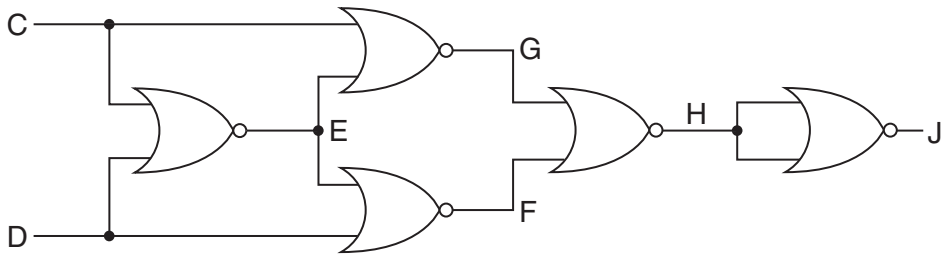

Fig. 1.1

Complete the truth table for this circuit.

C	D	E	F	G	H	J
1	1					
0	0					
0	1					
1	0					

[5]

(d) Describe the behaviour of an EOR gate in words.

.....

.....

..... **[2]**

2 Fig. 2.1 shows a circuit which switches on a motor when the light level gets too low.

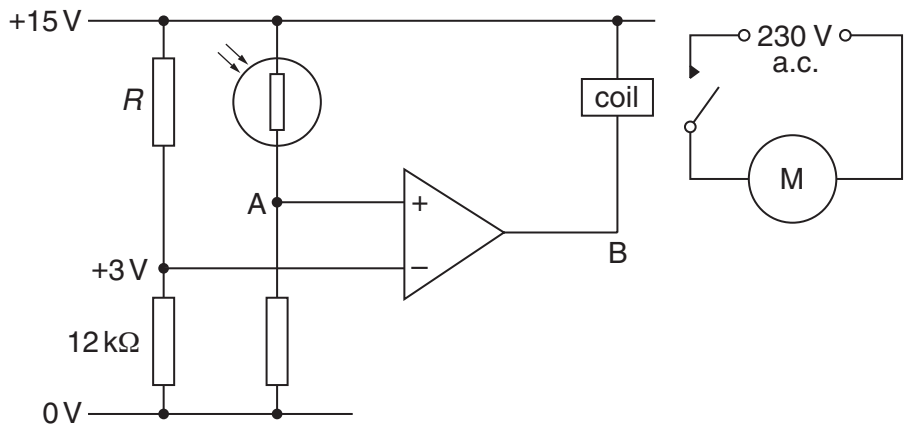

Fig. 2.1

(a) (i) Mark with an X the component which senses the light level. **[1]**

(ii) State the name of this component.

..... **[1]**

(b) A diode should be inserted into the circuit to protect the op-amp from voltage surges across the relay coil.

Add the diode to the circuit of Fig. 2.1. **[2]**

(c) State a value for the resistor *R* which will set the inverting input to +3 V.

Justify your choice.

R = ... kΩ **[3]**

(d) Explain why the motor comes on when the light level gets too low.

.....

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..... **[5]**

3 Fig. 3.1 shows a D-type flip-flop in a circuit.

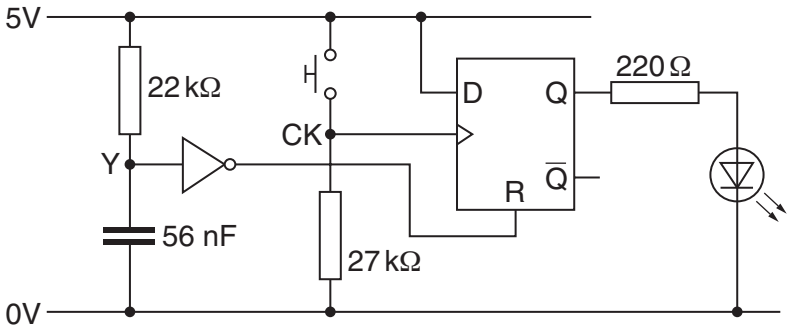

Fig. 3.1

(a) The graph of Fig. 3.2 shows how the voltage at Y changes when the 5V supply is first connected.

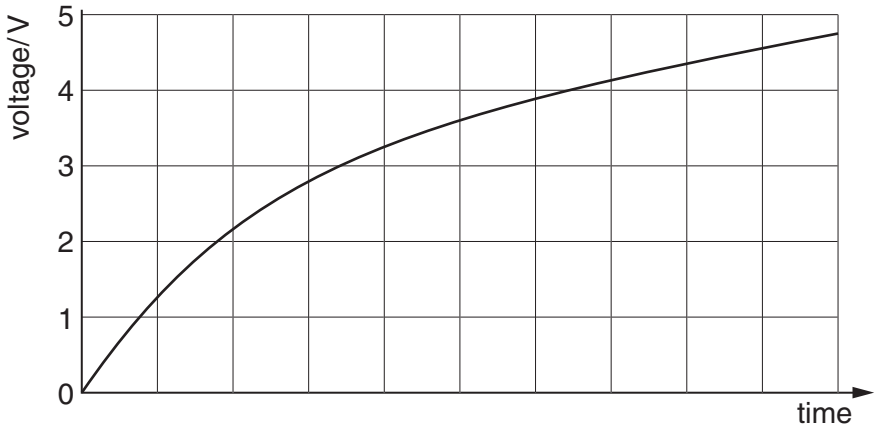

Fig. 3.2

The table gives data for the NOT gate.

input voltage	output voltage
below 2.0V	4.8V
above 2.0V	0.2V

Use the data to draw on Fig. 3.2 to show how the voltage at R changes with time. **[3]**

(b) The RC network connected to Y holds R high for a short time when the 5 V power supply is first connected to the circuit.

(i) Show that the time constant of the RC network is about 1 ms.

[3]

(ii) Calculate how long R remains high after the power supply has been connected.

time = ...s **[2]**

(c) **(i)** Describe and explain what happens to the LED when the circuit of Fig. 3.1 is first connected to the power supply, with the switch open.

.....

.....

..... **[2]**

(ii) Describe and explain what happens to the LED when the switch is now pressed **and** released.

.....

.....

.....

.....

.....

..... **[4]**

4 The graph of Fig. 4.1 shows how the output voltage of an amplifier depends on its input voltage.

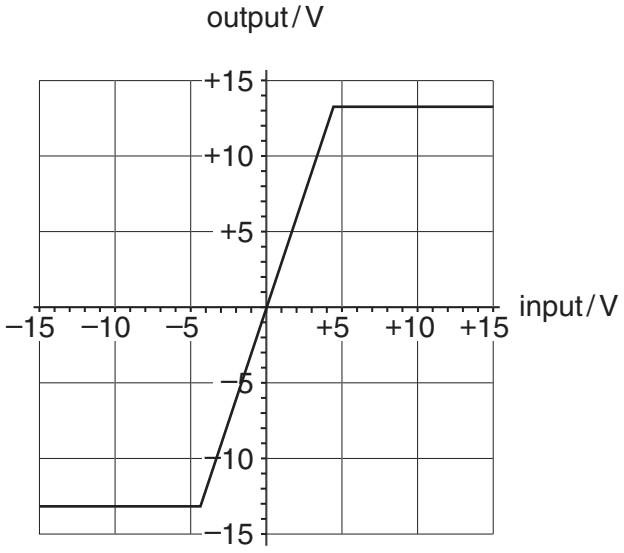

Fig. 4.1

(a) Use information from the graph to show that

(i) the sign of the gain is positive,

.....

.....

..... **[1]**

(ii) the value of the gain is about 3.

[2]

(b) Fig. 4.2 is a voltage-time graph for a low frequency test signal at the input of the amplifier with the characteristic shown in Fig. 4.1.

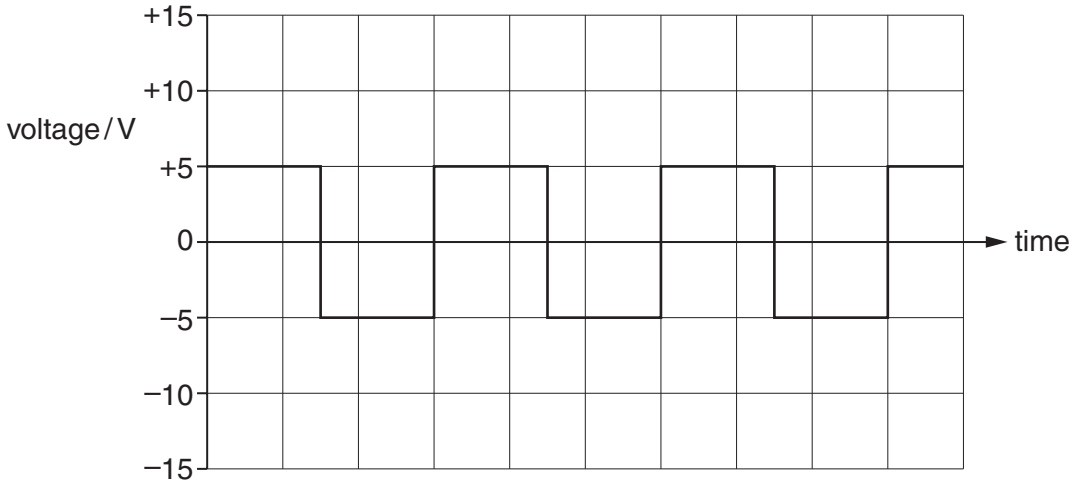

Fig. 4.2

Draw on Fig. 4.2 to show the signal at the output of the amplifier. **[2]**

(c) An op-amp can be converted into a non-inverting amplifier by connecting resistors to it.

Draw the circuit diagram for a non-inverting amplifier which has a gain of +3.

Label the input and the output.

Show all component values.

[6]

5 The circuit of Fig. 5.1 operates from a 9 V battery.
It provides a stabilised 5 V across the load.

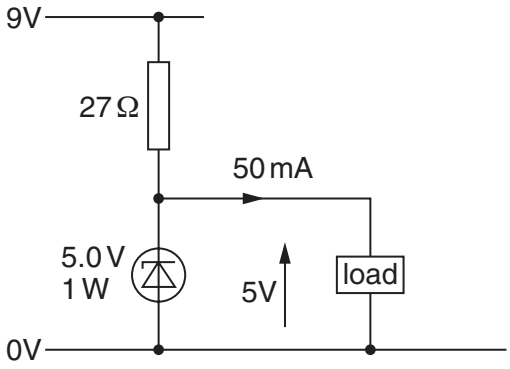

Fig. 5.1

(a) Draw on Fig. 5.1 to show how a voltmeter should be connected to measure the voltage of the 9 V battery. **[2]**

(b) The current in the load is 50 mA.

(i) Calculate the resistance of the load.

resistance = ...Ω **[3]**

(ii) Calculate the power delivered to the load.

power = ... W **[3]**

(c) The zener diode is rated at 5.0 V, 1 W.

(i) Show that the current in the 27 Ω resistor is about 150 mA.

[3]

(ii) State the current in the zener diode while the load is connected.

current = ... A **[1]**

(iii) Show that the zener diode will not overheat while the load is connected.

[3]

(d) The zener diode of Fig. 5.1 is reverse biased. Describe how the current in a reverse biased zener diode depends on the voltage across it.

.....

.....

.....

..... **[3]**

6 A simple power supply produces 9 V d.c. from a 120 V, 60 Hz mains supply.
It uses the following components.

capacitor **four diodes** **transformer**

(a) Draw a circuit diagram below to show how these components should be connected.

Include a load and the mains supply in your diagram.

[6]

(b) Explain why the voltage at the secondary of the transformer needs to be about 7.5 V rms.

[3]

(c) The frequency of the mains supply is 60 Hz.

Calculate the period of the ripple voltage across the load.

period = ...s **[3]**

(d) The load has a resistance of 33 Ω.

Calculate the ripple voltage for a 2200 μF capacitor.

ripple voltage = ... V **[3]**

7 Fig. 7.1 shows an incomplete circuit with an inverting amplifier based on an op-amp.

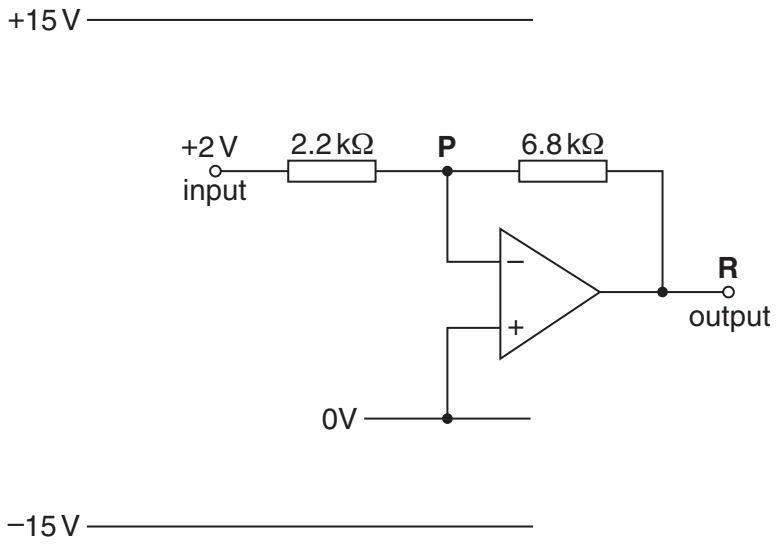

Fig. 7.1

The input is to be held at +2V by a potentiometer connected to the supply rails at –15V and +15V.

(a) Draw the potentiometer arrangement on Fig. 7.1. **[1]**

(b) State the voltage at P when the op-amp is not saturated.

voltage = ... V **[1]**

(c) Calculate the voltage at the output R.

voltage = ... V **[3]**

8 **(a)** Complete this truth table for a NAND gate. A and B are the inputs.

B	A	Q

[3]

(b) **(i)** Describe the behaviour of a two-input **OR** gate in words.

.....

.....

..... **[2]**

(ii) Show how an OR gate can be constructed from a number of two-input NAND gates. Use a truth table with a column for the output of each gate to justify your arrangement of gates.

[6]

(c) Fig. 8.1 shows a bistable made from NAND gates.

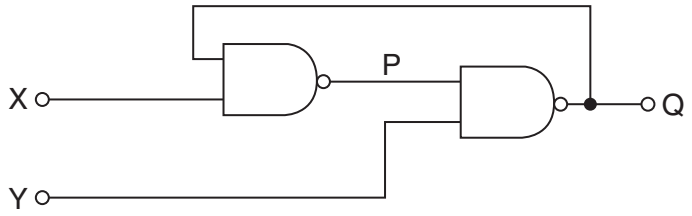

Fig. 8.1

(i) The inputs X and Y are initially high.

Explain why this allows Q to be either high or low.

.....

.....

..... **[2]**

(ii) Explain why pulling only the input X low forces the output Q low.

.....

.....

..... **[2]**

(iii) Complete the timing diagram of Fig. 8.2. Q is initially logic 0.

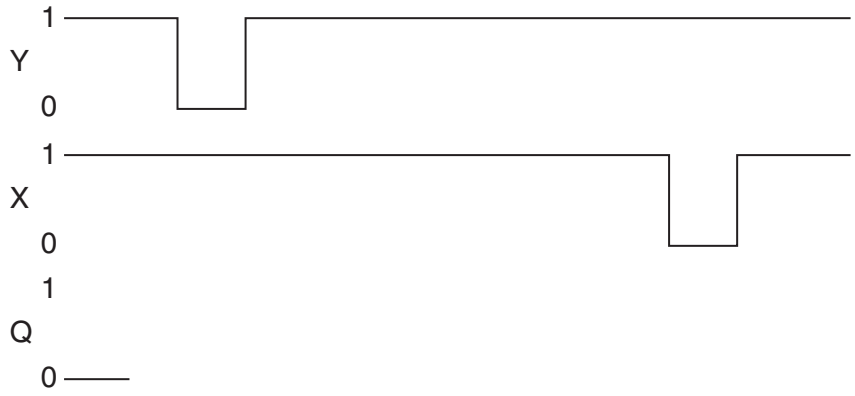

Fig. 8.2

[3]

9 The circuit of Fig. 9.1 includes three resistors.

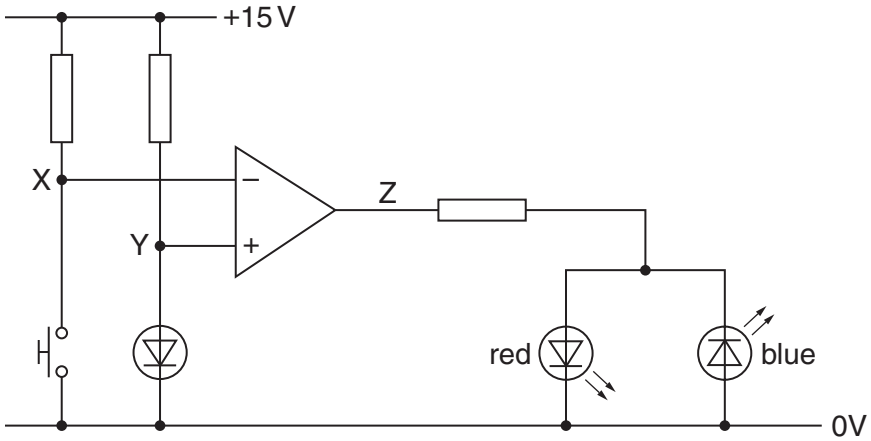

Fig. 9.1

(a) (i) Circle the resistor which limits the current in the LEDs. **[1]**

(ii) On the axes of Fig. 9.2, sketch a graph to show how the current in the **red** LED depends on the voltage across it when it is forward biased.

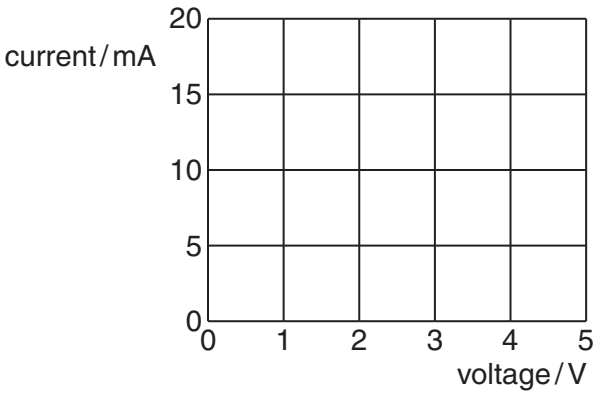

Fig. 9.2

[3]

(b) When the blue LED is glowing, the current in it is 12 mA and the voltage across it is 3.2 V.

(i) Calculate the voltage drop across the current-limiting resistor when the blue LED is glowing.

voltage drop = ... V **[2]**

(ii) Calculate a suitable value for the current-limiting resistor.

resistance = ...Ω **[3]**

(c) Explain why the **blue** LED stops glowing each time that the switch is pressed.

.....

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..... **[4]**

Quality of written communication **[3]**

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