OCR
RECOGNISING ACHIEVEMENT

ADVANCED SUBSIDIARY GCE **2526**

ELECTRONICS

Foundations of Electronics

FRIDAY 16 MAY 2008

Morning

Time: 1 hour 30 minutes

Candidates answer on the question paper

Additional materials (enclosed): None

Additional materials (required):
Calculator

CUP/T44954

Candidate Forename		Candidate Surname	
Centre Number		Candidate Number	

INSTRUCTIONS TO CANDIDATES

- Write your name in capital letters, your Centre Number and Candidate Number in the boxes above.
- Use blue or black ink. Pencil may be used for graphs and diagrams only.
- Read each question carefully and make sure that you know what you have to do before starting your answer.
- Answer **all** the questions.
- Do **not** write in the bar codes.
- Write your answer to each question in the space provided.

INFORMATION FOR CANDIDATES

- The number of marks for each question is given in brackets [ ] at the end of each question or part question.
- The total number of marks for this paper is **120**.
- You may assume, unless otherwise stated, that:
  - **(i)** the p.d. across a forward-biased silicon diode is 0.70V,
  - **(ii)** the power supplies for operational amplifiers are +15V and –15V,
  - **(iii)** the saturation levels for operational amplifiers are +13V and –13V,
  - **(iv)** logic 1 = 5V and logic 0 = 0V.
- The quality of written communication will be assessed in your answers to all questions.

FOR EXAMINER'S USE	
1	
2	
3	
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5	
6	
7	
8	
QWC	
TOTAL	

This document consists of **15** printed pages and **1** blank page.

1 **(a)** Complete the truth table for an EXCLUSIVE-OR gate. Use only 1 and 0.

B	**A**	**Q**

[3]

(b) The circuit diagram of Fig. 1.1 shows how an EXCLUSIVE-OR gate can be assembled from NOT, AND and OR gates.

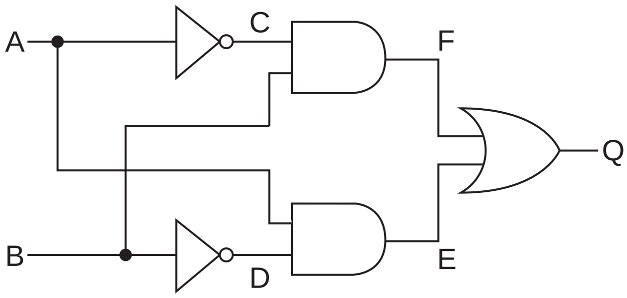

Fig. 1.1

Complete the truth table.

A	**B**	**C**	**D**	**E**	**F**	**Q**
0	0					
1	0					
1	1					
0	1					

[4]

(c) Show how an EXCLUSIVE-OR gate can be assembled from a number of NOR gates.

[5]

2 The circuit of Fig. 2.1 contains a capacitor in parallel with a resistor.

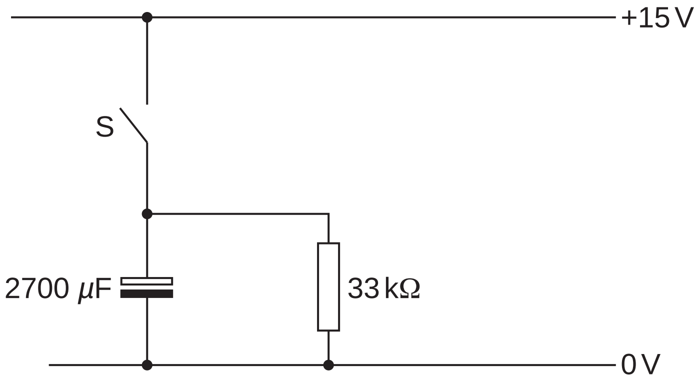

Fig. 2.1

(a) The switch S is closed.
Explain why the voltage across the resistor suddenly rises to 15 V.

....

....

....[2]

(b) On Fig. 2.1, show how a voltmeter should be connected to measure the voltage across the resistor. [2]

(c) When the switch is opened, the voltage across the resistor drops slowly to 0 V.

(i) Calculate the time constant of the circuit when the switch is open.

time constant = ... s [3]

(ii) Explain why the voltage drops slowly.

....

....

....

....[3]

(iii) Calculate the time delay between the opening of the switch and the reading of the voltmeter becoming 2.0 V.

time delay = ... s [2]

3 The circuit of Fig. 3.1 uses an LDR to control an LED.

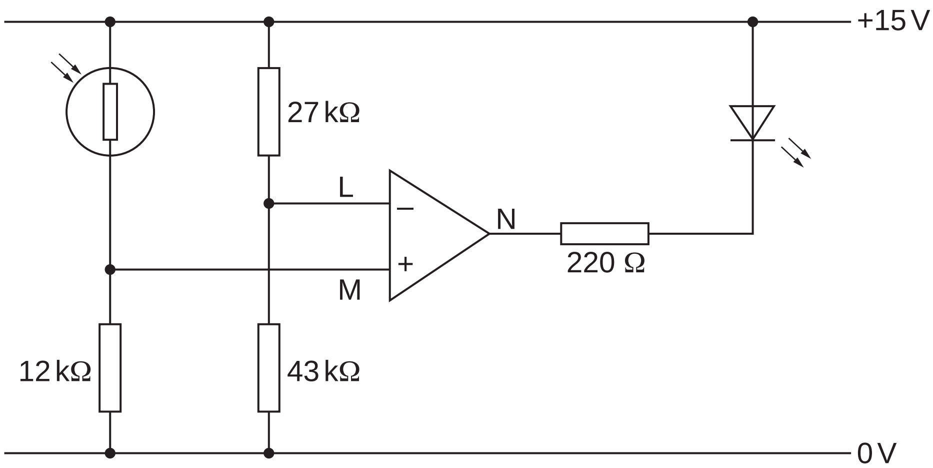

Fig. 3.1

(a) **(i)** Label the LDR [1]

(ii) Describe the electrical properties of an LDR.

....

....

....

....[3]

(iii) Explain why the circuit of Fig. 3.1 needs a resistor in series with the LDR.

....

....

....[2]

(b) The pair of resistors connected to L keep it a steady voltage.

(i) Calculate the total resistance of these resistors.

resistance = ... kΩ [1]

(ii) Calculate, in μA, the current in the resistors.

current = ... μA [3]

(iii) Show that the voltage at L is about 9 V.

voltage = ... V [2]

(c) Explain why the LED glows brightly whenever the voltage at M goes below about +9 V.

....

....

....

....

....

....

....[5]

4 The circuit of Fig. 4.1 contains a NOR gate bistable.

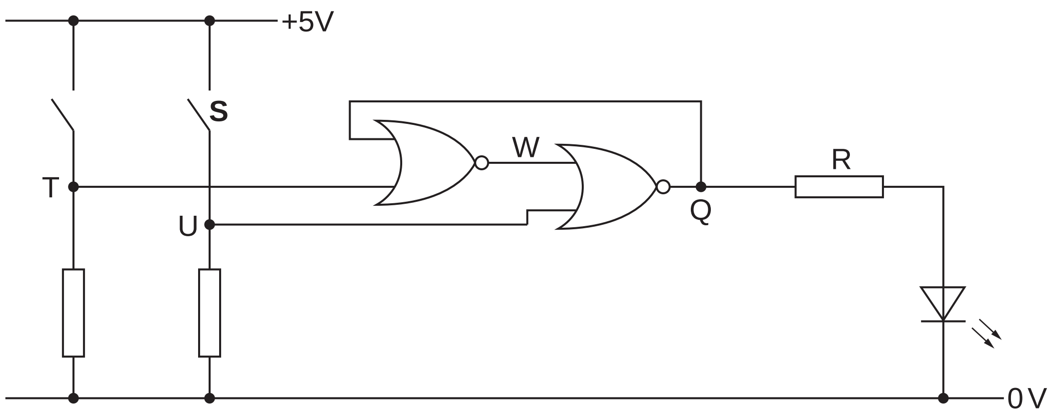

Fig. 4.1

(a) Complete the truth table for a NOR gate.

W	**U**	**Q**
0	0	
0	1	
1	0	
1	1	

[2]

(b) Explain why the LED stops glowing when the switch **S** is closed.

....

....

....

....[3]

(c) Describe and explain what happens to the LED when the switch **S** is opened again.

....

....

....

....

....[4]

(d) When the LED glows, the voltage across it is 1.8 V and it has a power of 5 mW.

(i) Show that the current in the glowing LED is about 3 mA.

[3]

(ii) Calculate the resistance of resistor R.

resistance = ... Ω [3]

(iii) By describing the electrical properties of an LED, explain why the series resistor is necessary.

....

....

....

....[3]

5 The circuit of Fig. 5.1 produces a steady 5V supply from the a.c. mains supply.

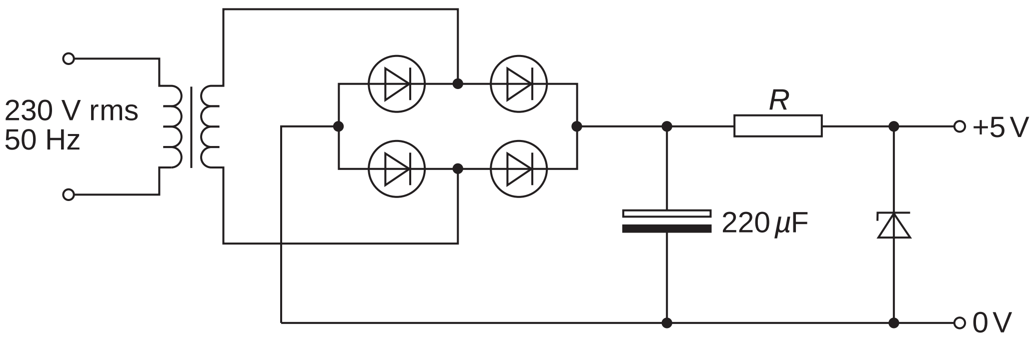

Fig. 5.1

(a) Complete the block diagram of Fig. 5.2 for the circuit of Fig. 5.1.

Choose words from the list.

converter **inverter** **rectifier** **smoother** **stabiliser** **transformer**

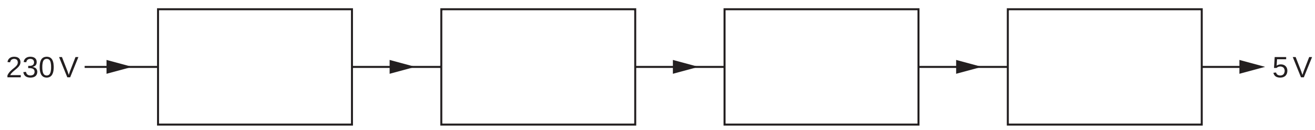

Fig. 5.2

[4]

(b) The mains supply has a frequency of 50 Hz.

(i) Explain why this means that the capacitor is charged up at intervals of 10 ms.

....

....

....

....

....[4]

(ii) Draw on Fig. 5.1 to show how an oscilloscope should be connected to measure the voltage across the capacitor. [2]

(iii) The voltage across the capacitor has a peak voltage of 9.0V and a ripple of 2.0V.

Draw on Fig. 5.3 to show this voltage on the screen of the oscilloscope.

The timebase is set at 5ms / division and the vertical amplifier is at 5V / division.

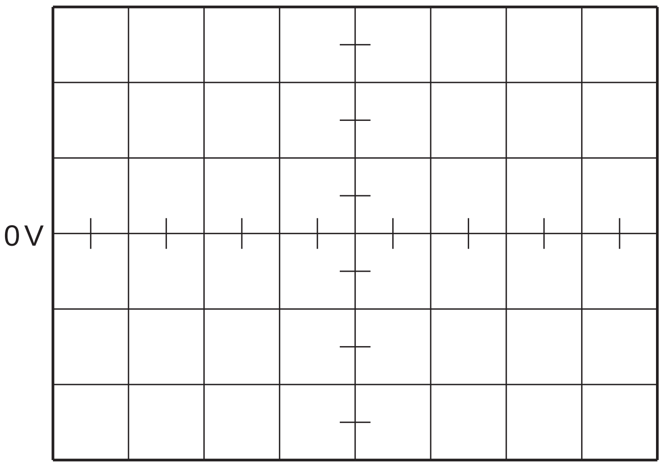

Fig. 5.3

[4]

(c) The circuit of Fig. 5.1 contains a zener diode.

(i) Put a ring around the zener diode. [1]

(ii) On the axes of Fig. 5.4 draw the current-voltage characteristic of the zener diode.

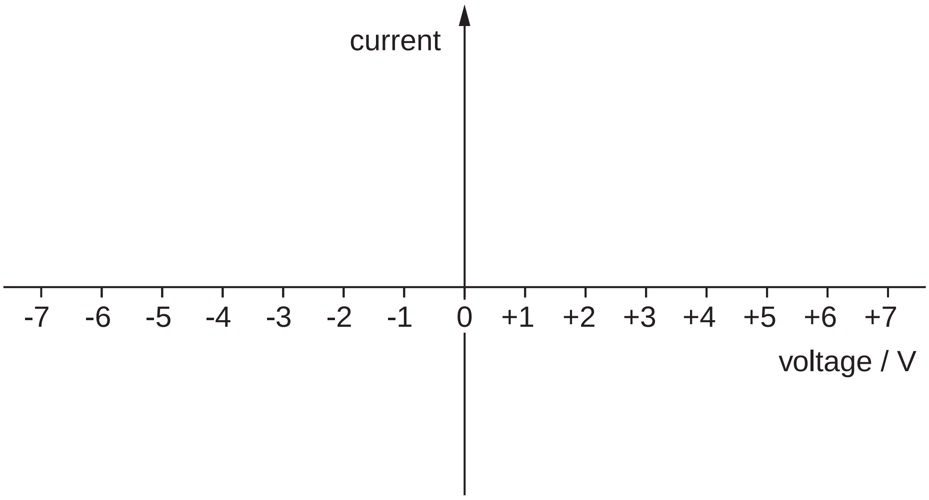

Fig. 5.4

[3]

6 The circuit of Fig. 6.1 is a low-temperature alarm for a refrigerator.

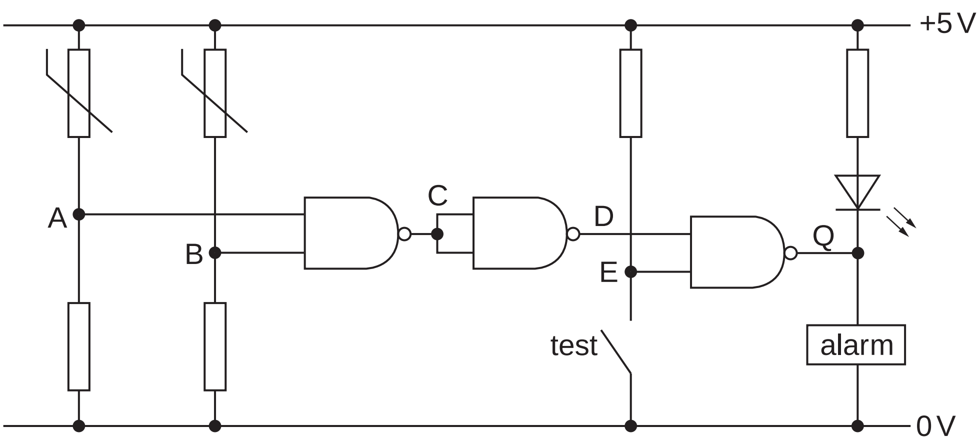

Fig. 6.1

(a) The circuit contains NAND gates.

(i) Describe the behaviour of a NAND gate.

....

....

....[2]

(ii) Complete the truth table for the circuit of Fig. 6.1.

E	**B**	**A**	**C**	**D**	**Q**
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

[5]

(b) The circuit contains a pair of identical thermistors. The graph of Fig. 6.2 shows how the resistance of a thermistor varies with temperature.

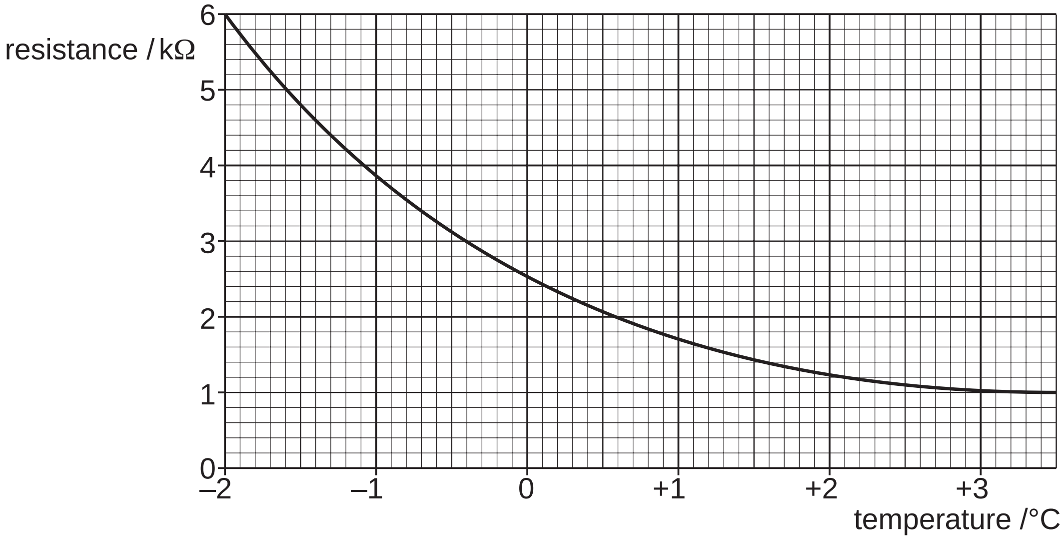

Fig. 6.2

(i) Explain why the voltage at A **rises** as the temperature of the thermistor rises.

....

....

....

....[3]

(ii) The voltage at A is +2V when the temperature of the thermistor is 0 °C.

Calculate the resistance of the resistor in series with the thermistor.

resistance = ... kΩ [4]

(c) The circuit of Fig. 6.1 contains a test switch.

Explain what happens when the switch is closed.

....

....

....

....[4]

7 The circuit of Fig. 7.1 shows an inverting amplifier.

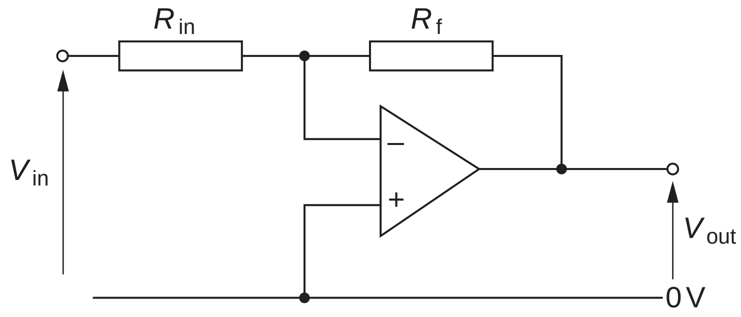

Fig. 7.1

(a) **(i)** State the voltage of the inverting input of the op-amp.

Give a reason for your answer.

voltage = ... V

....

....[2]

(ii) Here are some expressions for the current I in the resistor R_{in}.

$$I = (V_{in} - 0) \times R_{in} \qquad I = \frac{V_{in} - 0}{R_{in}} \qquad I = \frac{R_{in}}{V_{in} - 0}$$

Put a ring around the correct expression. [1]

(iii) Write down a different expression for the current I in the resistor R_f.

[2]

(iv) By equating the two expressions for I, show that the voltage gain G of the circuit is given by

$$G = -\frac{R_f}{R_{in}}$$

[2]

(b) On the graph of Fig. 7.2, sketch the transfer characteristic for the amplifier of Fig. 7.1 when R_{in} = 4.7 kΩ and R_f = 8.2 kΩ.

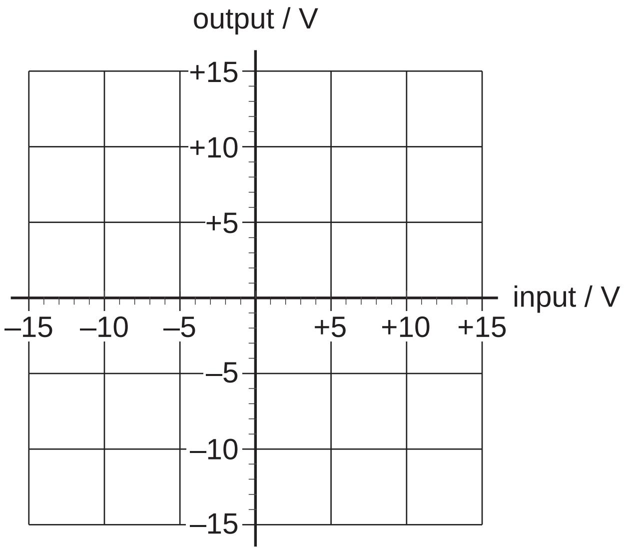

Fig. 7.2

[4]

(c) **(i)** On Fig. 7.3, show how an op-amp can be connected so that it has a voltage gain of +1 and an input resistance of 100 kΩ.

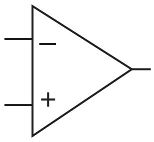

Fig. 7.3

[3]

(ii) An op-amp with a voltage gain of +1 is sometimes called a power amplifier.

Explain why the circuit of Fig. 7.3 is a power amplifier.

....

....

....[2]

8 The circuit of Fig. 8.1 contains a D-type flip-flop.

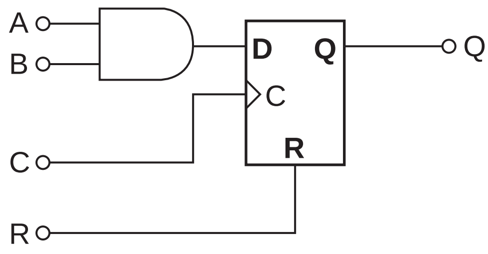

Fig. 8.1

(a) State the signals required at A and B to make D go high.

....

....[1]

(b) The timing diagram of Fig. 8.2 shows the signals at the flip-flop inputs R, C and D.

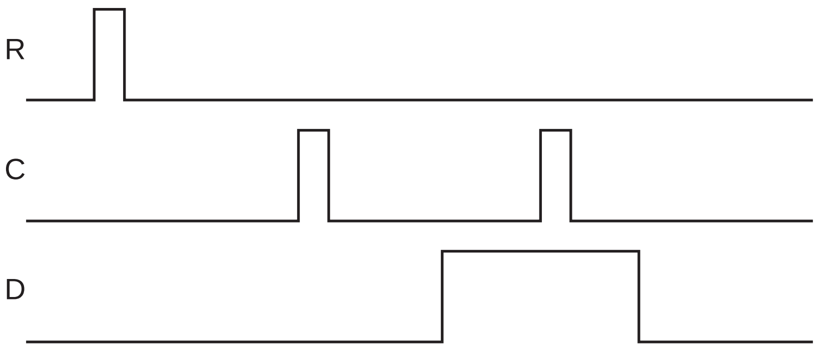

Fig. 8.2

The sentences below describe these signals and their effect on the D-type flip-flop.

A	Q goes low.
B	D starts off low.
C	The signal at A goes low.
D	The signals at A and B both go high.
E	A clock pulse at C leaves Q unchanged.
F	A clock pulse at C changes the state of Q.
G	A short pulse is applied to the reset terminal.

Put letters in the boxes below to show the correct order.

The first one has been done for you.

B						

[5]

Quality of Written Communication [3]

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