OCR
RECOGNISING ACHIEVEMENT

ADVANCED SUBSIDIARY GCE **2527**

ELECTRONICS

Signal Processing Circuits

FRIDAY 16 MAY 2008

Morning

Time: 1 hour 15 minutes

Candidates answer on the question paper
Additional materials (enclosed): None

Additional materials (required):
Calculator

CUP/T44943

Candidate Forename		Candidate Surname	
Centre Number		Candidate Number	

INSTRUCTIONS TO CANDIDATES

- Write your name in capital letters, your Centre Number and Candidate Number in the boxes above.
- Use blue or black ink. Pencil may be used for graphs and diagrams only.
- Read each question carefully and make sure that you know what you have to do before starting your answer.
- Answer **all** the questions.
- Do **not** write in the bar codes.
- Write your answer to each question in the space provided.

INFORMATION FOR CANDIDATES

- The number of marks for each question is given in brackets [ ] at the end of each question or part question.
- The total number of marks for this paper is **90**.
- You may assume, unless otherwise stated, that:
  - **(i)** the p.d. across a forward-biased silicon diode is 0.70V,
  - **(ii)** the base-emitter p.d. for a conducting silicon transistor is 0.70V,
  - **(iii)** the power supplies for operational amplifiers are +15V and –15V,
  - **(iv)** the saturation levels for operational amplifiers are +13V and –13V,
  - **(v)** logic 1 = 5V and logic 0 = 0V.
- The quality of written communication will be assessed in your answers to all questions.

FOR EXAMINER'S USE	
1	
2	
3	
4	
5	
6	
7	
QWC	
TOTAL	

This document consists of **14** printed pages and **2** blank pages.

1 **(a)** Fig. 1.1 shows the symbol for a logic gate with inputs A and B and output Q.

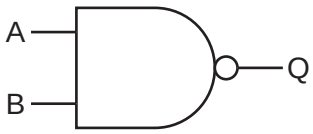


Fig. 1.1

(i) State the name of the logic gate in Fig. 1.1. .....[1]

(ii) Complete the truth table for the logic gate in Fig. 1.1.

A	B	Q

[3]

(iii) Write down a Boolean expression for the output Q in terms of the inputs A and B.

Q = ...[1]

(b) Fig. 1.2 shows a circuit containing three of the gates of Fig. 1.1

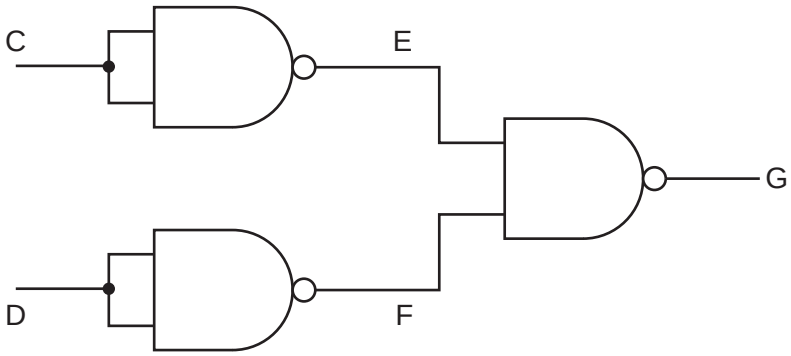


Fig. 1.2

(i) Write down a Boolean expression for E in terms of the input C.

E = ...[1]

(ii) Write down a Boolean expression for F in terms of the input D.

F = ...[1]

(iii) Using your answers to **(b)(i)** and **(b)(ii)** write down a Boolean expression for the output G in terms of the inputs C and D.

G = ...[1]

(iv) State the rule of Boolean algebra which allows your expression for G to be changed to the expression for another type of logic gate.

rule = ...[1]

(v) State the logic gate which will give the same output as the circuit in Fig. 1.2.

logic gate = ...[1]

(c) Fig. 1.3 shows a circuit containing five of the gates of Fig. 1.1

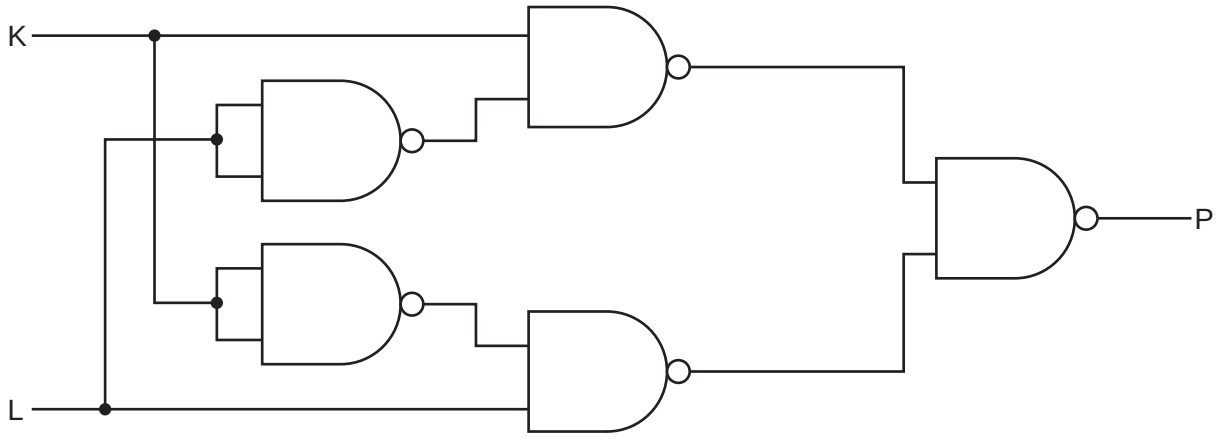


Fig. 1.3

(i) Write down a Boolean expression for the output P in terms of the inputs K and L

P = ...[2]

(ii) State the logic gate which will achieve the same result as Fig. 1.3.

logic gate = ...[1]

(iii) In the space below, draw the symbol for this logic gate.

[1]

2 **(a)** A logic circuit is defined by the Boolean expression. $H = J + \overline{K}$

Complete the truth table for this circuit.

J	K	H
0	0	
0	1	
1	0	
1	1	

[1]

(b) A logic circuit has the following truth table.

R	S	T
0	0	1
0	1	0
1	0	0
1	1	0

Circle **one** of the Boolean expressions below which correctly describes this truth table.

$T = R \cdot S$ $T = R + S$ $T = \overline{R \cdot S}$ $\overline{T} = R + S$

[1]

(c) A logic circuit is defined by the Boolean expression $Z = \overline{\overline{X} + Y}$

Complete the truth table for this circuit.

X	Y	Z
0	0	
0	1	
1	0	
1	1	

[2]

3 Fig. 3.1 shows a diagram of a solar cell controlling a dc motor through an amplifier.
The input voltage to the amplifier is measured on voltmeter V_1 while the voltage supplied to the motor is measured on voltmeter V_2.

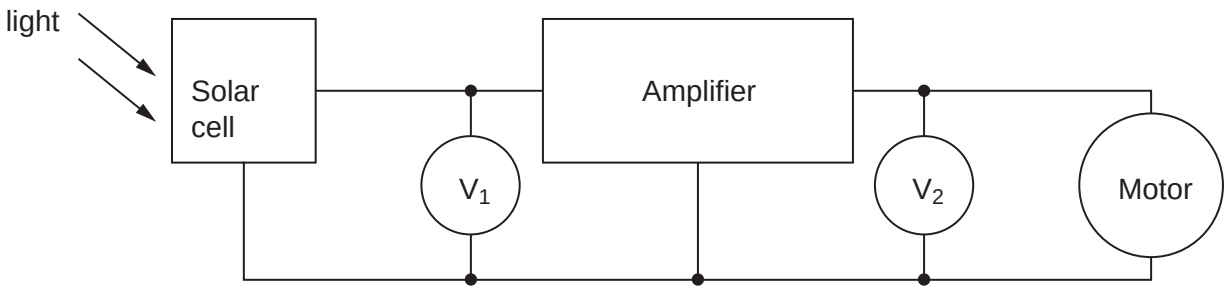


Fig. 3.1

Under certain light conditions, the voltmeter V_1 reads 0.4V while the voltmeter V_2 reads 8V and the power supplied to the motor is 24W.

(a) (i) Calculate the current output from the amplifier.

current output = ... A [2]

(ii) The amplifier has an output resistance of 4Ω.
Show that the amplifier is producing a voltage of 20V in order to achieve 8V across the motor.

[3]

(iii) Calculate the voltage gain of the amplifier.

voltage gain = ...[2]

(b) (i) The amplifier has an input resistance of 1.6kΩ.
Calculate the current input to the amplifier under the light conditions of part (a).

current input = ... A [2]

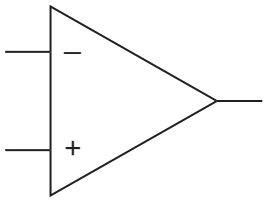
(ii) When the amplifier is disconnected under the same light conditions, the voltmeter V_1 reads 1.9V.
Calculate the internal resistance of the solar cell.

internal resistance = ...Ω [3]

4 **(a)** Using Fig. 4.1, complete the circuit for a **bass cut filter** with the following characteristics:

- Minimum input resistance 2.7 kΩ
- High frequency gain –320
- Break frequency 320 Hz

Give component values and show your working for all calculations.

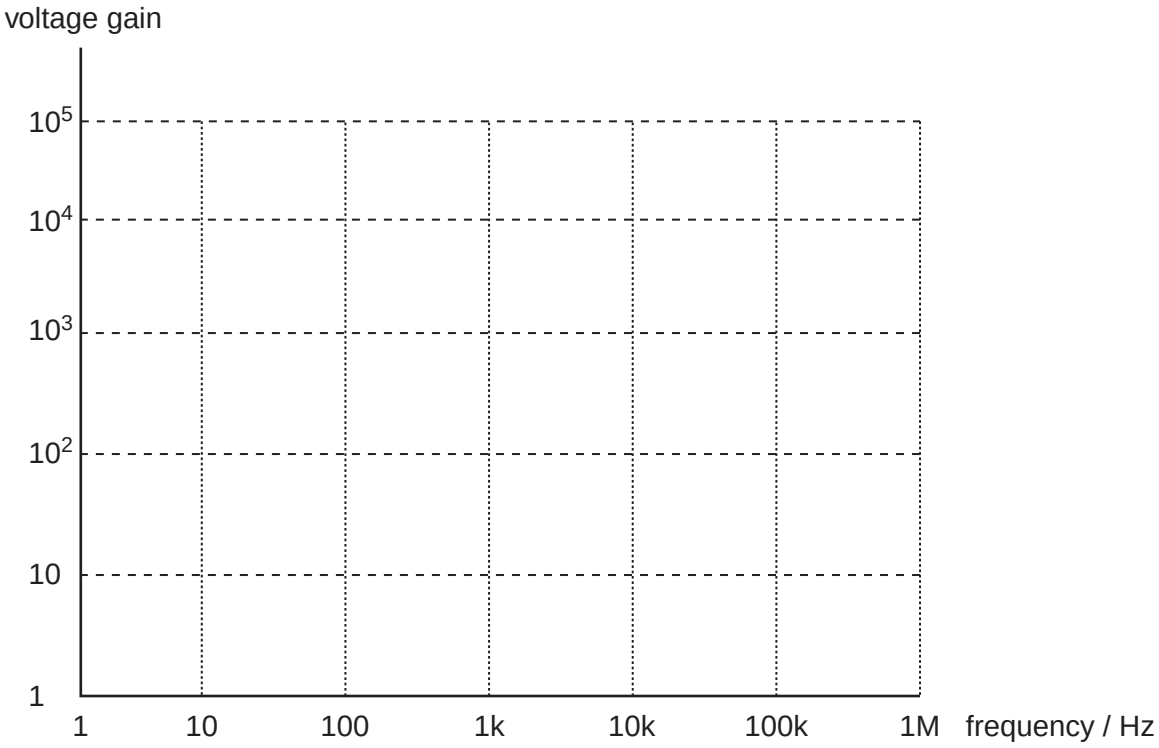


0V

[9]

Fig. 4.1

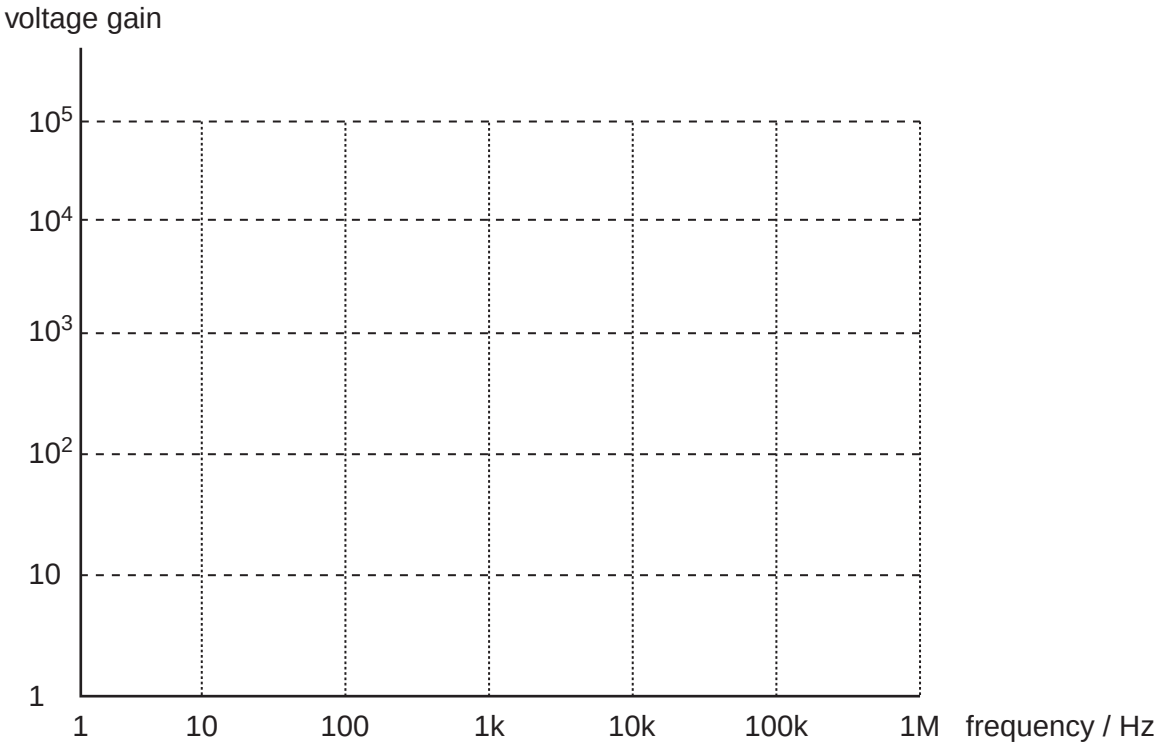
(b) On the axes of Fig. 4.2, draw the frequency response of your bass cut filter assuming the op-amp being used is ideal.



[4]

Fig. 4.2

(c) On the axes of Fig. 4.3, draw the frequency response of your bass cut filter if the op-amp being used is an 081 type.



[3]

Fig. 4.3

5 Fig. 5.1 shows part of a circuit built around an op-amp. The op-amp is driving a low power dc motor.

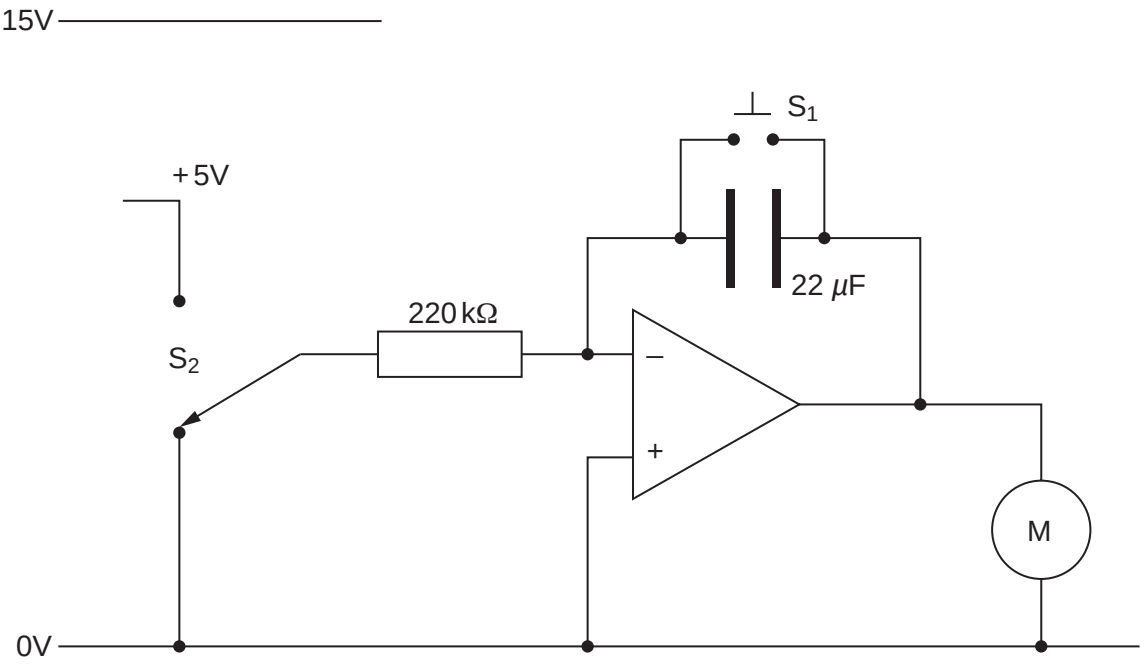


Fig. 5.1

(a) State the name of the op-amp circuit of Fig. 5.1.

.....[1]

(b) When the circuit is first powered up, the switch S_2 rests in the 0V position and the capacitor is uncharged. The switch S_2 is then thrown to the +5V position and left there for 20 seconds.

(i) Show that the op-amp output voltage initially falls at a rate of about $1\,V\,s^{-1}$.

[3]

(ii) Explain how the motor responds during the 20 seconds.

.....

.....

.....

.....

.....[4]

(c) At the end of the 20 seconds the switch S_2 is thrown back to 0V.
Explain how the motor responds.

.....

.....

.....[2]

(d) At the end of a further 20 seconds, the switch S_1 is given a brief push.
Explain how the motor responds.

.....

.....

.....[2]

(e) The op-amp is an 081 type.
Explain, with the aid of a calculation, why it is necessary that the motor power does not exceed about 130 mW.

.....

.....[2]

(f) Fig. 5.1 is missing a potential divider which will produce the +5V input from the +15V supply line.

(i) Draw on Fig. 5.1 a potential divider across the given supply lines. [1]

(ii) Choose resistor values which will produce the +5V input from the +15V supply line.
Your values should take account of the loading effect of the circuit shown and you should explain why this is necessary.

.....

.....

.....[3]

6 Fig. 6.1 shows the circuit of a summing amplifier.

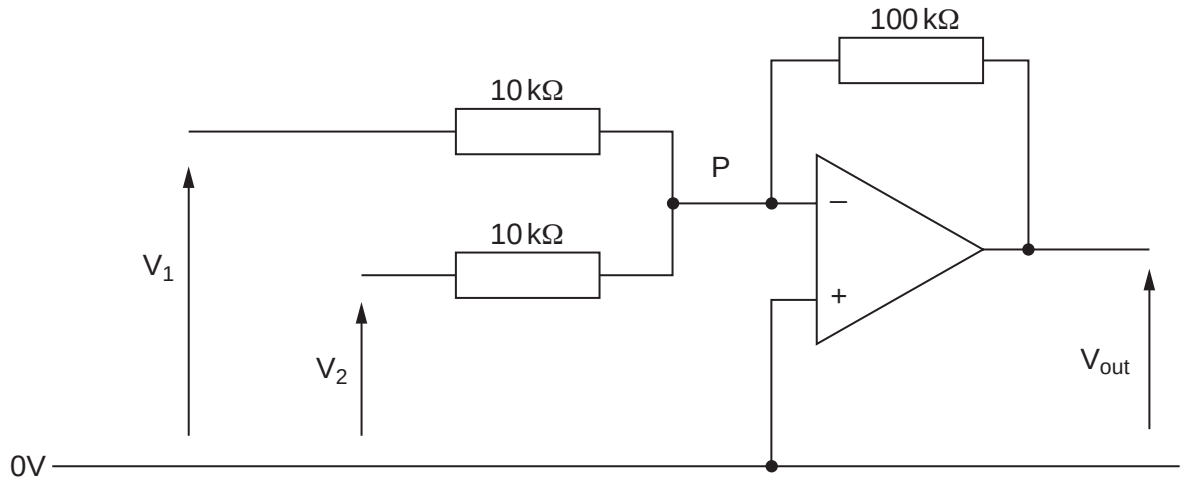


Fig. 6.1

(a) If the output is not *saturated*, the point P in the circuit is known as a *virtual earth*. Explain the meaning of the terms below.

Saturated .....

.....

Virtual Earth .....

.....

.....[3]

(b) When V_1 = + 0.5V and V_2 = + 0.2V,

(i) explain, with the aid of a calculation, why the current in the feedback resistor is 70 µA.

.....

.....

.....[4]

(ii) show that the output voltage is –7V.

[2]

(c) Show that the behaviour of the circuit of Fig. 6.1 is governed by the equation.

$$V_{out} = -10 (V_1 + V_2)$$

[3]

(d) Fig. 6.2 shows the summing amplifier of Fig. 6.1 being used to compare the terminal voltages of two batteries using a simple voltmeter which can only read from 0 to 15V in 1V intervals.

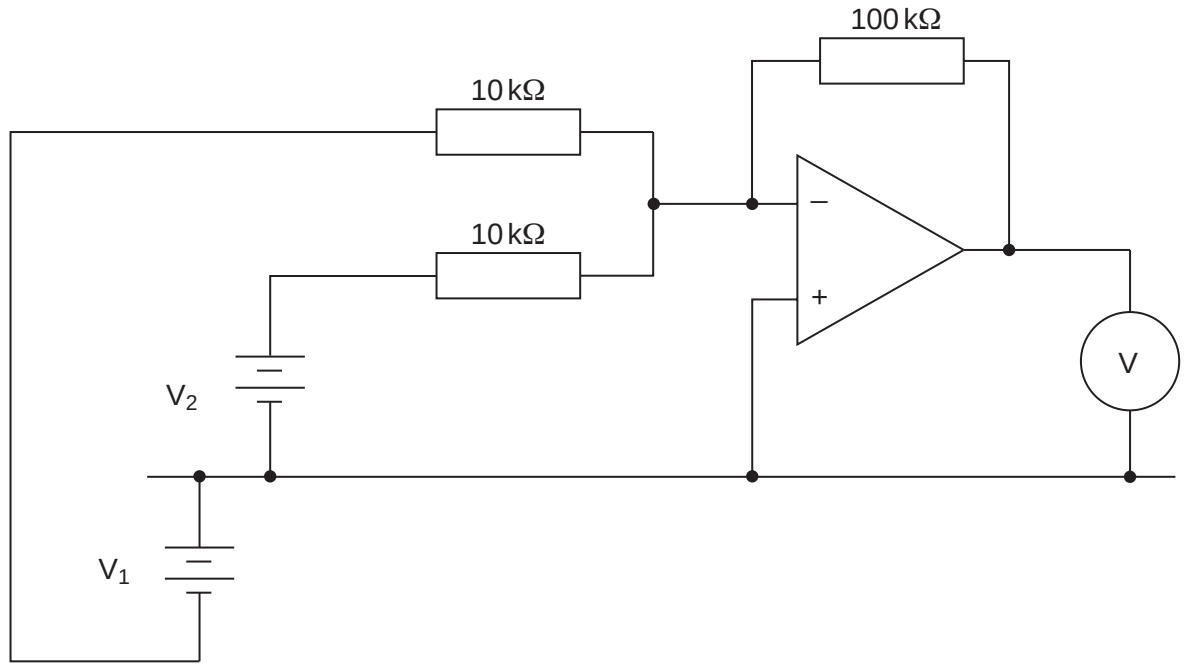


Fig. 6.2

Explain how the circuit works.

.....

.....

.....

.....

.....[3]

7 Fig. 7.1 shows the inputs and outputs of a board containing a quiz referee circuit which operates as follows:

- When the referee switch is pushed any LED which happens to be on goes off.
- The two contestants X and Y respond to a question by pushing their switch.
- The contestant who responds fastest causes their LED to light up and at the same time they prevent the LED of their opponent from lighting.

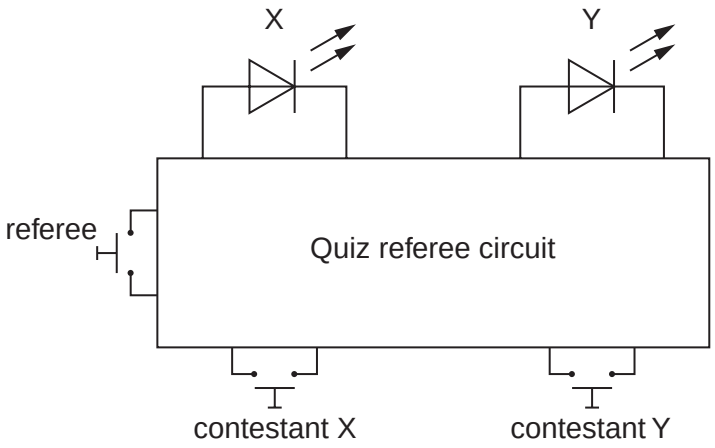
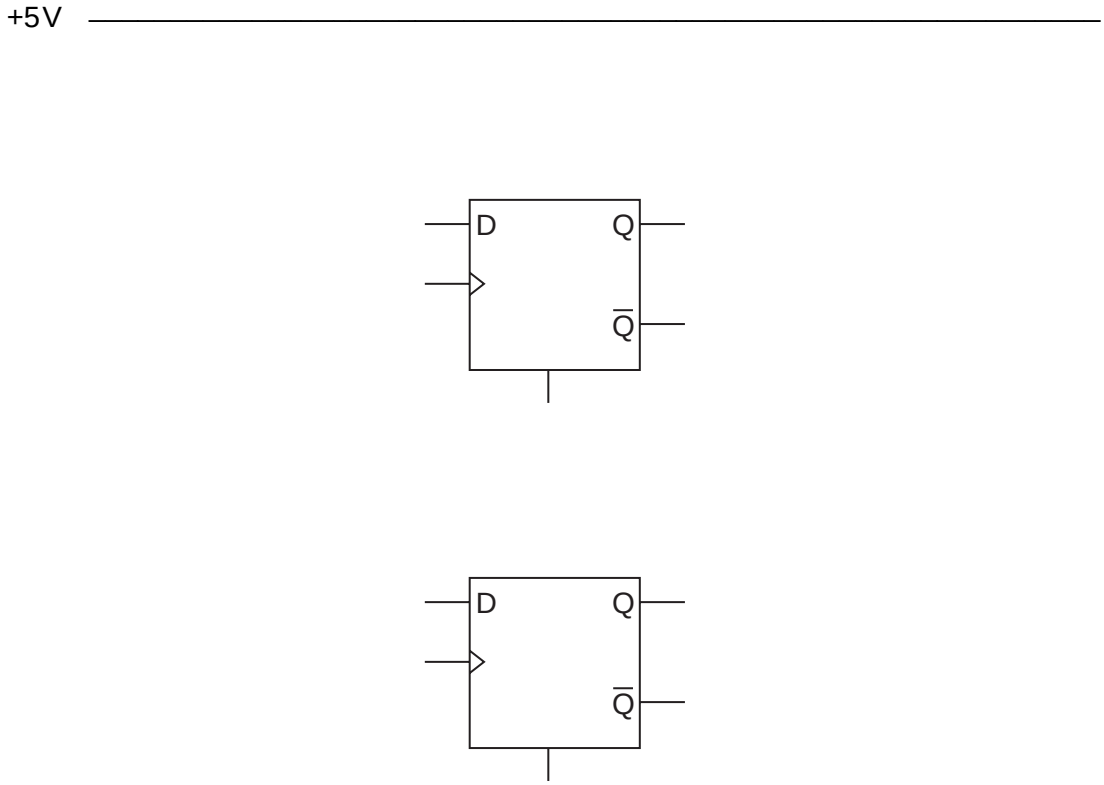


Fig. 7.1

The quiz referee circuit is to be built around the two D-type flip-flops shown in Fig. 7.2.

Complete the circuit in Fig. 7.2 so that it will behave as described above. You must clearly show how all switches are connected and label each one appropriately. Similarly, each LED must be clearly identified with its corresponding contestant.



[8]

Fig. 7.2

Quality of written communication [3]

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