OCR
RECOGNISING ACHIEVEMENT

GCE

# Electronics

Advanced GCE **A2 7826**

Advanced Subsidiary GCE **AS 3826**

# Report on the Units

# June 2008

**3826/7826/MS/R/08**

Oxford Cambridge and RSA Examinations

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# 2526 Foundations of Electronics

## General Comments

Although this paper will be set again this next year for candidates who wish to re-sit, this is the last time that it will attract a significant number of entries. It was good to see that the standard of entry was as high as ever, with a significant number of candidates able to demonstrate a thorough understanding of the contents of the module. In particular, the standard of presentation of calculations was higher than ever, with fewer candidates losing marks on "show that" questions by omitting formulae and powers of ten.

As ever, this report to centres dwells on the failures of weak candidates rather than singing the praises of strong ones. Some of these failures are long standing, others are new. All will need to be remedied for the new specification if weak candidates are to fare any better.

It is clear from their answers that too many weak candidates have a very poor grasp of electrical circuit theory. Their use (or lack of it) of the terms voltage, charge, current and power suggest that their model of electricity is quite at variance with the accepted one. Although one can dwell too long on basic electricity before moving on to a more advanced systems analysis, it probably pays to insist that candidates use the correct terms at all times.

Many candidates are not good at explaining the operation of a circuit. They need to be trained to start at the input and work their way through to the output, explaining the state of the signal(s) at each intermediate stage. Too many presume what the output state is going to be and work their way back to the input to justify it.

## Comments on Individual Questions

1 As always, the first question of the paper is about logic gates, truth tables and logic systems. As expected, nearly all candidates were able to complete the truth tables correctly, but the design of the logic system in NOR gates proved to be more challenging, with only the most able candidates earning full marks. Many candidates simply drew out the circuit without the aid of any truth tables or Boolean algebra to check that it behaved as required - and ended up with an incorrect system.

2 Part (a) was the worst-answered question of the whole paper, suggesting that most candidates still have a weak grasp of electrical circuit theory and the vocabulary required to explain circuit operation. Too many candidates talked of "voltage flowing", with only a minority realising that the low resistance of the closed switch was important. On the other hand, almost every candidate could show how to place the voltmeter for (b) and calculate the time constant in (c)(i). For (c)(ii), too many candidates could not use the terms voltage, current and charge correctly in their explanation. The calculation of (c)(iii) was only accessible to those strong candidates who could remember the formula $t = RC\ln(V_0/V)$.

3 This question followed the normal pattern of easy short parts interspersed with longer harder parts involving explanations and calculations. Very few candidates failed to identify the LDR or describe its properties correctly, but too many thought that the 12 kΩ series resistor was there to protect the LDR from too much current - clearly confusing it with an LED! The series of calculations for (b) were well done by the majority of candidates, with only the weakest struggling to obtain the correct answer. Part (c) required candidates to explain the operation of the circuit. Only the strongest candidates were able to do this methodically enough to earn full marks, starting with the inputs and working their way through to the output, describing all the signal changes along the way with correct

vocabulary. Since at least 10% of the marks for this paper were awarded for explaining circuits, it would pay centres to invest some time in imparting this skill to their candidates.

4 This question returned candidates to their preferred territory of digital electronics, but as ever, their understanding of bistables often left much to be desired. Having successfully completed the truth table, many candidates could earn marks for (b) as they were told the answer, but floundered in (c) they weren't. Too many assumed that if the LED came on when the switch was closed, it would go off again when the switch was opened. Only strong candidates could provide a methodical explanation - too many weak candidates failed to specify which gate or signals they were talking about, despite the labels being on the diagram for them, and often didn't give enough deep detail about the behaviour of the gates (e.g. any one input high forces the output of the gate low). They fared little better in the calculations of part (d), often using the wrong voltage drop across the series resistor. For (d)(iii), candidates were required to justify the use of a series resistor with reference to the properties of an LED. Although the majority knew that the resistor limited the current in the LED, almost none related this to the diode characteristic.

5 This question was about a power supply circuit. Most candidates had little difficulty in identifying the zener diode, connecting the oscilloscope and filling in the block diagram. The role of the diode bridge in doubling the frequency of charging the capacitor proved to be beyond weak candidates, as was the ability to draw an oscilloscope trace correctly. Too many weak candidate ignored the timebase and vertical amplifier settings and treated the grid as graph paper, setting out their own scales. It was good, however, to find that most candidates had the correct shape for the waveform, suggesting that they had come across it in their practical work. Sketches of the zener diode characteristic often lost marks through careless drawing, especially in the region where the current should be zero.

6 Candidates have always found it easier to describe device characteristics with algebra, tables and graphs than with words. So many candidates lost marks in (a) by failing to specify completely the behaviour of a NAND gate, usually by omitting to mention the state of the output for one or more input states. It was noticed that candidates no longer use the terms true, false, on and off for logic gates. Very few candidates failed to earn full marks for completing the truth table, and most were able to explain the role of the thermistor in providing a temperature dependent signal for the system. Part (b)(ii) required candidates to use the graph to find the thermistor resistance at 0°C, without telling them. Many weak candidates struggled on with only the data in the stem of the question, suggesting that they weren't registering all the data provided as they cam across it. Part (c) was well answered by candidates who analysed the circuit methodically, stating changes to signals as they passed from input to output. Many weak candidates assumed that the alarm would come on when the switch was pressed, and then tried to justify that assumption, getting lost along the way.

7 This question proved to be the hardest of the whole paper for weak candidates. Deriving formulae from basic principles is also on the new specification, so questions of this type will appear in future. They are the analogue equivalent of the use of Boolean algebra to analyse the behaviour of a logic system. Surprisingly, many candidates failed to spot that the inverting input of the op-amp should be at 0 V, and even more could not justify it in terms of the feedback being applied. Most candidates could select the correct formula in (a)(ii), but only a small minority earned all of the marks for (iii) and (iv). Many had to cheat with the minus sign in (a)(iv) to get the required answer! Candidates had to calculate the gain of the amplifier in order to draw the transfer characteristic for (b); too many candidates lost marks through inaccurate drawing of gradient and saturation levels. With four marks at stake, candidates should spend a little time with a ruler drawing the lines in the right place. The voltage follower of (c)(i) proved to be a step too far for the vast majority of candidates. Many attempted to draw a non-inverting amplifier, then apply the inverting amplifier

formula to obtain resistor values. Part (ii) required the correct use of the terms voltage, current and power - beyond many weak candidates.

8 This was intended as a straightforward end to the paper, and so it proved for many candidates. Putting the statements in the correct order to match the timing diagram was well done by the majority of weak candidates. It was rare to find more than one mistake.

# 2527 Principal Moderator's Report - Signal Processing Circuits

**General Comments**

The majority of candidates were able to demonstrate some degree of understanding of most aspects of the AS course. Indeed most had a clear understanding of Boolean algebra that was tested in questions 1 and 2.

As has been mentioned in previous reports, there was evidence that marks were lost due to book learning not having been reinforced by appropriate practical work. By way of example, many candidates were able to draw a bass cut filter for the early part of question 4 but few were aware of the frequency response and less still aware of the characteristics of the 081 type op amp. This lack of knowledge of the 081 type was also evident in question 5 (e). Question 7, that referred to a quiz referee circuit, also demonstrated that many candidates were familiar with a practical solution to such a problem, whilst others seemingly had little experience to call upon. Of some concern was the response to the op amp circuit of question 6. A small but significant number of candidates did not recognise the circuit diagram as an integrator or ramp generator. In addition many candidates stated but were not able to "explain" the response of the motor in parts (b) (ii), (c) and (d), being unclear as to the function of the capacitor within such a circuit. There was also a marked lack of clarity amongst many candidates in response to part (f) (ii) in the same question that tested understanding of "loading effect" on potential dividers.

**Question 1**

(a) Most candidates obtained maximum marks for this part of the question.
(b) Many candidates obtained full marks but some gave G in terms of E and F in part (iii). De Morgan's Theorem was not always known by name and was rarely described correctly in those instances when this was the case.
(c) Some candidates found difficulty in generating the correct Boolean algebra expression for P in part (i) but recognised the diagram as an Exclusive Or gate and stated the expression which was accepted.

**Question 2**

(a) Most candidates obtained maximum marks for this part of the question.
(b) The majority of candidates had little difficulty in selecting the correct Boolean expression.
(c) Most candidates obtained maximum marks for this part of the question.

**Question 3**

(a) Many candidates obtained maximum marks for this part of the question. Some subtracted 0.4 V from 8 V before calculating the current. The most common error for part (iii) was to divide 8 volts by 0.4 V instead of using 20 V.
(b) The most common error in part (i) was to omit the "k" in kilohms and divide 0.4 V by 1.6 Ω. Some candidates had difficulty in converting to or from amps or milliamps. A number of candidates selected 1.9 V instead of 1.5 V when calculating the internal resistance in part (ii).

**Question 4**

(a) The circuit diagram for the filter was accurately completed by the majority of candidates, calculations of resistance and capacitance were correct and working out was shown. The capacitor was incorrectly positioned by a few candidates.
(b) Many candidates were able to draw a reasonable graph with the break frequency correctly positioned. Fewer were able to draw the power of 10 roll-off below 320 Hz.

(c) There was a poor response to this part of the question with very few candidates aware of the characteristics of the 081 type op amp.

**Question 5**

Parts of this question were only well answered by a few candidates.

(a) Most candidates obtained maximum marks for this part of the question but some saw it as an audio filter circuit.

(b) The ramp rate equation was not recalled by a significant number of candidates in part (i) and of those that did a number omitted the minus sign and therefore did not show that the rate fell as required by the question. In part (ii) many candidates stated what they believed to be the response of the motor but few explained their reasoning. Those that did often gained full marks, recognising that saturation was reached after approximately 13 s and that the motor continued at a fixed speed for the remaining 7 s.

(c) Very few candidates were able to explain that with S2 pressed there was no input to the circuit and therefore there was no further integration. Consequently the motor continued at a fixed speed as the voltage was not changing.

(d) A greater number of candidates recognised that applying switch S1 discharged the capacitor so stopping the motor.

(e) Some candidates made informed guesses as to the current handling capacity of the 081 type op amp being the key issue but very few seemed to be aware of its characteristics.

(f) The majority of candidates correctly drew the potential divider arrangement in part (i) and many successfully selected suitable resistance values for part (ii). However very few demonstrated an understanding of the “loading effect” and even fewer could apply it.

**Question 6**

Parts of this question were only well answered by a few candidates.

(a) In explaining the meaning of “saturated”, responses were mainly confined to references to plus or minus 13 V and rarely made a link to the power supply or supply line. Responses to the meaning of “virtual earth” were better with some candidates referring to a lack of a current source or sink or the role of feedback.

(b) Although many candidates were able to successfully calculate the currents through the two input resistors in part (i), only a few commented upon the high input impedance of the op amp and its relevance in finding the current through the feedback resistor. Many candidates simply quoted the summing amplifier formula to show that the output was -7 V in part (ii) with only a few realising that the application of Ohms Law was what was required.

(c) Many candidates quoted and then used the summing amplifier formula whereas a derivation based upon Kirchhoff’s Law was required.

(d) Relatively few candidates noted that the batteries were placed in opposing directions within the circuit diagram and therefore the circuit generated an amplified difference between V1 and V2.

**Question 7**

This question was often very well done having clearly been well taught.

Many candidates did score maximum marks but others made silly mistakes like leaving out the switch resistor or the LED resistor. There were some ingenious solutions beyond the obvious cross coupled $\overline{Q}$ and D for locking out the loser.

However some candidates were clearly unaware as to how to approach such a problem with proposed solutions that connected the Q into the R alongside the referee's switch (but with no gate) or taking the $\overline{Q}$ from one D type and putting it into the Q of the other, which leads one to ask just how much practical experience such candidates have gained during their course.

# 2528 Electronics (Project 1)

**General Comments**

For this last report of the current specification, it was thought instructive to discuss in detail some of the criteria which have consistently caused problems for centres and, consequently, moderators. The criteria to be discussed still have a major role in the new specification so it is hoped that this report can serve as extra guidance, in addition to the guidance already in place on the OCR website (www.ocr.org.uk/).

The criteria to be discussed are those which relate to the core premise of this coursework, namely, the design – build – test – analyse cycle and the use of subsystems to realise the final circuit.

The starting point for all circuits must be the full circuit specification, covered by criterion A. The specification can be thought of as a 'wish list' that the final circuit should achieve, given the constraints of the equipment available, and the time limit. It is important to specify the equipment available as this highlights any restrictions which may be placed on testing procedures. This part of the specification is often overlooked by candidates and can be a source of mark adjustment. Components and i.c.s should not normally be mentioned – they do not form part of the specification. A good specification is necessary as it outlines what should be achieved and hence, what should be tested in order to show that a particular aspect of the specification has actually been achieved. The specification is so important that candidates are advised to spend some time formulating it, researching the final circuit (research does not mean copying a given circuit from the web or elsewhere).

The full circuit specification is not the sole specification quoted. Each subsystem should also have a brief specification. A subsystem will have input(s) and desired output(s) and this should be specified as well. The best place for this is at the beginning of each subsystem write-up. It is for this reason that the 'diary style' of report writing is not recommended as candidates tend to omit this important detail and only report on what has been achieved on a particular day. Having completed the circuit specification, subsystems can then be designed, built, and tested using an appropriate test procedure. Currently, subsystem development and testing is covered by criterion D. The marking of criterion D has been problematic for some centres that have consistently marked this section too generously. The question of 'evidence of testing' has arisen time and time again and it is important that centres are clear what is expected as marks cannot be given if there is no evidence of a test procedure. Before looking at some appropriate test procedures, let us consider some unacceptable ones:

- Bland statements of the kind, 'the subsystem was tested and it worked fine' (no evidence provided whatsoever)
- Submitting simulated test results as the only evidence of testing
- Using a test procedure which is inappropriate.

An inappropriate test procedure is one in which the test equipment used or the testing procedure is not suitable for the given inputs/outputs. For example, testing the response of a filter using only a voltmeter.
In order to decide upon a suitable test procedure, the expected inputs/outputs need to be considered. In general, there will be 4 possible types of signal:

- Digital - static
- Digital – time varying
- Analogue - static
- Analogue - time varying

Whichever test procedure is adopted, candidates must first state how the test procedure is to be accomplished and ideally provide a sketch of the proposed setup. The test is then carried out and the results of the test presented in a suitable manner. Ideally, a thumbnail digital colour photograph should be taken to show the setup. Let us consider some examples – these are only examples of possible testing procedures and other suitable procedures do exist.

1. Static digital signal – for example, the output from a combinational logic system or even an n-bit counter clocked at low frequency. Possible test procedure involves hanging current limited LEDs on each output in question and, possibly, the inputs. A truth table can then be constructed for all combinations.
2. Time varying digital signal – for example, a high frequency square wave. This could be tested using an ordinary oscilloscope but the screen shot must be taken and the time scale and voltage amplification must be evident – the reader of the report should be able to calculate the amplitude and frequency of the signal – if not, the evidence is not suitable.
3. Static analogue signal – for example, the output of an opamp comparator. In this example, there may well be three signals to record – two inputs and one output. One suitable test procedure could involve putting both inputs into a dual beam oscilloscope and hanging two different coloured LEDs on the output to show positive saturation and negative saturation.
4. Time varying analogue signal – for example, a filter. Both input and output could be displayed on a dual beam oscilloscope and a suitable frequency range decided upon. A signal generator is used to provide the input and a range of frequencies inputted to the filter. For each chosen frequency, the input amplitude (which could be constant) is noted, along with the corresponding output amplitude. A table of results is constructed and the filter response drawn.

It is also important to test fully the final circuit as well as the individual subsystems. This important test procedure is often omitted by candidates. Being the last system to test, it is frequently overlooked by candidates but this is where the full system specification is tested and analysed to show that the specification has been achieved.

Whichever type of signal is to be tested, it is the responsibility of the candidate to ensure (a) a suitable test procedure is adopted, and (b) the results are clearly displayed and all relevant measurements can be ascertained from the displayed results.

Once the results of a test procedure have been successfully taken, these results can then be analysed against the subsystem/full circuit specification. Currently, this section is covered by criterion E. The analysis is done to verify that the specification has been achieved – if not, it may well be necessary to modify the circuit and test again. Typically, the analysis is often weak or non-existent. Having provided test result/s, candidates often fail to analyse these and relate them to the initial specification. This also has repercussions for criterion F (extent to which the final circuit has achieved the specification). If the final circuit is not tested, or if these results have not been analysed, how can a high mark be given for this section?

Let us assume that a candidate is awarded the following marks:

- Criterion D – 10/10
- Criterion E – 8/8
- Criterion F – 4/4

This means that it is clear in the report that the project has been constructed using a subsystem approach, that every subsystem and the final circuit have been fully tested and that the report contains all the evidence of this. Also, that all test results have been suitably analysed, and that the test results of the final circuit have been fully analysed and referenced back to the specification to show that all aspects of the specification have been achieved. This, of course, assumes that the specification is rigorous and identifies all the main points.

**Other Points Arising**

Quality of circuit build (criterion G) – one or two centres were still marking this too generously, and in some cases a centre mark of 8/8 has been adjusted to 5/8. In order to score full marks the final circuit must be colour coded, neat, and all subsystems well positioned. For example, minimal colour coding could assume red wire for positive supply, black wire for 0V, any colour for negative supply (but not red or black or any other colour used on the board), and the inputs and outputs to subsystems of different colours. Neatness assumes that all wires will be flat to the board and run in a horizontal or vertical direction. There should be no loops and no wires should cross components or be too close to a chip to make removal of the chip necessitate removing wires.

Accuracy of the report (criterion K) – apart from inaccuracies which have been introduced in the report, many candidates omit essential information relevant to the report. Examples of such include how a test was performed, any problems which may have arisen in the building of the circuit (it seems many candidates build circuits which need no debugging whatsoever), and, in the case for those candidates who build the final circuit on pcb (highly discouraged), how the pcb was designed and constructed.

Quality of Written Communication (Criterion L) – the word limit of 2500 words is sometimes exceeded by candidates and these reports are subsequently penalised. These reports are nearly always too verbose and lack concision – they also tend to be reports which also lack detailed testing and analysis.

Circuit diagrams (criterion M) – some candidates failed to provide a full circuit diagram. Also, some of the commercially available schematic drawing packages can produce circuit diagrams which are very small and difficult to read.

Further support on coursework is available from the OCR website. Should more detail be required, do not hesitate to contact the subject officer (mark.judge@ocr.org.uk).

# 2529 Communication Circuits

## General Comments

It was good to see that the standard of preparation of candidates for this paper was as high as ever. Many candidates had ample opportunity to show how much they had learnt on the A2 course, and their centres have much to be proud of.

This report will necessarily concentrate on aspects of the paper which caused candidates difficulty. It can be argued that sometimes this is because the way a question is phrased lacks clarity or more is required of a candidate than is specified in the question. However, there were no questions for which no correct answers were supplied, and the best candidates could answer everything. Even the weakest candidates were supplying answers to most of the questions, so they clearly though that they knew what the question was about!

This paper has a large synoptic element, requiring candidates to earn about a third of the marks for AS work in the A2 context of communications. It was noticeable that candidates were less competent at analogue topics than digital topics from AS. Centres could bear this in mind as they teach the A2 course and take every opportunity for candidates to review AS work of an analogue nature.

## Comments on Individual Questions

1 Although the calculation of (a)(i) was done well by the majority of candidates, the explanation of tuned circuit operation for (a)(ii) was not. Candidates often failed to use the terms voltage, current and resistance correctly - often relying on the word "signal" instead. However, most candidates drew the correct three spikes for the frequency spectrum for (a)(iii), with fewer rounded humps than in previous years. As expected, only strong candidates were able to give sensible reasons why MOSFETs made better amplifiers than NPN transistors for tuned circuits. The calculations of (c) provided good differentiation, with weak candidates assuming that the voltage drop across the drain resistor was the same as the voltage at the drain. It was good to find that many candidates could provide a good explanation for the sign of the amplifier gain, based on postulating a change of voltage at the input and working out the consequent changes of current and voltage in the rest of the system. Some candidates assumed a variable resistor model for the MOSFET; a current sink model is more appropriate for amplifiers.

2 Many candidates confuse term "explain" with the term "describe". So for (a), many candidates mentioned two advantages instead of mentioning one and justifying it. Nevertheless, it was good to find that most candidates could say something sensible about both analogue and digital signals. Most candidates drew, as required, an amplitude modulated waveform for (b)(i), but often had a sine wave modulated onto a square wave carrier rather than the other way round. Part (b)(ii) was probably the worst answered question of the whole paper. Although many candidates realised that serial form required the addition of start and stop bits, giving 10 bits per word, they stopped when they realised that 10 bits per sample $\times$ 10 000 samples per second = 100 kbits $s^{-1}$. Few candidates went on to explain why that bit rate resulted in a bandwidth of 100 kHz, assuming that they had already proved it. Part (c) was well answered by many candidates, including the use of large enough resistors and appropriate capacitors. The block diagram of (d) rarely earned all three marks because many candidates insisted on putting the filter immediately before the shift register rather than after the DAC. This may be because they had not fully grasped the context of the question, and had forgotten the digital nature of the signal from the radio receiver.

3 This series of calculations for a transistor amplifier was well answered by the majority of candidates. Some lost marks in (b) by using the voltage divider formula instead of Ohm's Law, as directed, and only a minority remembered that the gain in (d)(iii) was negative.

4 The first two parts of this question were synoptic, testing understanding of aspects of the AS course. As expected, most candidates earned all three marks for adding a logic gate to reset the counter, but only a minority earned full marks for showing how to make the counter from flip-flops. Common errors included using Q instead of $\overline{Q}$ to trigger the next flip-flop and getting the order of the outputs wrong. Part (c) required candidates to analyse the system by putting sentences in the correct order. It was good to find that most candidates could earn most of the marks for this. Part (d) proved to be more difficult. Many candidates failed to realise that 0, a, b, c, d and 1 emerged from the shift register in that order, assumed that the final bit told the receiver that the transmission was over, or failed to mention the role of the receiver at all. Surprisingly few candidates earned any marks at all for (e), suggesting that they lacked much experience of this type of circuit.

5 This question was almost entirely synoptic. Parts (a) and (b) were well answered by most candidates, although it was rare to find a two op-amp circuit which had a gain of only 50 between the break frequencies. Although the calculations of (c) were well done by the majority of candidates, suggesting that they had a good understanding of the concept of output impedance, only a few could draw an op-amp circuit with a gain of +1. Too often, they drew an inverting amplifier instead of a non-inverting one.

6 This final question was about time-division multiplexing and its implementation with logic gates. Few candidates had a good enough grasp of Boolean algebra to earn all three marks for part (b)(i) (many attributed the last stage of the proof to the Redundancy Theorem instead of the Race Hazard Theorem, and not a few invoked the use of De Moivre's Theorem instead of De Morgan's. Despite clear instructions, many candidates lost marks for (b)(ii) by failing to label the output of each gate with its Boolean expression. Had they done so, they might have recognised that their circuit did not have the intended behaviour and changed its design accordingly. Part (c) was well done by many, including the final circuit using NOR gates. Again, many lost a mark by not justifying their circuit in enough detail.

# 2530 Control Circuits

**General Comments**

As has been the case in the previous six papers of the Curriculum 2000 Electronics course, there was a wide range of responses seen by examiners with some candidates showing a high level of understanding and the ability to apply their knowledge whilst others showed little awareness of even the basic concepts.
Overall the standard remains high and many candidates were able to make good attempts at every question with some outstanding responses in a few cases.

**Question 1**

(a) Although many candidates were aware of the existence of the Program Counter, only a few recalled that it held the address of the next instruction to be processed and that it is normally incremented.
(b) This was well answered by candidates.
(c) Many candidates incorrectly suggested that the memory locations could contain code as well as data.
(d) The function the ALU was well understood by the majority of candidates.

**Question 2**

(a) In i) a few candidates mistook the NOR for a NAND gate. In ii), although many stated that the output “floated” , only a smaller number were able to explain what was meant by this term.
(b) Although many students stated that “double 0” on both inputs was impossible, only a few explained why this was the case. Others stated that the presence of the NOT gate was crucial but then failed to elaborate.
(c) This was answered well.
(d) A significant number of candidates gave “triac” in their response to (i). In the response to (iii) there were many references to “multiplexing” but only a few also suggested “economy of tracking or wiring” as a reason.

**Question 3**

(a) Most candidates scored all the available marks for the calculations.
(b) Again calculations of the current were, in the main, correctly performed but the current rating was sometimes set too low at 4.2 to 4.5 A.
(c) Generally resistance values were again correctly calculated with a few candidates seemingly mis-reading the position of R2 and R3 on the circuit diagram.
(d) A significant number of candidates stated the characteristics of a triac but did not explain how these related to the scenario outlined in this part of the question.
(e) On the whole there was a poor response to this part of the question. Very few candidates realised the effect of the change in potential on either side of the capacitor plates when the switch S2 was pressed and how this led to zero current flow to triac T1, so switching it off.
(f) Generally the drawing of the potential divider was well done by the majority of candidates but some did not relate their diagram to triac T2, drawing the light dependent resistor in the incorrect position. In addition a few responses failed to show the connection to resistor R3 as required by the question.
(g) Although many students stated that alternating current passes through zero during its cycle, only a few explained the significance of this as far as the action of a triac is concerned.

**Question 4**

(a) The majority of candidates referred to a lack of an electrical connection.
(b) The action of a transformer was poorly explained, with little reference to variations in current and potential difference being a key feature.
(c) The device was correctly named by the majority of candidates but a few referred to the two components shown in figure 4.2. In explaining the action of figure 4.2, only a few candidates mentioned that current variation was the cause of change in light intensity in circuit A.
(d) This part was poorly done with the majority stating that light and electro-magnetic variations were the only difference between the two methods.

**Question 5**

(a) This was generally well answered.
(b) Many responses of “17” were given for the number of data pins.
(c) Many candidates stated what was meant by “unidirectional” and did not relate their response to the “address bus” as required by the question.
(d) Many candidates stated what was meant by “bidirectional” and did not relate their response to the “data bus” as required by the question.
(e) The difference between “state” and “explain” also had an impact upon the marks obtained by some candidates in this part of the question. The action of “read”, “write” and “enable” were stated but it was not explained how this action related to the storage and retrieval of a “word”, and, in particular, the order in which the process occurs.

**Question 6**

This year marked a slight change in the structure of the question with candidates being asked to explain the action of the instructions and then to briefly summarise the overall impact of a section. Many candidates seemed to benefit from this arrangement.

(a) The majority of marks on offer were obtained by most candidates in this section.
(b) This section also provided maximum marks to the majority of candidates with many recognising the time delay sub-set of instructions.
(c) Only a few candidates realised that the 7-segment displays were blanked out within this section of code and that “E6 10” tested for switch A alone before jumping to the appropriate address for further processing.
(d) Many candidates found this section a challenge with only a few able to explain the relevance of adding”04” to the score of A or B, although many stated in their summary that the purpose of the section was to increment the score of A or B as appropriate.
(e) Only a few candidates successfully explained the code used in this section; in particular the relevance of adding “02” or “01” to the score of A or B respectively, the testing for the “test switch”, and the return to address “10” which represented the start of the time delay in section (a).

# 2531 Principal Moderator's Report - Electronics (Project 2)

The comments made in the AS report about the design - build – test – analyse cycle are also relevant to Project2 and have been reprinted at the end of this report. Before that, some specific comments on Project2 are to be made.

It is important that the centre shows in the report where marks have been awarded. Some centres offered reports that had no teacher comments whatsoever and this makes the moderation process difficult. The preferred technique is to use a red pen and highlight in the report where a particular criterion has been awarded marks.

Some of the projects seen this year were very ambitious and, I should imagine, have taken a lot more that the proposed 20 hours of laboratory time to complete. As always, there was a wide spread in the type of projects undertaken by candidates; the vast majority of which were most suitable. The choice of project is an important one and candidates must not attempt those projects which are too complex for the candidate – this is another reason why candidates must thoroughly research the project before attempting a solution. For the more able candidate, a complex project can give the candidate a suitable challenge and the mark awarded for criterion J (elegance, brilliance, etc.) can reflect this.

Alternative circuits (Criterion B) were generally weak this year but were usually accurately marked. As stated previously, candidates could consider an alternative to the full circuit or just consider alternatives to two subsystems. In either case, it is expected that candidates will offer circuit diagrams of the alternative, a full description of how it works, and valid reasons why the alternative was not chosen. The solution to many digital circuits could involve the use of a microcontroller. However, it is not sufficient for candidates to report, 'this circuit could be achieved using a microcontroller…' In order to score highly, candidates would be expected to describe the function of the microcontroller, possibly supplying a flowchart.

Criterion H (impedance matching etc.) still causes trouble for some centres. Although a little dated with modern ICs (and this criterion does not appear in the new specification), to score highly in this section the signal transfer between each subsystem must be considered and it shown that the signal does not suffer significant degradation.

Criterion J (elegance, brilliance, etc) is designed to reward those candidates who have worked particularly well on the project, have developed some neat solutions, or have successfully attempted a more ambitious project.

As mentioned in the AS report, candidates are usually not reporting on any problems encountered in the construction of subsystems. In practice, it is usually necessary to debug circuits for a multitude of reasons – these should be referred to in the report and this is marked in criterion K.

For Criterion M, a full circuit diagram is expected, in addition to subsystem diagrams. Candidates must ensure that the diagrams fit on A4 paper, and that they are of a suitable size to be read easily. A large project may require the need of 2 sheets of A4.

**The Design – Build – Test – Analyse Cycle of Construction**

The starting point for all circuits must be the full circuit specification, covered by criterion A. The specification can be thought of as a 'wish list' that the final circuit should achieve, given the constraints of the equipment available, and the time limit. It is important to specify the

equipment available as this highlights any restrictions which may be placed on testing procedures. This part of the specification is often overlooked by candidates and can be a source of mark adjustment. Components and ICs should not normally be mentioned – they do not form part of the specification. A good specification is necessary as it outlines what should be achieved and hence, what should be tested in order to show that a particular aspect of the specification has actually been achieved. The specification is so important that candidates are advised to spend some time formulating it, researching the final circuit (research does not mean copying a given circuit from the web or elsewhere).

The full circuit specification is not the sole specification quoted. Each subsystem should also have a brief specification. A subsystem will have input/s and desired output/s and this should be specified as well. The best place for this is at the beginning of each subsystem write-up. It is for this reason that the 'diary style' of report writing is not recommended as candidates tend to omit this important detail and only report on what has been achieved on a particular day.

Having completed the circuit specification, subsystems can then be designed, built, and tested using an appropriate test procedure. Currently, subsystem development and testing is covered by criterion D. The marking of criterion D has been problematic for some centres that have consistently marked this section too generously. The question of 'evidence of testing' has arisen time and time again and it is important that centres are clear what is expected as marks cannot be given if there is no evidence of a test procedure. Before looking at some appropriate test procedures, let us consider some unacceptable ones:

- Bland statements of the kind, 'the subsystem was tested and it worked fine' (no evidence provided whatsoever)
- Submitting simulated test results as the only evidence of testing
- Using a test procedure which is inappropriate.

An inappropriate test procedure is one in which the test equipment used or the testing procedure is not suitable for the given inputs/outputs. For example, testing the response of a filter using only a voltmeter.
In order to decide upon a suitable test procedure, the expected inputs/outputs need to be considered. In general, there will be 4 possible types of signal:

- Digital - static
- Digital – time varying
- Analogue - Static
- Analogue - time varying

Whichever test procedure is adopted, candidates must first state how the test procedure is to be accomplished and ideally provide a sketch of the proposed setup. The test is then carried out and the results of the test presented in a suitable manner. Ideally, a thumbnail digital colour photograph should be taken to show the setup. Let us consider some examples – these are only examples of possible testing procedures and other suitable procedures do exist.

5. Static digital signal – for example, the output from a combinational logic system or even a N bit counter clocked at low frequency. Possible test procedure involves hanging current limited LEDs on each output in question and, possibly, the inputs. A truth table can then be constructed for all combinations.
6. Time varying digital signal – for example, a high frequency square wave. This could be tested using an ordinary oscilloscope but the screen shot must be taken and the time scale and voltage amplification must be evident – the reader of the report should be able to calculate the amplitude and frequency of the signal – if not, the evidence is not suitable.
7. Static analogue signal – for example, the output of an opamp comparator. In this example, there may well be 3 signals to record – 2 inputs and 1 output. One suitable test procedure

could involve putting both inputs into a dual beam oscilloscope and hanging 2 different coloured LEDs on the output to show positive saturation and negative saturation.

8. Time varying analogue signal – for example, a filter. Both input and output could be displayed on a dual beam oscilloscope and a suitable frequency range decided upon. A signal generator is used to provide the input and a range of frequencies inputted in to the filter. For each chosen frequency, the input amplitude (which could be constant) is noted, along with the corresponding output amplitude. A table of results is constructed and the filter response drawn.

It is also important to test fully the final circuit as well as the individual subsystems. This important test procedure is often omitted by candidates. Being the last system to test, it is frequently overlooked by candidates but this is where the full system specification is tested and analysed to show that the specification has been achieved.

Whichever type of signal is to be tested, it is the responsibility of the candidate to ensure (a) a suitable test procedure is adopted, and (b) the results are clearly displayed and all relevant measurements can be ascertained from the displayed results.

Once the results of a test procedure have been successfully taken, these results can then be analysed against the subsystem/full circuit specification. Currently, this section is covered by criterion E. The analysis is done to verify that the specification has been achieved – if not, it may well be necessary to modify the circuit and test again. Typically, the analysis is often weak or non-existent. Having provided test result/s, candidates often fail to analyse these and relate them to the initial specification. This also has repercussions for criterion F (extent to which the final circuit has achieved the specification). If the final circuit is not tested, or if these results have not been analysed, how can a high mark be given for this section?

Let us assume that a candidate is awarded the following marks:

- Criterion D – 10/10
- Criterion E – 8/8
- Criterion F – 4/4

This means that it is clear in the report that the project has been constructed using a subsystem approach, that every subsystem and the final circuit have been fully tested and that the report contains all the evidence of this. Also, that all test results have been suitably analysed, and that the test results of the final circuit have been fully analysed and referenced back to the specification to show that all aspects of the specification have been achieved. This, of course, assumes that the specification is rigorous and identifies all the main points.

**Further Sources of Support**

The OCR website, www.ocr.org.uk, contains support for both the current and the new specification.
Teachers of electronics are also encouraged to join the OCR Electronics Communities forum where support/discussion takes place. See the OCR website for more details and how to join the Community.

# Grade Thresholds

**Advanced GCE Electronics 3826 7826**
**June 2008 Examination Series**

**Unit Threshold Marks**

| Unit | | Maximum Mark | A | B | C | D | E | U |
|---|---|---|---|---|---|---|---|---|
| **2526** | Raw | 120 | 86 | 77 | 69 | 61 | 53 | 0 |
| | UMS | 120 | 96 | 84 | 72 | 60 | 48 | 0 |
| **2527** | Raw | 90 | 59 | 52 | 45 | 39 | 33 | 0 |
| | UMS | 90 | 72 | 63 | 54 | 45 | 36 | 0 |
| **2528** | Raw | 78 | 61 | 54 | 47 | 40 | 33 | 0 |
| | UMS | 90 | 72 | 63 | 54 | 45 | 36 | 0 |
| **2529** | Raw | 120 | 87 | 78 | 69 | 61 | 53 | 0 |
| | UMS | 120 | 96 | 84 | 72 | 60 | 48 | 0 |
| **2530** | Raw | 90 | 65 | 59 | 53 | 47 | 41 | 0 |
| | UMS | 90 | 72 | 63 | 54 | 45 | 36 | 0 |
| **2531** | Raw | 90 | 71 | 64 | 58 | 52 | 46 | 0 |
| | UMS | 90 | 72 | 63 | 54 | 45 | 36 | 0 |

**Specification Aggregation Results**

Overall threshold marks in UMS (ie after conversion of raw marks to uniform marks)

| | Maximum Mark | A | B | C | D | E | U |
|---|---|---|---|---|---|---|---|
| **3826** | **3826** | 300 | 240 | 210 | 180 | 150 | 120 |
| **7826** | **7826** | 600 | 480 | 420 | 360 | 300 | 240 |

The cumulative percentage of candidates awarded each grade was as follows:

| | A | B | C | D | E | U | Total Number of Candidates |
|---|---|---|---|---|---|---|---|
| **3826** | 22.8 | 36.7 | 55.3 | 69.7 | 83.1 | 100 | 699 |
| **7826** | 32.1 | 52.5 | 72.8 | 86.5 | 96.1 | 100 | 421 |

**1120 candidates aggregated this series**

For a description of how UMS marks are calculated see:
http://www.ocr.org.uk/learners/ums_results.html

Statistics are correct at the time of publication.

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