GCE

Electronics

Advanced GCE **A2 7826**

Advanced Subsidiary GCE **AS 3826**

Mark Schemes for the Units

June 2008

3826/7826/MS/R/08

Oxford Cambridge and RSA Examinations

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This mark scheme is published as an aid to teachers and students, to indicate the requirements of the examination. It shows the basis on which marks were awarded by Examiners. It does not indicate the details of the discussions which took place at an Examiners' meeting before marking commenced.

All Examiners are instructed that alternative correct answers and unexpected approaches in candidates' scripts must be given marks that fairly reflect the relevant knowledge and skills demonstrated.

Mark schemes should be read in conjunction with the published question papers and the Report on the Examination.

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MARK SCHEMES FOR THE UNITS

General advice to Assistant Examiners on the procedures to be used

YOU WILL BE REQUIRED TO UNDERTAKE PRACTICE AND STANDARDISATION SCRIPTS BEFORE STARTING TO MARK LIVE SCRIPTS, YOU WILL BE ADVISED OF THE AMOUNT OF SCRIPTS PRIOR TO THE MARKING PERIOD.

1 The schedule of dates for the marking of this paper is very important. It is vital that you meet these requirements. If you experience problems then you must contact your Team Leader (Supervisor) without delay.

2 An element of professional judgement is required in the marking of any written paper. Candidates often do not use the exact words which appear in the detailed sheets which follow. If you are in doubt about the validity of any answer then consult your Team Leader (Supervisor) by phone, the messaging system within SCORIS or e-mail.

3 Some questions may have a 'Level of Response' mark scheme. Any details about these will be in the rationale.

4 If an answer has been crossed out and no alternative answer has been written then mark the answer crossed out.

5 In addition to the award of 0 marks, there is a NR (No Response) option on SCORIS.

<u>Award 0 marks</u>

- if there is any attempt that earns no credit (including copying out the question or some crossed out working)

<u>Award NR (No Response)</u>

- if there is nothing written at all in the answer space
  OR
- if there is any comment which does not in any way relate to the question being asked (eg 'can't do', 'don't know')
  OR
- if there is any sort of mark which is not an attempt at the question (eg a dash, a question mark)

6 Abbreviations, annotations and conventions used in the detailed Mark Scheme. These vary from paper to paper, you will be advised in advance of the correct abbreviations, annotations and conventions to be used.

Highlighting is also available to highlight any particular points on the script.

7 The Comments box

The comments box will be used by your PE to explain their marking of the practice scripts for your information. Please refer to these comments when checking your practice scripts. You should only type in the comments box yourself when you have an additional object of the type described in Appendix B of the Handbook for Assistant Examiners and Subject Markers.

Please do not use the comments box for any other reason.

Any questions or comments you have for your team leader should be communicated by phone, SCORIS messaging system or e-mail.

8 Abbreviations, annotations and conventions that are used in this Mark Scheme vary from paper to paper. The following annotations are available for this paper.

(SO to add any others)

✓and ✗
BOD - Benefit of doubt
NBOD – No benefit of doubt
TV - Too Vague

Highlighting is also available to highlight any particular points on the script.

ADVICE TO EXAMINERS ON THE ANNOTATION OF SCRIPTS

1 Please ensure that you use the **final** version of the Mark Scheme.
You are advised to destroy all draft versions.

2 Please mark all post-standardisation scripts in red ink. A tick (✓) should be used for each answer judged worthy of a mark. Ticks should be placed as close as possible to the point in the answer where the mark has been awarded. Ticks should **not** be placed in the right-hand margin. The number of ticks should be the same as the number of marks awarded. If two (or more) responses are required for one mark, use only one tick. Half marks ($^1/_2$) should never be used.

3 The following annotations may be used when marking. No comments should be written on scripts unless they relate directly to the mark scheme. Remember that scripts may be returned to Centres.

×	= incorrect response (errors may also be underlined)
∧	= omission of mark
bod	= benefit of the doubt (where professional judgement has been used)
ecf	= error carried forward (in consequential marking)
con	= contradiction (where candidates contradict themselves in the same response
sf	= error in the number of significant figures
up	= omission of units with answer

4 The marks awarded for each part question should be indicated in the right-hand margin. The mark total for each question should be ringed at the bottom right-hand side. These totals should be added up to give the final total on the front of the paper.

5 In cases where candidates are required to give a specific number of answers, mark the first answers up to the total required. Strike through the remainder.

6 The mark awarded for Quality of Written Communication in the margin should equal the number of ticks under the phrase.

7 Correct answers to calculations should obtain full credit even if no working is shown, unless indicated otherwise in the mark scheme.

8 Strike through all blank spaces and pages to give a clear indication that the whole of the script has been considered.

The following abbreviations and conventions are used in the mark scheme:

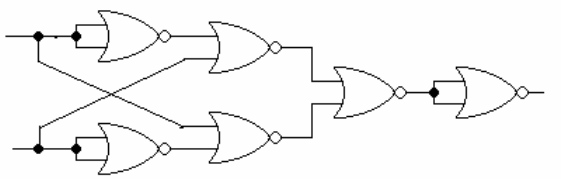
wttee	= words to that effect
/	= alternative correct answers
;	= separates marking points
NOT	= answers which are not worthy of credit
( )	= words which are not essential to gain credit
___	= (underlining) key words which **must** be used to gain credit
ecf	= error carried forward
ora	= or reverse argument
eor	= evidence of rule

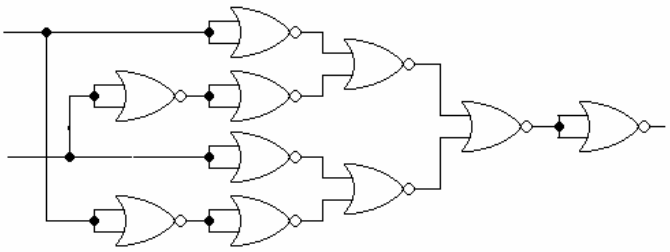
2526 Foundations of Electronics

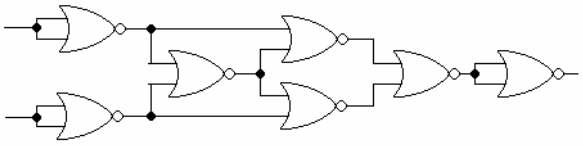
question	grade	expected answer	mark
1a	DE	all four combinations of BA (any order)	1
	DE	Q = 1 for BA = 01 or 10	1
	DE	Q = 0 for BA = 11 or 00	1
1b		C = NOT A	1
		D = NOT B	1
		ecf: E = A AND D	1
		ecf: F = B AND C	1
		ecf: Q = E OR F (ignore Q completely)	0

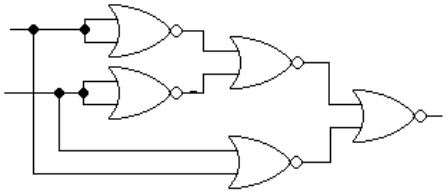
A	B	C	D	E	F	Q
0	0	1	1	0	0	0
1	0	0	1	1	0	1
1	1	0	0	0	0	0
0	1	1	0	0	1	1

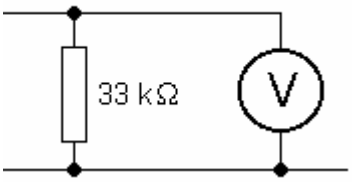
question	grade	expected answer	mark
1c	DE	output generated by a NOR gate	1
	DE	correct use of blobs or bridges	1
	DE	use of NOR gates as inverters at inputs (joined inputs or one input low)	1
	BCD	correct symmetry between inputs	1
	BCD	any of the circuits shown below	1

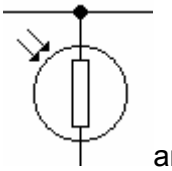






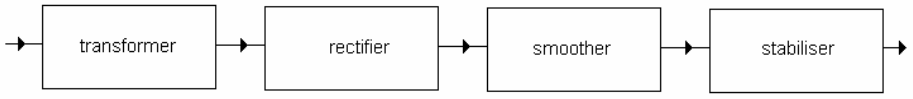
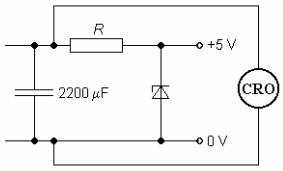
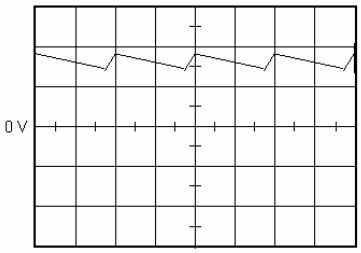
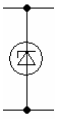


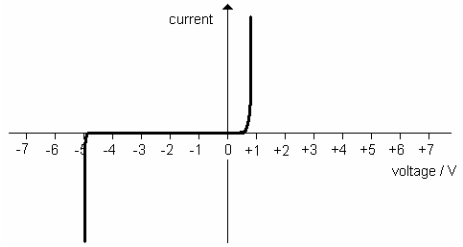
question	grade	expected answer	mark
2a		EITHER	
	DE	switch connects resistor to top supply rail (owtte)	1
	BCD	capacitor charges up <u>rapidly</u> (owtte)	1
		OR	
		switch has very low resistance	
		<u>short time constant</u> for charging circuit	
2b	DE	correct symbol	1
	DE	in parallel with resistor	1
			
2ci	DE	$\tau = RC$ (eor)	1
	BCD	units conversion: $R = 33\times10^3\ \Omega$, $C = 2700\times10^{-6}$ F	1
	DE	ecf incorrect powers of ten: $RC = 33\times10^3 \times 2700\times10^{-6} = 89$ s	1
2cii	DE	capacitor discharges	1
	DE	through resistor	1
	BCD	big time constant / small discharge current	1
2ciii		EITHER	
	AB	$t = \tau\ln(V_0/V)$ or $V = V_0e^{-t/RC}$ (eor)	1
	AB	ecf incorrect τ: $t = 89 \times \ln(15/2) = 179/180$ s	1
		OR	
		drops by 0.37 in RC (eor)	
		$0.37 \times 0.37 \times 15 = 2.0$, so $t = 2 \times 89 = 178$ s (ACCEPT 180 s)	
		OR	
		voltage halves in $0.7RC$ (eor)	
		$15/8 = 1.9$, so $t = 3 \times 0.7$ x 89 = 187 s (accept 190 s)	

question	grade	expected answer	mark
3ai	DE	 any indication of this component	1
3aii	DE	resistance	1
	BC	increases for decreasing	1
	BC	light intensity	1
3aiii	BC	makes a voltage divider	1
	AB	(allows change of resistance) to become a change of voltage (owtte)	1
3bi	DE	27 + 43 = 70 kΩ	1
3bii	DE	$I = V/R$ (eor)	1
	DE	ecf incorrect R: ($15/70\times10^{3}$) = 2.14×10^{-4} A	1
	BCD	ecf incorrect I : units conversion: 214 μA (ACCEPT 210 μA)	1
3biii	DE	$V = IR$ (eor)	1
	BCD	ecf incorrect I: $V = 2.14\times10^{-4} \times 43\times10^{3}$ = 9.2 V	1
		ACCEPT resistor ratio or voltage divider formula	
		evidence of rule for [1]	
		correct answer for [1]	
		210 μA gives 9.0(3) V	
3c	DE	non-inverting input M below inverting input L (owtte)	1
	DE	output N (saturates) low (ACCEPT 0 V)	1
	BCD	at -13 V	1
	BCD	LED is forward biased / voltage across LED	1
	AB	therefore current in LED (so it glows)	1

question	grade	expected answer	mark
4a	DE	first row correct	1
	DE	last three rows correct	1
		<table><tr><th>W</th><th>U</th><th>Q</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	
4b	DE	U goes high / becomes 1 / goes to 5 V	1
	BCD	so Q goes low / becomes 0 V	1
	BCD	no voltage drop / no forward bias across LED	1
		IGNORE references to current in LED	
4c	DE	EITHER (T low)	
	BCD	LED stays off	1
	BCD	both inputs Q, T of left-hand gate low	1
	AB	so output W high	1
		so Q (stays) low / 0V	1
		OR (T high because other switch closed)	
		LED comes on	
		one input of left-hand gate high	
		so output W low	
		so Q goes high / +5V	
4di	DE	SHOW: $P = VI$ - must be formula or correct equivalent, not a triangle	1
	DE	$I = P/V$ (eor)	1
	DE	5×10^{-3} / 1.8 = $\underline{2.8}\times10^{-3}$ A	1
		ACCEPT 2.7×10^{-3} A	
4dii	DE	$R = V/I$ (eor)	1
	BCD	V = 5 - 1.8 = 3.2 V	1
	DE	ecf incorrect V: R = 3.2 / 2.8×10^{-3} = 1.1×10^{3} Ω	1
		600 Ω for [2]	
		1700 Ω for [2]	

question	grade	expected answer	mark
4diii	DE	LED destroyed by too much power / heat (NOT current or voltage)	1
	AB	current rises rapidly with increasing voltage	1
	BCD	resistor limits current / voltage to safe value	1

question	grade	expected answer	mark
5a	DE	[1] per correct box	4
	DE		
	DE		
	BCD		
5bi	DE	each cyle of mains lasts for 1/50 s	1
	DE	or 20 ms	1
	BCD	rectifier / diode bridge	1
	AB	charges capacitor at both positive and negative peaks of voltage / gives two peaks for each cycle / makes the negative voltage positive ACCEPT appropriate sketches of input and output waveforms	1
5bii	DE	one terminal to upper plate (any recognisable symbol)	1
	AB	other terminal to 0 V	1
			
5biii	BCD	correct shape across whole screen	1
	BCD	correct timescale (pattern repeats every 10 ms)	1
	AB	correct peak voltage	1
	AB	correct ripple (ACCEPT half a division)	1
			
5ci	DE		1

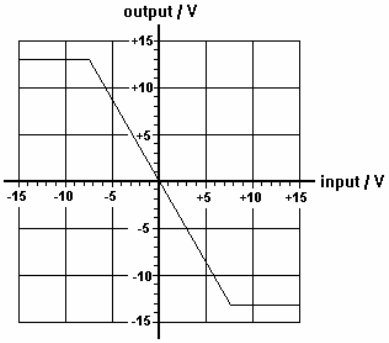
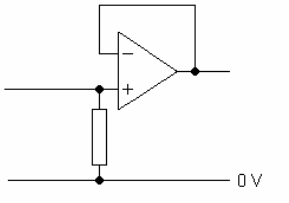
question	grade	expected answer	mark
5cii	DE	correct shape in forward bias (zero then sudden rise)	1
	BCD	correct shape in reverse bias (zero then sudden fall)	1
	AB	correct voltages for sudden increase of current (by eye)	1
			

question	grade	expected answer	mark
6ai	DE	output <u>only</u> low / 0 V / 0	1
	BCD	when both inputs high / 5 V / 1	1
		IGNORE truth table	
		any correct but incomplete description for [1]	
6aii	DE	no ecf from (a)(i): C low when A and B high	1
	DE	C high otherwise	1
	DE	ecf incorrect C: D opposite of C	1
	DE	ecf incorrect D: Q low when D and E high	1
	DE	Q high otherwise	1

E	B	A	C	D	Q
0	0	0	1	0	1
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	1
1	0	0	1	0	1
1	0	1	1	0	1
1	1	0	1	0	1
1	1	1	0	1	0

question	grade	expected answer	mark
6bi	DE	resistance of thermistor decreases	1
	BCD	current increases / voltage across thermistor decreases	1
	AB	voltage across fixed resistor increases	1
6bii	DE	thermistor = 2.5 kΩ ± 0.1 kΩ	1
	DE	$I = V/R$ (eor)	1
	BCD	ecf incorrect thermistor resistance: $I = 5 - 2 / 2.5\times10^{3} = 1.2\times10^{-3}$ A	1
	AB	$R = V/I = 2 / 1.2\times10^{-3} = 1.7$ kΩ	1
		ACCEPT alternative method for full marks (resistor ratios or voltage divider formula) i.e. rule [1], substitution [1], correct answer for stated thermistor resistance [1]	
6c	DE	E goes low / 0 / 0V	1
	DE	Q goes high / 1 / 5V	1
	DE	ecf incorrect Q: alarm sounds	1
	AB	ecf incorrect Q : LED goes out / off	1

question	grade	expected answer	mark
7ai	DE	0 V	1
	BCD	negative feedback (or equivalent explanation)	1
		NOT just "virtual earth" / "inputs at same voltage"	
7aii	DE	$I = \frac{V_{in} - 0}{R_{in}}$	1
7aiii	BCD	$I = \frac{0 - V_{out}}{R_f}$ or $I = -\frac{V_{out}}{R_f}$	2
	AB	[1] for $I = \frac{V_{out}}{R_f}$ or $I = \frac{V_{out} - 0}{R_f}$	
		[2] for $I = \frac{V_{in} - V_{out}}{R_{in} + R_f}$	
7aiv	AB	$G = V_{out}/V_{in}$	1
		linking expressions to answer e.g. $\frac{V_{in}}{R_{in}} = -\frac{V_{out}}{R_f}$ etc.	
	AB		1

7b	DE	straight line through origin (by eye)	1
	BCD	negative slope	1
	BCD	saturates at ±13 V (NOT at ± 12.5 V)	1
	AB	gain of (-)1.74 (13 V out for 7.5 V in)	1
			
7ci	DE	inverting input only connected to output (via resistor)	1
	BCD	(100 kΩ) resistor from non-inverting input to 0 V	1
	AB	input directly to non-inverting input	1
			
7cii	BCD	current at output larger than current at input	1
	AB	power amplifier increases *VI* (owtte)	1

question	grade	expected answer	mark
8a	DE	both A and B are high	1
8b	DE	G before A	1
	DE	A before E	1
	DE	E before D	1
	BCD	D before F	1
	BCD	F before C	1
		got any extra diodes for Christmas?	

Quality of Written Communication

3 The candidate expresses complex ideas extremely clearly and fluently. Sentences and paragraphs follow on from one another smoothly and logically. Arguments are consistently relevant and well structured. There will be few, if any, errors of grammar, punctuation and spelling.

2 The candidate expresses straightforward ideas clearly, if not always fluently. Sentences and paragraphs may not always be well connected. Arguments may sometimes stray from the point or be weakly presented. There may be some errors of grammar, punctuation and spelling, but not such as to suggest a weakness in these areas.

1 The candidate expresses simple ideas clearly, but may be imprecise and awkward in dealing with complex or subtle concepts. Arguments may be of doubtful relevance or obscurely presented. Errors in grammar, punctuation and spelling may be noticeable and intrusive, suggesting weaknesses in these areas.

0 The language has no rewardable features.

2527 Signal Processing Circuits

Question 1

(a) (i) NAND gate (1)

(ii)

A	B	Q
0	0	1
1	0	1
0	1	1
1	1	0

(1) (1) (1)

(iii) $Q = \overline{A \cdot B}$ (1)

(b)

(i) $E = \overline{C}$ (1)

(ii) $F = \overline{D}$ (1)

(iii) $G = \overline{\overline{C} \cdot \overline{D}}$ (1)

(iv) De Morgan's Theorem (1)

(v) OR gate (1)

(c)

(i) $P = \overline{(K \cdot \overline{L}) \cdot (\overline{K} \cdot L)}$ (1) (1)

or $= K\overline{\cdot L} + \overline{K \cdot L}$

(ii) Exclusive OR (1)

(iii) Correct symbol for EOR gate (1)

Question 1 Additional guidance for markers

a. i. gate correct (1)

ii. correct A, B and Q columns (3)
correct A and B columns (2)
correct Q wrt incorrect answer to a. i. (1)
allow A B columns either way around

iii correct Q = $\overline{A \cdot B}$ (1)
ecf from a. ii. (1)
Allow equivalent Boolean expressions

Allow Q = $\overline{A} \cdot \overline{B} + A \cdot \overline{B} + \overline{A} \cdot B$

Allow Q = $\overline{A} + \overline{B}$

b. i. correct E = $\overline{C}$ (nothing else allowed) (1)
ecf from a. ii. not allowed as different configuration

ii. correct F = $\overline{D}$ (nothing else allowed) (1)
ecf not allowed as for b. i.

iii. G = $\overline{\overline{C} \cdot \overline{D}}$ or Boolean simplification (1)
ecf from incorrect response to b. i. / ii. but correct
interpretation of AND gate (1)

iv. De – Morgan's Theorem (1)
Allow correct explanation of the Theorem for 1 mark

v. correct - OR gate (1)

c. i. Allow 1 mark for each term and 1 mark for operators (2)
Remove one mark for each error made
Allow P = K "EOR" L (where EOR is replaced by correct symbol)

ii. Correct - EOR / XOR (1)

iii. Correct symbol for EOR / XOR gate (1)
Allow ecf for incorrect gate response to c. ii. (1)

Question 2

(a)

J	K	H
0	0	1
0	1	0
1	0	1
1	1	1

(1)

(b) $\overline{T} = R + S$ (1)

(c)

X	Y	Z
0	0	0
0	1	0
1	0	1
1	1	0

1 for correct Z = (1)
1 for correct Z = (1)

Question 2 Additional guidance for markers

a. Correct order (1 / 0 / 1 / 1) (1)

b. Correct response (1)

c. Correct order (0 / 0 / 1 / 0) (2)
For correct Z = 0 response (1)
For correct Z = 1 response (1)

Question 3

(a)	(i)	I	=	P / V		(1)
			=	24 / 8		
			=	3 A		(1)
	(ii)	pd lost across internal resistance	=	I r		(1)
			=	3 x 4		
			=	12 V		(1)
		power amplifier produces	=	12 + 8		(1)
			=	20 V		
	(iii)	Voltage gain of power amplifier	=	20 / 0.4		(1)
			=	50		(1)
(b)	(i)	Current input to power amplifier	=	0.4 / 1.6 k		(1)
			=	0.25 mA		(1)
	(ii)	pd lost across internal resistance of cell	=	1.9 - 0.4		(1)
			=	1.5 V		
		Internal resistance of solar cell	=	1.5 / 0.25		(1)
			=	6 k Ω		(1)

Question 3 Additional guidance for markers

a. i. Use of correct Power formula (may be implied) (1)
Correct response - 3A (1)

ii. Expected answer -
Formula for pd lost across internal resistance (1)
Correct response to pd (1)
Correct addition of pd's (1)

Alternative answer –
Resistance of motor – 2.7 ohms (1)
Total resistance - 6.7 ohms (1)
Correct use of resistance ratio (1)

Note: Allow incorrect current from a (i) for 2 marks

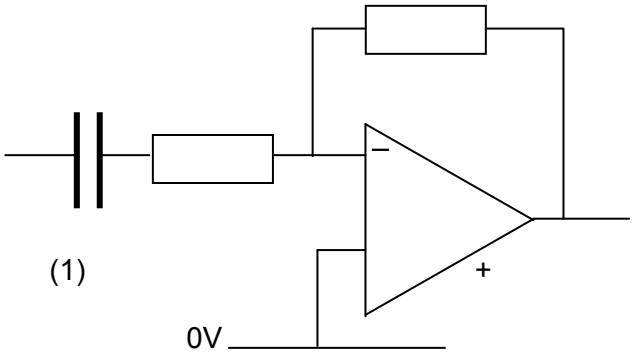
iii. Correct selection of ratio for voltage gain (1)
Correct calculation – 50 (1)
Allow 1 mark for use of Gain formula even if 8/0.4
Not worried about units for Gain

b. i. Correct selection of values for I calculation (1)
Correct answer - 0.25 mA or other suitable form (1)

ii. Correct pd loss across ir of call (1)
Correct use of ohms law with 1.5V (1)
Correct answer – 6 kohms (1)
Allow ecf of incorrect I from b. i. but correct use of 1.5V for 3 marks
Correct use of equation with incorrect 1.9 V value for 1 mark

Question 4

(a)

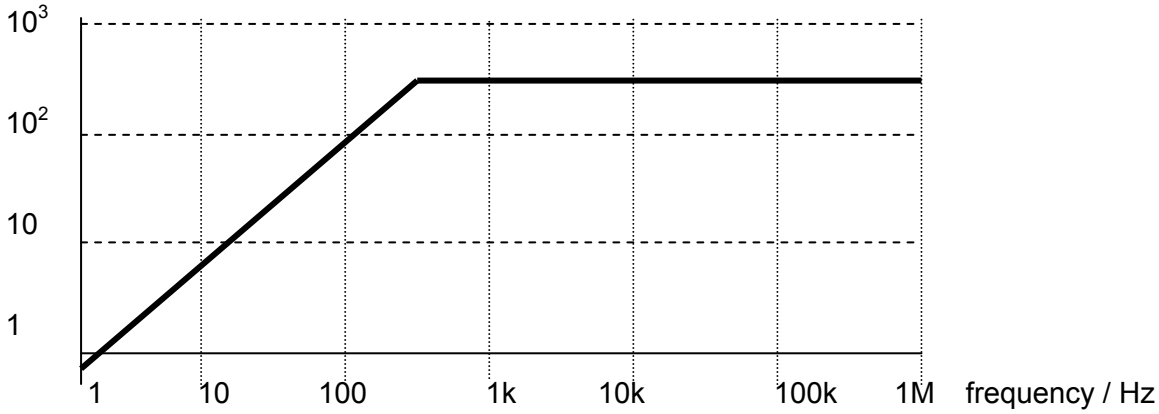


two resistors used correctly (1)
non-inverting input to 0V (1)
capacitor in series with input (1)

input resistor 2.7 k Ω (1)
voltage gain quoted as R_f / R_i (1)
R_f = 320 x 2.7 = 864 k Ω (1)

Break frequency quoted as 1 / 2πRC (1)
C = 1 / 2π x 2700 x 320 (1)
= 1.84 x 10^{-7} F
= 184 nF (1)

(b)



any bass cut shape (1)
break frequency at 320 Hz (1)
flat frequency response beyond 320 Hz (1)
power of 10 roll off below 320 Hz (1)

(c) no change in frequency response within gain-bandwidth product of 10^6 (1)
flat frequency response ends at about 3.2 kHz (1)
thereafter the gain rolls off to 1 at 1 MHz (1)

Question 4 Additional guidance for markers

a. As per expected mark scheme (9)
Correct calculation of Capacitor value allowed irrespective of positioning of capacitor in diagram
Allow input resistor values greater than 2.7k

b. As per expected mark scheme (4)

c. As per expected mark scheme (3)
Allow 1 mark for a repeat of a correct 4 b graph line

Question 5

(a) Integrator or Ramp generator (1)

(b) (i) V_{out} / time = - V_{in} / RC (1)

= - 5 / 220 x 10^3 x 22 x 10^{-6} (1)

= - 1.03 volt sec^{-1} (1)

(ii) The motor starts from rest and accelerates (backwards?) (1)
It continues getting faster and faster (linearly?) for 13 seconds (1)
At which point the output saturates (1)
So the motor continues running at top speed for a further 7 seconds (1)

(c) When input to circuit becomes zero the integrator freezes on its present output (1)
So the motor will continue to run at top speed (1)

(d) When S_1 is pushed the capacitor discharges more or less instantly (1)
(So the output rises from - 13V to 0V and the motor stops)
Because S_2 is set to 0V no further integration takes place so the motor stays off (1)

(e) Maximum voltage across motor will be in the order of ±13V (1)
So maximum current drawn from op-amp ≈ 130 mW / 13V ≈ 10 mA
(Exam Board 081 type) op-amp cannot deliver much more than 10 mA (1)

(f) Potential divider of two resistors drawn between +15V line and 0V
with junction connected to the +5V line (1)

Resistor values generate +5V as asked (1)
Resistor values at least 10 times lower than 220 k Ω (to avoid loading effect) (1)
Explanation of loading effect :
e.g. current drained by 220 k Ω input resistor should be significantly smaller than current in potential divider otherwise the input will drop below +5V. (1)

Question 5 Additional guidance for markers

a. Correctly identifies integrator / ramp generator (1)

b. i. Correct selection of formula (1)
Correct use of R and C values (1)
Minus sign required

ii. As per expected mark scheme (4)
Allow reference to saturation at 13V

c. As S2 goes to zero, then no further charging (1)
so V(out) remains at -13v and motor remains at that speed (1)

d. S1 discharges capacitor so V(out) rises by 13V to 0V (1)
Motor stops as input at S2 is zero so no integration (1)

e. Calculation to indicate max I for motor is approx 10mA (1)
Reference to max current for TL081 being 10mA (1)

f. i. Correct positioning of potential divider (1)

ii. As per mark scheme (3)
R values <<220 kohms to avoid large current to op amp and
Reduction of pd below 5V

Question 6

(a) *Saturation* When the output voltage tries to exceed op-amp power supplies
or when output has (approx) reached supply line and can go no further (1)

Virtual earth When not saturated the two op-amp input voltages are almost identical
Because of the huge open loop gain (or due to negative feedback)
And as + input is wired to 0V the - input must be approx 0V also
P is virtual because it is not a current source or sink (any) (1) (1)

(b) (i) pd across top 10k resistor is 0.5V (0.5 at one end and 0V at other end)
Similarly, pd across lower 10k is 0.2V (1)

Current from V_1 in 10k resistor = 0.5 / 10k = 50 μA
Current from V_2 in 10k resistor = 0.2 / 10k = 20 μA (1)
These currents add and as no current enters op-amp input it must all enter
feedback resistor.

(ii) Output voltage V_{out} = I R = 70 μA x 100 k = 7V (1)
and is -ve because the op-amp output is sinking this current (or wtte) (1)

(c) In general, the current in the feedback resistor is the vector sum of the currents in the two input resistors

$I_1 + I_2 = I_{feedback}$ (1)

$(V_1 - 0) / 10k + (V_2 - 0) / 10k = (0 - V_{out}) / 100k$ (1)

$V_{out} = - 100k (V_1 / 10k + V_2 / 10k)$

$= - 10 (V_1 + V_2)$ (1)

(d) Voltmeter connected directly across either battery can only measure terminal pd to nearest volt so it cannot detect small differences
Batteries are connected with a common 0V line to make V_1 -ve and V_2 +ve
(1)
Circuit now operates according to $V_{out} = 10 (V_1 - V_2)$
(1)
So any difference in terminal pd is magnified tenfold and should allow the voltmeter to be read
(1)

Question 6 Additional guidance for markers

a. Saturation – As per mark scheme (1)
Do not allow reference to "+-13V" without explanation

Virtual Earth - As per mark scheme (2)
Allow reference to high resistance of op amp input
Explanation required not just a statement

b. i. As per mark scheme (4)
Alternative –
Allow use of voltage summer formula (1)
Correct values selected and used (1)
Correct answer (1)
Comment relating to no current entering op amp (1)

ii. As per mark scheme (2)

c. As per mark scheme (3)
"Show" requires use of formula plus V and R values
Providing voltage summer formula with no explanation (1)

d. As per mark scheme (3)

Question 7

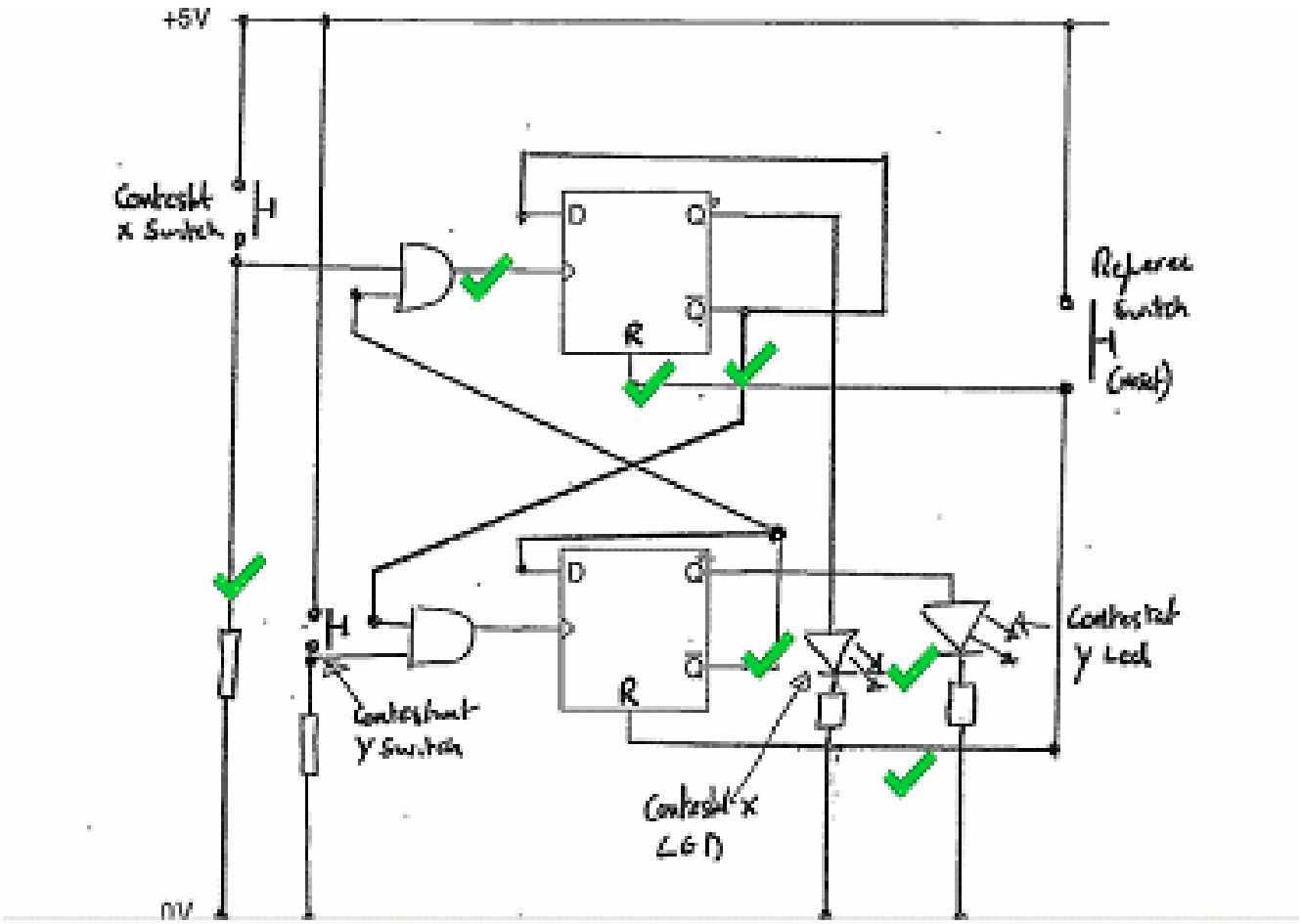
Referee push button + resistor across power lines	(1)
Referee junction correctly connected to both Resets of D-types	(1)
X push button + resistor across power lines Y push button + resistor across power lines	(1)
X junction correctly connected to clock input of D-type Y junction correctly connected to clock input of D-type	(1)
NOT Q from X's D-type correctly connected to D input of Y's D-type	(1)
NOT Q from Y's D-type correctly connected to D input of X's D-type	(1)
Q outputs connected to LEDs + resistors to 0V (or NOT Q to +5V)	
LEDs correctly labelled from corresponding contestant push buttons	(1)

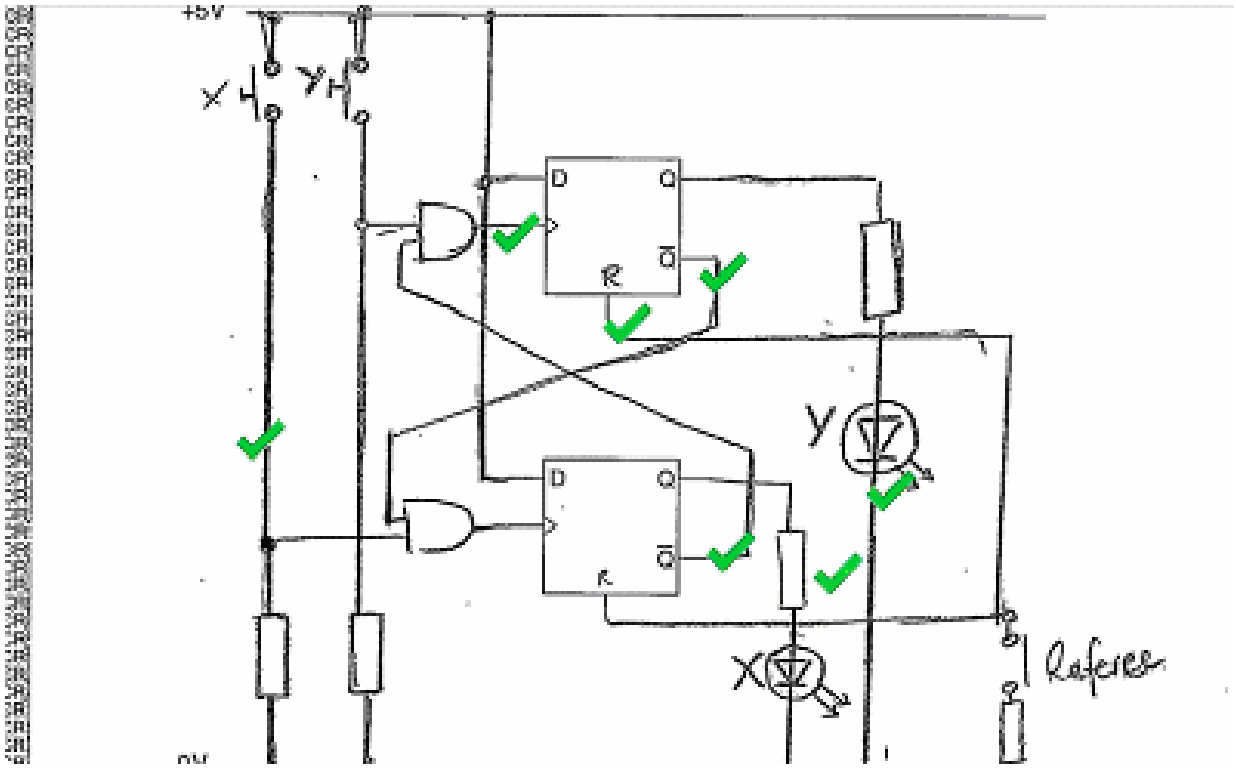
Question 7 Additional guidance for markers

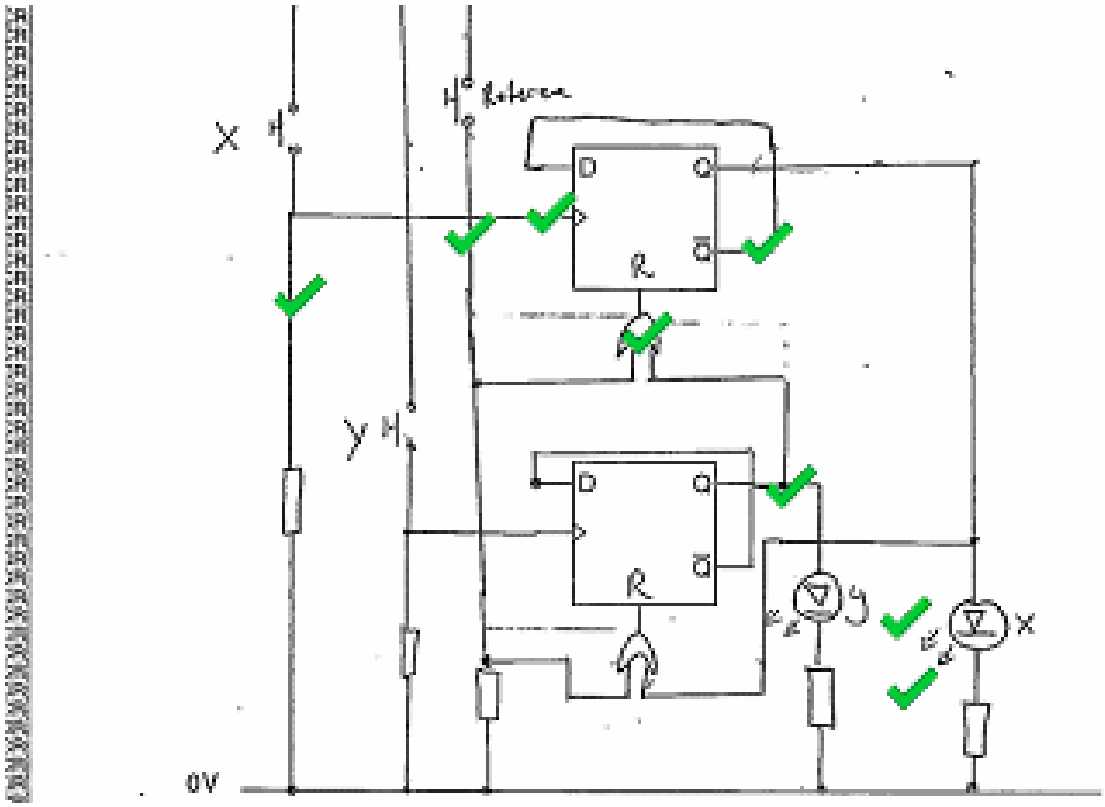
As per mark scheme (8)
Allow resets of D-types being "active low" and therefore "referee" switch and potential divider resistor positions could be reversed.

Allow 1 mark for X and Y push buttons and pull down resistors
Allow 1 mark for correct connections of both X and Y to clocks

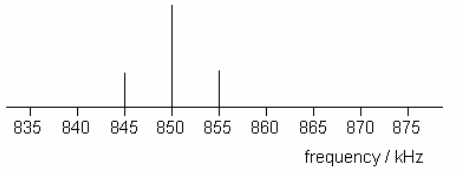
Examples of alternative solutions

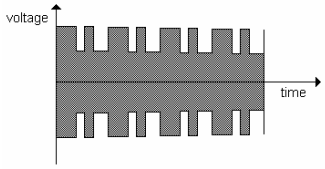
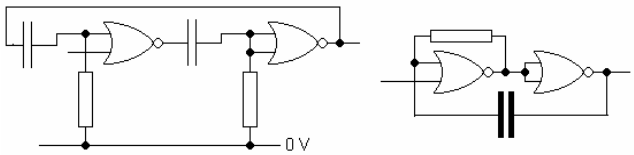


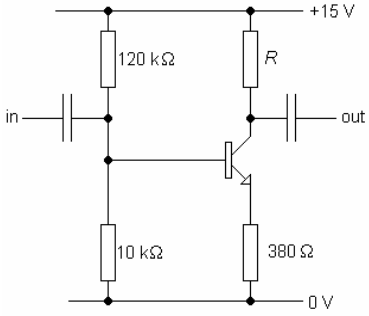

+5V
X
Y
D
Q
R
Y
X
Referee
0V

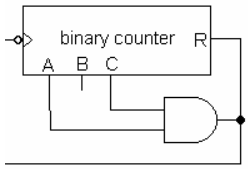
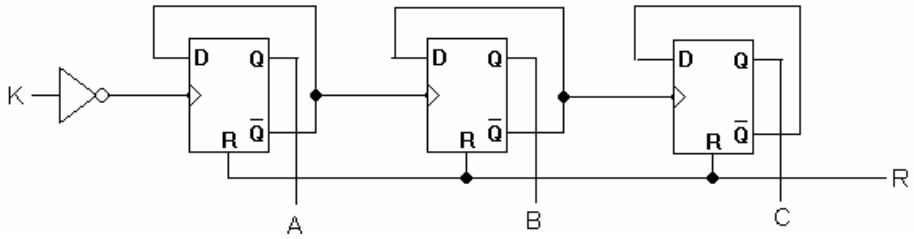

X
Referee
D
Q
R
Y
0V

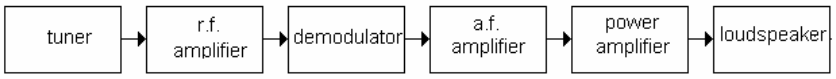
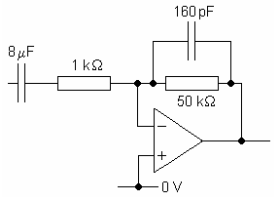
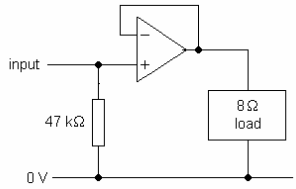
2529 Communications Circuits

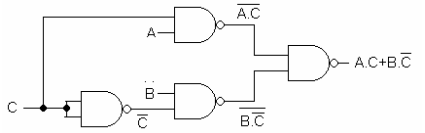
question	grade	expected answer	mark
1ai	BCD	$f_0 = \frac{1}{2\pi\sqrt{LC}}$ (eor)	1
	DE	correct units conversion: $L = 470\times10^{-6}$ H, $C = 91\times10^{-12}$ F	1
	AB	no ecf: $f_0 = 1 / 2\pi\ (470\times10^{-6} \times 91\times10^{-12})^{1/2} = \underline{7.7}\times10^5$ Hz (NOT 7.6)	1
1aii	DE	tuned circuit has large impedance/reactance/resistance	1
	DE	at frequencies close to 800 kHz / resonant frequency	1
	BCD	only (alternating) current in the aerial at those frequencies	1
	AB	sets up an (alternating) voltage at G	1
1aiii	DE	any pattern with correct symmetry, peaking at 850	1
	DE	pattern extends from 845 to 855 only	1
	BCD	pattern is three spikes separated by 5 kHz	1
			
1b	DE	higher input resistance (impedance) / draws less current (power)	1
	BCD	any two of the following, [1] each:	2
	AB	• raising Q of tuned circuit • increasing sensitivity / increasing signal • increasing selectivity / smaller bandwidth	
1ci	DE	SHOW: $I = V/R$	1
	DE	V = -3 - (-15) = 12 V	1
	BCD	ecf incorrect V : $I = 12/2.2\times10^3$	1
	BCD	$I = \underline{5.5}\times10^{-3}$ A (ACCEPT 5.5 / 5.4 mA)	1
1cii	DE	$V = IR$ (eor)	1
	DE	voltage drop = $5.5\times10^{-3} \times 2.2\times10^3$ = 12.1 V	1
	AB	so voltage at D = 15 - 12.1 = 2.9 V	1
		5.4 mA gives 3.1 V 6 mA gives 1.8 V ACCEPT 3 V	
1d	DE	increasing voltage at gate increases source / drain current	1
	BCD	so more voltage drop across drain resistor	1
	AB	(top of drain resistor fixed) so drain goes down in voltage. ACCEPT reverse argument	1

question	grade	expected answer	mark
2ai	DE BCD	any two of the following, [1] each • higher quality transmission of signals / better SNR • because noise can be removed • by a Schmitt trigger • can be encoded / compressed • to speed up transmission / give smaller file	2
2aii	DE BCD	any two of the following, [1] each • less bandwidth required • more channels available • less distortion • simpler circuitry • cheaper	2
2bi	DE	amplitude modulated carrier	1
	DE	square wave modulation (ACCEPT 100% modulation)	1
	DE	higher frequency carrier (ACCEPT shading)	1
			
2bii	DE	each word needs start and stop bits	1
	DE	ecf: <u>bit rate</u> = $10 \times 10 \times 10^3$ = 100 kbits per second (8 bits = 80 kbps)	1
	BCD	signal for widest spread of sidebands is 101010101	1
	AB	maximum modulation frequency therefore 50 kHz	1
	AB	sidebands at $\pm$50 kHz	1
2c	DE	correct circuit	3
	DE	[-1] per error or omission, minimum [0]	
	AB	R at least 10 kΩ	1
	BCD	RC between 2×10^{-4} s and 5×10^{-5} s	1
			
2d	DE		
	BCD	shift register in any box	1
	DCB	shift register anywhere before DAC	1
		DAC anywhere before filter	1

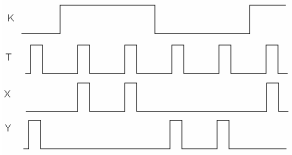
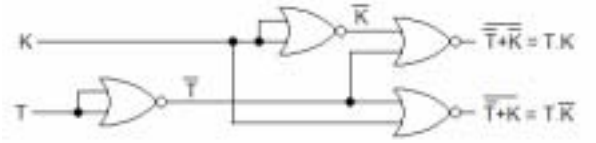
question	grade	expected answer	mark
3a	DE	correct output capacitor	1
	DE	correct input capacitor	1
	DE	input and output labelled	1
			
3b	DE	SHOW: $I = V/R$	1
	DE	R = 130 kΩ	1
	DE	ecf R: $I = 15/130\times10^3 = 1.15\times10^{-4}$ A (ACCEPT 120 μA or 0.12 mA)	1
	BCD	ecf I: $V = IR = 1.15\times10^{-4} \times 10\times10^3 = 1.2$ V	1
		NOT alternative method	
3c	DE	SHOW: $I = V/R$	1
	BCD	V = 1.2 - 0.7 = 0.5 V 1.0 V gives 0.3 V	1
	DE	ecf incorrect V: I = 0.5 / 380 = 1.3 mA	1
		1.15 V gives 1.2 mA 1.0 V gives 0.79 mA	
3di	DE	halfway between supply rails	1
	BCD	alllows large amplitude output signal (owtte)	1
3dii	DE	$R = V/I$ (eor)	1
	DE	ecf incorrect I: $R = 7.5 / 1.3\times10^{-3}$	1
	DE	R = 5700 Ω	1
		1.2 mA gives 6.25 kΩ 1.15 mA gives 6.5 kΩ	
		0.79 mA gives 9.5 kΩ 1 mA gives 7.5 kΩ	
3diii	BCD	$G = -R_c/R_e$ (eor)	1
	BCD	ecf incorrect R_c: G = - 5700/380 = (-)15	1
	AB	negative sign	1

question	grade	expected answer	mark
4a	DE	correct symbol for AND gate	1
	DE	inputs to A, C	1
	DE	output to R	1
			
4b	DE	D to Q-bar three times	1
	BCD	Q-bar to next clock twice	1
	DE	outputs A, B, C labelled correctly	1
	DE	reset and clock inputs labelled appropriately	1
	AB	NOT gate before first clock	1
	AB	all blobs or bridges as required	1
			
4c	DE	A before D	1
	BCD	D before F	1
	BCD	F before E	1
	AB	E before B	1
		all diodes feel extremely bad	
4d	DE	0 shows that word transmission has started	1
	AB	1 resets line so that subsequent start bit can be recognised (owtte)	1
		ACCEPT allows receiver to detect start of the word for [1]	
		NOT just start and stop bits	
	DE	$6 \times 6.8 \times 10^6 = 4.1 \times 10^7$ (Hz) [1]	2
	BCD	$6 \times 512 \times 10^3 = 3.1 \times 10^6$ (Hz) [2]	

question	grade	expected answer	mark
5a	DE	r.f. amplifier before a.f. amplifier	1
	DE	a.f. amplifier before power amplifier	1
	BCD	power amplifier before loudspeaker	1
			
5b	DE	$f_0 = 1/2\pi RC$ (eor)	1
	DE	$RC = 8\times10^{-3}$ s for bass cut filter	1
	DE	$RC = 8\times10^{-6}$ s for treble cut filter	1
	BCD	all R between 1 kΩ and 10 MΩ	1
	DE	overall midband gain 50	1
	AB	bass cut filter circuit	1
	AB	treble cut filter circuit	1
			
		ACCEPT two stage circuit	
5ci	AB	negative feedback to give voltage gain of 1	1
	BCD	input to non-inverting terminal (ignore 47 kΩ in series)	1
	DE	ecf: input resistance of 47 kΩ	1
			
5cii	DE	$V_0 = \sqrt{2} \times V_{rms}$ (eor)	1
	DE	$V_0 = 1.414 \times 9 = \underline{12.7}$ V	1
5ciii	DE	SHOW: $I = V/R$	1
	BCD	ecf V: $I = 12.7 / (4 + 8) = 1.06$ A	1
	AB	$V = IR = 1.06 \times 8 = \underline{8.5}$ V	1
		13 V gives 8.7 V	
		ACCEPT use of voltage divider formula / idea	
		stated rule [1], substitution [1], answer [1]	
5civ	DE	$P = VI$ (eor) or V^2/R (eor)	1
	DE	ecf I, V: $P = 8.5 \times 1.06 = 9.0$ W	1

question	grade	expected answer	mark
6a	DE	more than one signal / channel	1
	DE	sent down a single link	1
	BCD	by allowing each signal / channel access to the link for short times	1
6bi	DE	De Morgan's Theorem:	1
	BCD	correct use e.g. $T=\overline{(\overline{A.C})}+\overline{(\overline{B.\overline{C}})}+\overline{(\overline{A.B})}$	1
	AB	Race Hazard Theorem: $T=(A.C)+(B.\overline{C})+(A.B)=(A.C)+(B.\overline{C})$	1
6bii	DE	NAND gate to generate NOT C	1
	BCD	NAND gates to generate inverse of each term	1
	BCD	NAND gate to generate output	1
	AB	correct algebra at output of each gate, e.g.  full marks for any NAND gate circuit which works and is justified ignore blobs or bridges	1
6ci	DE	all four combinations of TK	1
	DE	X correct	1
	DE	Y correct	1

T	K	X	Y
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	0

6cii	DE	X correct (by eye)	1
	DE	Y correct (by eye) 	1
6cii	DE	NOR to generate NOT K (and NOT T) - including one input low	1
	BCD	correct NOR gate circuit for X	1
	BCD	correct NOR gate circuit for Y	1
	AB	truth table or algebra showing outputs of all gates e.g.  IGNORE number of gates used.	1

Quality of Written Communication

3 The candidate expresses complex ideas extremely clearly and fluently. Sentences and paragraphs follow on from one another smoothly and logically. Arguments are consistently relevant and well structured. There will be few, if any, errors of grammar, punctuation and spelling.

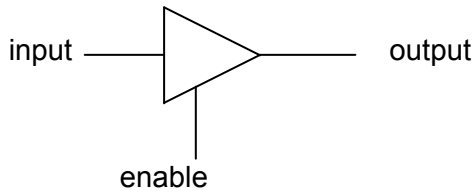
2 The candidate expresses straightforward ideas clearly, if not always fluently. Sentences and paragraphs may not always be well connected. Arguments may sometimes stray from the point or be weakly presented. There may be some errors of grammar, punctuation and spelling, but not such as to suggest a weakness in these areas.

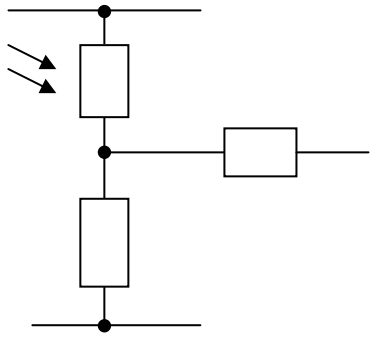
1 The candidate expresses simple ideas clearly, but may be imprecise and awkward in dealing with complex or subtle concepts. Arguments may be of doubtful relevance or obscurely presented. Errors in grammar, punctuation and spelling may be noticeable and intrusive, suggesting weaknesses in these areas.

0 The language has no rewardable features.

2530 Control Circuits

Question	Expected answer		Mark
1 (a)	Program counter	Register inside the microprocessor	[1]
		Holds address of next memory location to be accessed Is normally incremented by one to move through memory Can be loaded with new memory location for Jumps (any two) (1)(1)	[2]
(b)	Accumulator	Register inside the microprocessor	[1]
		Holding data which can be processed/controlled	[1]
(c)	Look-up table	Area of memory	[1]
		Where only data is stored	[1]
(d)	Arithmetic Logic Unit	Circuitry inside microprocessor	[1]
		Carries out any logic functions or arithmetic processing	[1]

Question			Expected answer	Mark
2	(a)	(i)	E = logic 1	[1]
			Because OR / NOR gates are frozen with a logic 1 input or because this produces a logic 0 output from both NOR gates	[1]
		(ii)	The output floats	[1]
			because it is not connected to any power line/no defining voltage	[1]
	(b)		To energise a relay there must be a logic 1 at the NOR output	
			Logic 1 output is only produced by both inputs being logic 0	[1]
			The inverter from D means there can never be a double logic 0 at inputs	[1]
	(c)		To energise relay 1 there must be two logic 0s at the NOR inputs	[1]
			Thus E = 0 and D = 1	[1]
	(d)	(i)	Tristate,	[1]
		(ii)	 allow ECF from d(i) (ignore any inversion circles) (1) (1)	[2]
		(iii)	It allows multiplexing where multiple users can share the same data line for economy of tracking/wiring (1) (1)	[1]

Question	Expected answer	Mark
3 (a)	Maximum resistance R_1 = 24V / 30mA	[1]
	= 800 Ω	[1]
(b)	Motor current = 100W / 24V	[1]
	= 4.2 A	[1]
	Current rating for T_2 ≥ 5A	[1]
(c) (i)	Maximum R_2 = 24V / 4mA = 6 k Ω	[1]
	Maximum R_3 = 24V / 50mA = 480 Ω	[1]
(d)	Pressing S_1 allows a current in excess of minimum 30mA in gate to fire T_2	[1]
	Once fired, the gate ceases to have any effect so the switch S_1 can be released	[1]
(e)	Before pressing S_2 when T_1 is still conducting, plate A = +24V plate B ≈ 0V	[1]
	Pressing S_2 allows a current in excess of minimum 4mA in gate to fire T_2. Thus plate A falls rapidly to ≈ 0V Thus plate B also falls rapidly to ≈ - 24V	[1]
	Triac T_1 is thus momentarily deprived of its main current so it switches off	[1]
(f)	 Any potential divider with LDR	[1]
	LDR in correct position	[1]
	Junction connected to R_2	[1]
(g)	Once fired by the gate, the triac cannot be turned off by the same initiation or once fired the triac latches (or wtte)	
	Hence very limited use eg burglar alarms	
	In ac circuits the supply is constantly returning to zero hence triac is constantly turned off every half cycle (any two) (1) (1)	

Question	Expected answer	Mark
4 (a)	*Isolation* This means there is no electrical connection between the two circuits or the power supply for A has no reference whatsoever to that of B (or wtte)	[1]
(b) (i)	Transformer	[1]
(ii)	Changing current or voltage from A in primary coil creates variations Variation induce /create varying current or voltage in B Changing magnetic flux generates induced emf in secondary coil to B (allow 1 mark for a simple explanation of an ac input generating an ac output)	[1] [1]
(c) (i)	Optoisolator or Optocoupler or optotransistor	[1]
(ii)	Current from A generates light emission from LED Light falls on phototransistor and generates current in circuit B	[1] [1]
(d)	The transformer in Fig 4.1 can only transmit wobbly/ac signals and generally within a fairly limited bandwidth The optoisolator in Fig 4.2 can transmit dc signals or ac signals and generally over a fairly broad bandwidth Include signal size;include voltage range Difference between -1 mark Explanation of difference -1mark	[1] [1]

Question	Expected answer	Mark
5 (a)	Total number of address locations = $2^{\text{number of address pins}}$	[1]
	$8192 = 2^n$	[1]
	$n \log 2 = \log 8192$	[1]
	$n = 13$	
(b)	Total number of memory cells = total addresses x number of data pins	
	number of data pins = 131072 / 8192	
	= 16	[1]
	Allow ECF from (a)	
(c)	Address information on bus can only flow one way into chip from µP	[1]
(d)	Data can flow into or out of the chip so flows both ways on data bus	[1]
(e)	Address bus must be set up with the location of memory store in RAM	[1]
	The R / $\overline{W}$ = logic 0 and the chip is in WRITE mode	[1]
	the data to be stored is placed on the data bus by µP or peripheral	
	The Enable pin is pulsed low and the data word is swallowed and stored	[1]
	The R / $\overline{W}$ = logic 1 and the chip is in READ mode	[1]
	The Enable pin is made logic 0	
	the data stored at the active address is placed on the data bus in order to exit RAM and travel to µP or peripheral for use.	[1]
	Alternative Correct Sequence 1mark R= 1 read (1) $\overline{E}$=0 enable (1) W=0 write (1) Address first (1)	

Question	Expected answer			Mark
6 (a)	**Address**	**Contents**	**Explanation**	**[1]**
	00	3E 00	Accumulator = 00	
	02	32 AA	Move 00 to memory location AA	
	04	32 BB	Move 00 to memory location BB	**[1]**
	06	3E 03	Accumulator = 03	
	08	32 FF	Output 03	**[1]**
	Summary	Clear contents of memory locations AA and BB		**[1]**
		Then unfreeze D-types		
		And display zero on both 7-segment displays		**[1]**
		Keeps LED off		
		(any 2 for 2marks)		
(b)	**Address**	**Contents**	**Explanation**	
	0A	3A EF	Swallow input port	**[1]**
	0C	E6 80	Mask for test switch only	**[1]**
	0E	CA 0A	If zero, go back and input again	**[1]**
	10	3E 00	Accumulator = 00	
	12	6F	X register = 00	**[1]**
	13	C9	increment X register	
	14	7D	Move X contents to Accumulator	
	15	C2 13	(all for 1 mark)	**[1]**
			If not yet zero, return to increment X	
	17	C3 30	further	**[1]**
			jump to address 30	
			(not load Pc with 30)	
	Summary	Wait until the test switch has been pushed		**[1]**
	Then execute a short time delay			**[1]**
(c)	**Address**	**Contents**	**Explanation**	
	30	3E 40	Accumulator = 40	**[1]**
	32	32 FF	Output 40	
	34	3A EF	Swallow input	
	36	E6 11	Mask for A or B inputs only*	
	38	CA 34	if still zero go back and input again	**[1]**
			(all for 1 mark)	
	3A	E6 10	Mask for A alone	
	3C	C2 50	if A's button is pressed go to	
			address 50	**[1]**
	3E	C3 60	if not A then must be B so go to 60	
			(all for 1 mark)	
			*key point for the mark	
	Summary	This section lights up the LED		**[1]**
		Unfreezes the D-types		
		Blanks out both 7-segment displays		**[1]**
		Then it waits for either A or B to press their switch		**[1]**
		If A has won then got to address 50 otherwise go to		
		address 60 for B win		**[1]**

Question	Expected answer			Mark
(d)	**Address**	**Contents**	**Explanation**	
	50	3A AA	Accumulator = A's current score	
	52	C6 04	Increment A's score by one	
	54	32 AA	and save new score back in memory AA	**[1]**
	56	C3 70	go to address 70 (all for 1 mark)	
	60	3A BB	Accumulator = B's current score	
	62	C6 04	Increment B's score by one	
	64	32 BB	and save new score back in memory BB	
	66	C3 70	go to address 70	
	Summary	This section either increments A's score by one point Or it increments B's score by one point After which it jumps to address 70		**[1]** **[1]**
(e)	**Address**	**Contents**	**Explanation**	
	70	3E 80	Accumulator = 80	
	72	32 FF	Output	
	74	3A AA	Accumulator = A's current score	
	76	C6 02	Add 02	**[1]**
	78	32 FF	Output	
	7A	3A BB	Accumulator = B's current score	
	7C	C6 01	Add 01	
	7E	32 FF	Output	
	80	3A EF	Swallow input port	
	82	E6 80	Mask for test switch only	
	84	CA 74	If test zero go back to output score of A then B	**[1]**
	86	C3 10	If test positive, go back to time delay sequence	
	Summary	This section resets all three D-types Then it takes A's current score and adds 02 (ie logic 1 to activate A's display) **Then it lights up A's display while that of B is blanked. (and at the same time unfreezes the D-types)** **Then it takes B's current score and adds 01 (ie logic 1 to activate B's display)** **Then it lights up B's display while that of A is blanked. (and still unfreezes D-types)** **Then it swallows the input to see if the referee has pressed the test switch.** **If not then it returns to the loop of flashing A's score and then flashing B's score after each check on the test switch.**		**[1]** **[1]** **[1]**

Question	Expected answer	Mark
	Once the referee has pressed the test switch the program jumps back to address 10 Alternative applies to bold type Adds 02 to A and explains why and display or wtte(1) Adds 01 to B and explains why display or wtte A and B displayed alternately (1)	**[1]** **[1]**

Grade Thresholds

Advanced GCE Electronics 3826 7826
June 2008 Examination Series

Unit Threshold Marks

Unit		Maximum Mark	A	B	C	D	E	U
2526	Raw	120	86	77	69	61	53	0
	UMS	120	96	84	72	60	48	0
2527	Raw	90	59	52	45	39	33	0
	UMS	90	72	63	54	45	36	0
2528	Raw	78	61	54	47	40	33	0
	UMS	90	72	63	54	45	36	0
2529	Raw	120	87	78	69	61	53	0
	UMS	120	96	84	72	60	48	0
2530	Raw	90	65	59	53	47	41	0
	UMS	90	72	63	54	45	36	0
2531	Raw	90	71	64	58	52	46	0
	UMS	90	72	63	54	45	36	0

Specification Aggregation Results

Overall threshold marks in UMS (ie after conversion of raw marks to uniform marks)

	Maximum Mark	A	B	C	D	E	U
3826	**3826**	300	240	210	180	150	120
7826	**7826**	600	480	420	360	300	240

The cumulative percentage of candidates awarded each grade was as follows:

	A	B	C	D	E	U	Total Number of Candidates
3826	22.8	36.7	55.3	69.7	83.1	100	699
7826	32.1	52.5	72.8	86.5	96.1	100	421

1120 candidates aggregated this series

For a description of how UMS marks are calculated see:
http://www.ocr.org.uk/learners/ums_results.html

Statistics are correct at the time of publication.

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