OCR
RECOGNISING ACHIEVEMENT

ADVANCED GCE **2529**

ELECTRONICS

Communication Circuits

TUESDAY 10 JUNE 2008 Afternoon

Time: 1 hour 30 minutes

Candidates answer on the question paper
Additional materials (enclosed): None

Additional materials (required):
Calculator

CUP/T44950

Candidate Forename		Candidate Surname	
Centre Number		Candidate Number	

INSTRUCTIONS TO CANDIDATES

- Write your name in capital letters, your Centre Number and Candidate Number in the boxes above.
- Use blue or black ink. Pencil may be used for graphs and diagrams only.
- Read each question carefully and make sure that you know what you have to do before starting your answer.
- Answer **all** the questions.
- Do **not** write in the bar codes.
- Write your answer to each question in the space provided.

INFORMATION FOR CANDIDATES

- The number of marks for each question is given in brackets [ ] at the end of each question or part question.
- The total number of marks for this paper is **120**.
- You may assume, unless otherwise stated, that:
  - **(i)** the p.d. across a forward-biased silicon diode is 0.70V,
  - **(ii)** the power supplies for operational amplifiers are +15V and –15V,
  - **(iii)** the saturation levels for operational amplifiers are +13V and –13V,
  - **(iv)** logic 1 = 5V and logic 0 = 0V.
- The quality of written communication will be assessed in your answers to all questions.

FOR EXAMINER'S USE	
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2	
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4	
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6	
QWC	
TOTAL	

This document consists of **14** printed pages and **2** blank pages.

[Turn over

1 The circuit of Fig. 1.1 is part of a radio receiver for the MW band.

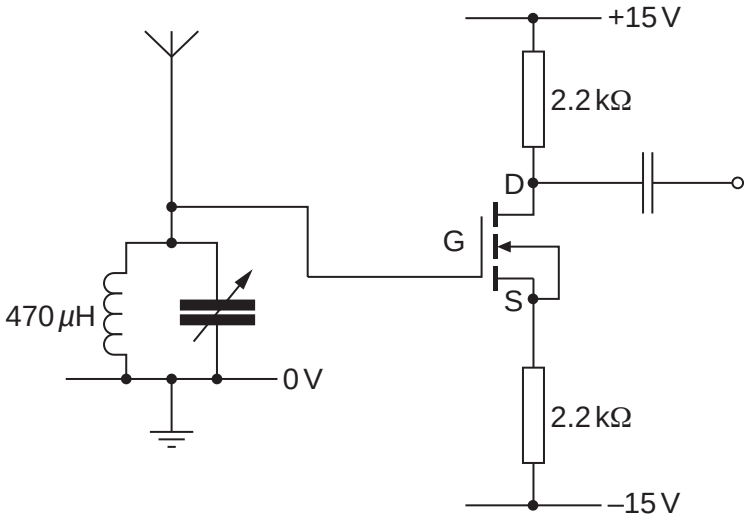

Fig. 1.1

(a) The variable capacitor is set to 91 pF.

(i) Show that the receiver is tuned to a station broadcasting at a frequency of about 800 kHz.

[3]

(ii) Explain how the parallel tuned circuit selects just one station out of the many broadcasting on the MW band.

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.....[4]

(iii) One station broadcasts on 850 kHz. The carrier is amplitude modulated by a test signal at 5 kHz. On Fig. 1.2, draw an amplitude-frequency graph for the amplitude modulated carrier.

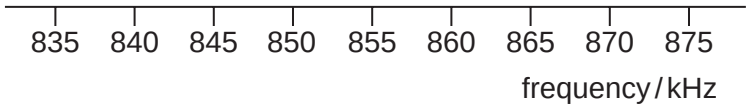

Fig. 1.2

[3]

(b) The signal from the tuned circuit is processed by a MOSFET amplifier.

Explain the advantage of using a MOSFET amplifier instead of an NPN transistor amplifier.

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.....

.....[3]

(c) When there is no signal at G, S is at –3 V.

(i) Show that the source current of the MOSFET is about 6 mA.

[4]

(ii) Calculate the voltage at D.

voltage = ... V [3]

(d) Explain why the MOSFET amplifier of Fig. 1.1 has a voltage gain which is negative.

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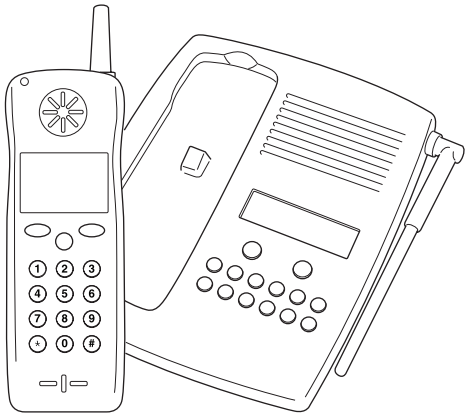
.....[3]

2 A cordless telephone uses a digital format for the wireless exchange of signals between the handset and the base station.



(a) (i) Explain one advantage of sending wireless signals in **digital** format.

.....

.....

.....[2]

(ii) Explain one advantage of sending wireless signals in **analogue** format.

.....

.....

.....[2]

(b) The handset converts the signal from the microphone into an eight-bit word. This digital signal is amplitude modulated in serial form onto a radio-frequency carrier.

(i) On Fig. 2.1, sketch a voltage-time graph of a digital signal which is amplitude-modulated onto a high frequency carrier.

Fig. 2.1

[3]

(ii) The signal from the microphone is sampled at a rate of 10 kHz. Explain why the bandwidth required to transmit the digital signal in **serial** form is about 100 kHz.

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.....

.....[5]

(c) On Fig. 2.2, show how an astable with a frequency of 10 kHz can be made from NOR gates, resistors and capacitors. Show all component values and justify them.

Fig. 2.2

[5]

(d) The base station uses a radio receiver to recreate the serial digital signal. This is used to recreate the original microphone signal for transmission down the telephone line. Fig. 2.3 shows a simple incomplete block diagram for the base station.

Fig. 2.3

Complete the block diagram. Choose from

ADC **counter** **DAC** **filter** **shift register** **monostable** [3]

3 The circuit of Fig. 3.1 shows an NPN transistor arranged as an incomplete a.c. amplifier.

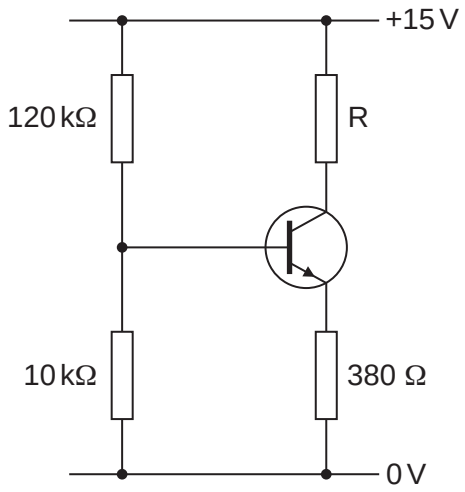

Fig. 3.1

(a) Draw on Fig. 3.1 to show how capacitors should be used to allow a.c. signals into and out of the amplifier. Label the input and output terminals. [3]

(b) By calculating the current in the 120 kΩ resistor, show that the base of the transistor is held at about +1 V by the 120 kΩ and 10 kΩ resistors.

Assume that the base current of the transistor is negligible.

[4]

(c) Show that, in the absence of an a.c. signal, the emitter current is about 1 mA.

[3]

(d) The value of the resistor R is not shown in Fig. 3.1.

(i) Suggest why R should be chosen to set the collector at 7.5V in the absence of an a.c. signal.

.....

.....

.....[2]

(ii) Calculate a value of R which sets the collector at +7.5V.

resistance = ...Ω [3]

(iii) Calculate the voltage gain of the amplifier for this value of R.

gain = ...[3]

4 The incomplete circuit of Fig. 4.1 shows a serial transmitter of four-bit words.

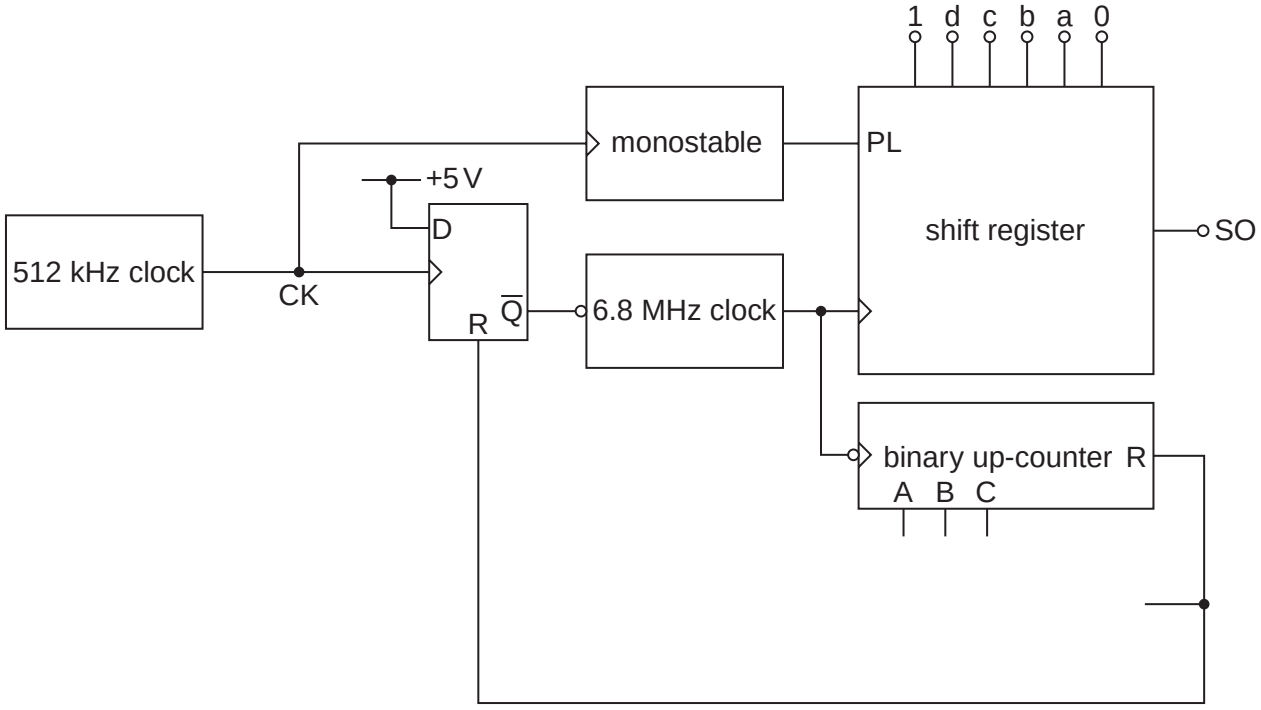

Fig. 4.1

(a) The binary up-counter has to reset on the fifth falling edge from the 6.8 MHz clock.

On Fig. 4.1, show how this can be done with a logic gate. [3]

(b) On Fig. 4.2, show how the binary up-counter can be assembled from D-type flip-flops and a NOT gate.

Label all the inputs and outputs.

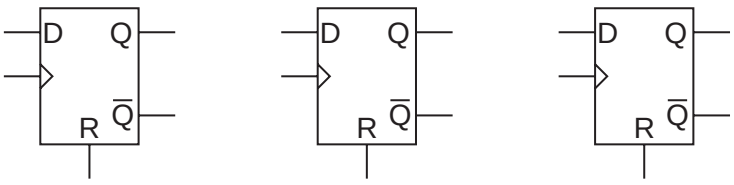

Fig. 4.2

[6]

(c) The sentences describe how the circuit operates. They are in the wrong order.

A	The monostable is triggered.
B	The D-type flip-flop is reset by the logic gate.
C	A rising edge from CK sets the D-type flip-flop.
D	The six-bit word is loaded into the shift register.
E	The six-bit word appears at SO, one bit at a time.
F	Clock pulses from the 6.8 MHz clock enter the shift register.

Show the correct order by putting the letters **A**, **B**, **C**, **D**, **E** or **F** in the boxes.

The first one has been done for you.

C					

[4]

(d) The word loaded into the shift register is **1dcba0**, where **d c**, **b** and **a** can be 1 or 0.

Explain the significance of the **0** and **1** at either end of the word.

.....

.....

.....[2]

(e) Calculate the number of bits which appear at SO in one second.

bits per second = ...[2]

5 The incomplete block diagram of Fig. 5.1 is for a radio receiver.

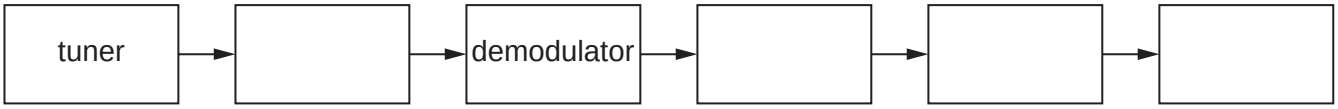

Fig. 5.1

(a) Complete the block diagram. Choose from the list.

a.f. amplifier **loudspeaker** **power amplifier** **r.f. amplifier** [3]

(b) The a.f. amplifier has the gain-frequency graph shown in Fig. 5.2.

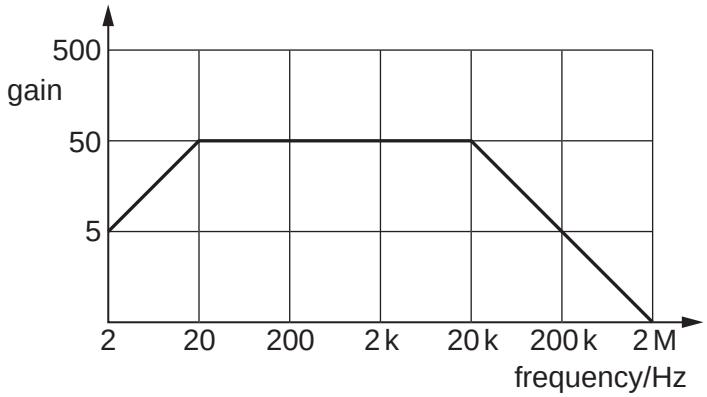

Fig 5.2

Draw in the space below to show how the a.f. amplifier can be made from op-amps, resistors and capacitors. Show all component values. Justify them with calculations.

[7]

(c) The power amplifier uses the op-amp of Fig. 5.3 which can deliver currents of up to 2 A at its output.

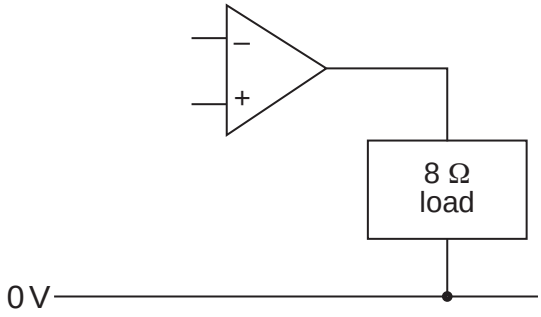

Fig. 5.3

(i) Draw on Fig. 5.3 to show how the op-amp should be connected to have a voltage gain of +1 and an input impedance of 47 kΩ. Label the input. [3]

(ii) A test signal of amplitude 9.0 V rms is applied to the input of the power amplifier. Show that the peak voltage of this signal is about 13 V.

[2]

(iii) The output impedance of the op-amp is 4 Ω.

Show that the peak voltage across the 8 Ω load is about 9 V.

[3]

(iv) Calculate the peak power delivered to the load by the op-amp when the 9 V rms test signal is applied to its input.

peak power = ... W [2]

6 Fig. 6.1 shows a simple time-division multiplexing system for digital signals.

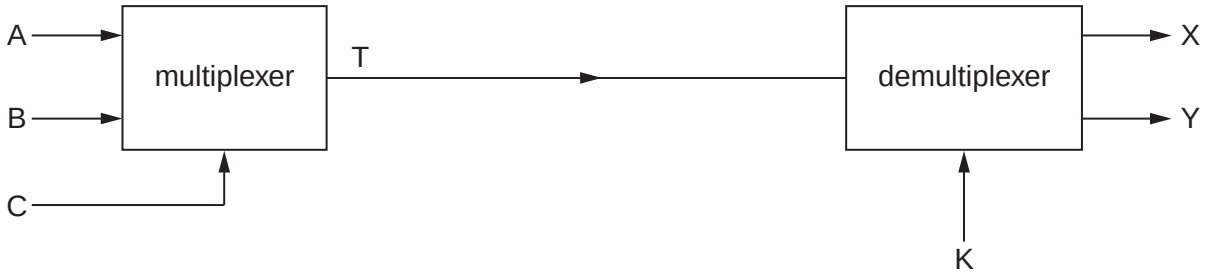

Fig. 6.1

(a) Describe what is meant by **multiplexing** and state how **time-division** multiplexing works.

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.....

.....[3]

(b) The multiplexer obeys the expression $T = \overline{(\overline{A.C})}.\overline{(B.\overline{C})}.\overline{(\overline{A.B})}$.

(i) Use the theorems of Boolean Algebra to show that $T = A.C + B.\overline{C}$.

Name the theorem used for each step.

[3]

(ii) In the space below, show how the multiplexer can be assembled from NAND gates. Label the output of each gate with its Boolean expression.

[4]

(c) The demultiplexer obeys these expressions:

$$X = T.K$$
$$Y = T.\overline{K}.$$

(i) Complete the truth table for the demultiplexer.

T	K	X	Y

[3]

(ii) Complete the timing diagram of Fig. 6.2 for the demultiplexer.

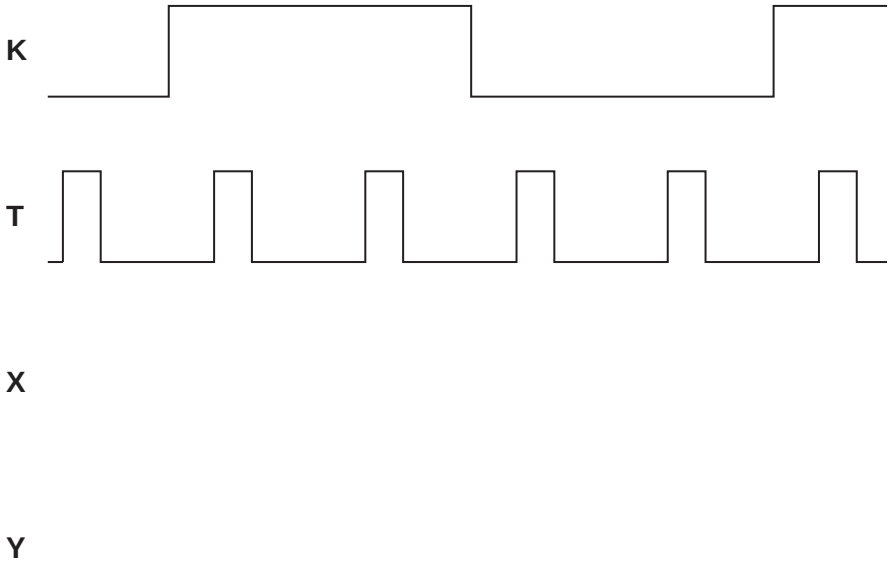

Fig. 6.2 [2]

(iii) In the space below, show how the demultiplexer can be made from four NOR gates. Use a truth table or Boolean algebra to justify your design.

[4]

Quality of Written Communication [3]

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